JEITA

Standard of Japan Electronics and Information Technology Industries Association

EIAJ ED-4701/300-2

Environmental and endurance test methods for semiconductor devices (Stress test I) (Amendment 2)

Established in June, 2004

Prepared by
Technical Standardization Committee on Semiconductor Devices

Published by
Japan Electronics and Information Technology Industries Association

11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan
Printed in Japan

Translation without guarantee in the event of any doubt arising, the original standard in Japanese is to be evidence.

JEITA standards are established independently to any existing patents on the products, materials or processes they cover.
JEITA assumes absolutely no responsibility toward parties applying these standards or toward patent owners.

CONTENTS

EIAJ ED-4701/300-2

Standard of Japan Electronics and Information Technology Industries Association

Environmental and endurance test methods for semiconductor devices (Stress test Ⅰ) (Amendment 2)

1. SCOPE

Conforming to **EIAJ ED-4701/300** “Environmental and endurance test methods for semiconductor devices (Stress tests Ⅰ)”

2. DEFINITION OF TERMS

Conforming to **EIAJ ED-4701/300**

3. PRECAUTIONS

Conforming to **EIAJ ED-4701/300**

4. TEST METHODS

Conforming to **EIAJ ED-4701/300**

Remarks: The Process of deliberation and technical description of each test methods are given to the test methods as Explanation.

COMMENTS

1. PURPOSE OF ESTABLISHMENT OF THE AMENDMENT 2

It was recondite where the latest test methods was entered, it was resulting the confusion of users. So establishment of new numbering system that was easy to use both users and manufacturers was decided, and the standard has been established as **EIAJ ED-4701/300** “Environment and endurance test methods for semiconductor devices (Stress test Ⅰ)” in August, 2001.

The change of a technical matter is needed in the test methods in part, we decided after that to publish only the test methods of requiring change as the Amendment. However, every three years it will be established as not the Amendment but the latest version of the standard “Environment and endurance test methods for semiconductor devices (Stress test Ⅰ)” that includes the whole test methods of **EIAJ ED-4701/300**.

2. EVOLUTION OF THE DELIBERATIONS

The evolution of the deliberations is conformed to the explanation of each test methods.

3. DELIBERATING MEMBERS

Deliberation of this standard has been made by “Sub-Committee on Semiconductor Devices Reliability” of the Technical Standardization Committee on Semiconductor Devices/Semiconductor Devices Reliability Group.

Below are listed the members of deliberation of this standard.

<Technical Standardization Committee on Semiconductor Devices/Semiconductor Devices Reliability Group>

Chairman	Kazuo Endo	NEC Electronics Corp.

<Semiconductor Devices Reliability Group>

Chairman	Kazutoshi Miyamoto	Renesas Technology Corp.

<Sub-Committee on Semiconductor Devices Reliability>

Chairman	Tetsuaki Wada	Matsushita Electric Industrial Co., Ltd.
Vice Chairman	Masaki Tanaka	Renesas Technology Corp.
Member	Tadafumi Tashiro	NEC Electronics Corp.
	Yasuhito Anzai	Oki Electric Industry Co., Ltd.
	Osamu Nakayama	Kawasaki Microelectronics, Inc.
	Kazutoshi Kitazume	Sanyo Electric Co., Ltd.
	Makoto Kanayama	Shindengen Electric Mfg. Co., Ltd.
	Shinichi Ikezoe	New Japan Radio Co., Ltd.
	Hiroyoshi Odaira	Seiko Epson Corp.
	Hisashi Hosoya	Sony Corp.
	Takumi Tanabe	Toshiba Corp.
	Yasuyuki Igarashi	IBM Japan, Ltd.
	Toshiki Yamaguchi	Fujitsu Ltd.
	Naohiro Yasuda	Fuji Electric Co., Ltd.
	Masashi Kusuda	Mitsumi Electric Co., Ltd.
	Kohki Ohara	Ricoh Co., Ltd.
	Takahiro Ito	Rohm Co., Ltd.
Special Members	Takeshi Watanabe	NEC Electronics Corp.
	Takayasu Handa	NEC Electronics Corp.
	Yasuhiro Fukuda	Oki Electric Industry Co., Ltd.
	Hirofumi Yamazaki	Sharp Corp.
	Kouji Obinata	Sony Corp.

Test Method 305
Charged device model electrostatic discharge (CDM/ESD)

1. Scope

This standard specifies the test method for clarifying resistance when integrated circuits are exposed in the electrostatic discharge of the charged device model during handling until integrated circuits are mounted in electronic equipment.

Note: Although this test method is based on the model to which a charged device discharges toward metal, this test method corresponds also to the model to which charged metal tools discharge toward a device (the polarity of an electrical potential just before discharge has a reverse relation). Moreover, although this test method is based on the discharge model after the device was charged directly, since equivalent discharge occurs, this test method can correspond also to the discharge model after the static induction of the device.

2. Terminological definition

The terms used by this standard are defined as follows.

(1) Standard test module

For verifying test equipment, it is the disk made with the metal specified the size, and is put on the place which places the DUT in test equipment, and charge and discharge are made.

(2) DUT

Semiconductor device for performing a test.

(3) Initial measurement

Measurement performed before testing DUTs.

(4) Final measurement

Measurement performed after testing DUTs.

3. Test equipment

In this test, test equipment shall be manufactured based on the test circuit shown in **3.1**, and shall satisfy the verification conditions specified in **3.3**.

3.1 Test circuit Test equipment shall satisfy the following items.

(1) As shown in **Fig. 1**, the DUT shall be able to be held in contact with the top of the insulating sheet stuck on the metal plate. The metal plate shall be maintained at the electrical potential of grounded or stabilized, and shall be wider than a DUT enough. Metal plates can be divided as shown in **Fig. 2**, and they can be maintained by different electrical potential, respectively.

Note: The insulating sheet should be made from glass epoxy material (FR-4 etc.) with the thickness of 0.40 ± 0.04 mm, the dielectric constant of 4.0 ± 0.5 (1GHz), volume resistivity more than 1 × 1015Ωm, and withstand voltage more than test voltage.

(2) The metal bar/board just before discharging shall be maintained by the electrical potential of the ground.

Note 1: The metal bar/board shall be grounded by wiring (electrical potential of the case of test equipment etc.).

2: By adjusting the form and size, a metal bar/board should satisfy specification of verification of **3.3**.

(3) As shown in **Fig. 1** and **Fig. 2**, test equipment shall be able to hold all the terminals of a DUT to the specified electrical potential.

When connecting high voltage power supply to the terminal of a DUT through wiring, the resistor R_1 that bears test voltage between high voltage power supply and a DUT shall be connected in series.

Although 10MΩ to 100MΩ is appropriate to the value of the protection resistor R_1 for charge, the resistance may be still higher when satisfying the conditions shown in **3.3**.

When the terminal of a DUT is connected to high voltage power supply through an electrode, connect resistor R_2 or resistive material R_2 of 1MΩ to 10MΩ in series near the electrode.

When all terminals need to be charged at the specified potential as shown in **4.2 (1)**, R_3 shall be contacted for all the terminals of DUT. The volume resistance of a resistive material R_3 should be 1 × 108Ωm from 1 × 104Ωm.

The following procedure shall be able to be performed when a resistive material R_3 cannot contact all the terminals of a DUT. First, the electrode of test equipment is connected to the power supply terminal of a DUT, and voltage is applied to an electrode. Next, an electrode is separated from a power supply terminal, maintaining the voltage. Furthermore, an electrode is connected to a terminal under test, maintaining the voltage. (see the **Note 2** of **4.2 (3)**)

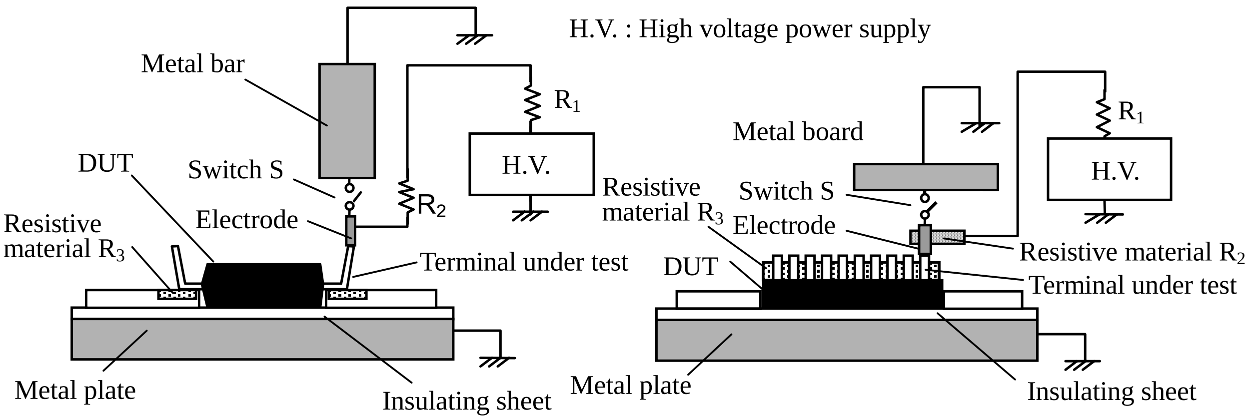
Note: In order to avoid that the electric charge charged on wiring influences discharge, resistor R_2 must be connected near the electrode. When R_2 is a resistive material, as shown in **Fig. 1 (b)**, connect with the electrode of test equipment directly.

(4) The electrode of **Fig. 1** or the tip of the metal bar/board of **Fig. 2** shall be able to contact the terminal under test of a DUT.

(5) The switch of **Fig. 1** shall have sufficient withstand voltage to test voltage.

Note: A switch shall be a high withstand voltage mercury lead switch. Moreover, the resistance of contact and the capacitance of contact should be small enough.

(6) For verification, 1Ω disk resistor as a current detector is mounted in a metal bar/board, and there must be with the structure which can measure the voltage generated in a resistor when the discharge current flows from the center of a resistor to a metal bar/board using 50Ω coaxial cable and an oscilloscope (see **3.3.3**).



(a) Example using a metal bar

(b) Example using a metal board and a resistive material R_2

Fig. 1 Example of equipment that holds electrical potential of DUT from electrode side, and discharges with switch (current measurement circuit is omitted)

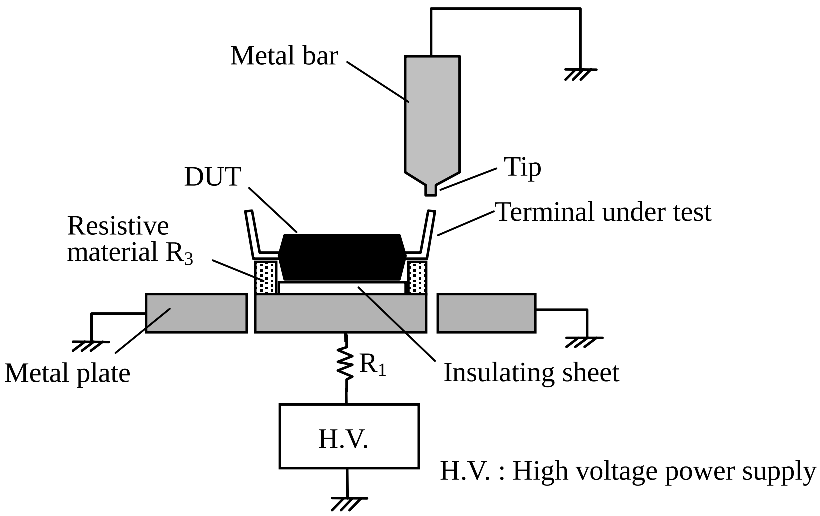


Fig. 2 Example hold electrical potential of DUT from the metal plate side using divided metal plate, and according to aerial discharge (current measurement circuit is omitted)

3.2 Standard test module

The standard test modules made to charge and discharge for verification should have the large and small shape of two kinds of metal disks shown in **Table 1**.

Note: The surface of a standard test module must be able to maintain good electric contact by plating of gold etc.

Table 1 Dimensions of the standard test modules

Type of modules	Small	Large
Diameter (mm)	9.0 ± 0.1	25.0 ± 0.2
Thickness (mm)	1.3 ± 0.1	1.3 ± 0.1

3.3 Verification of test equipment

Before the verification of test equipment, the measurement circuit for the verification shown in **3.3.2** must be evaluated, the correction coefficients to the peak current values measured in verification must be obtained, and test equipment must be verified using the correction coefficients in **3.3.3**.

3.3.1 Equipment for Verification

(1) The oscilloscope used for verification can measure a single shot pulse, input impedance should be 50Ω and frequency bandwidth should be 2GHz or more.

(2) The bandwidth of a current probe should be 2GHz or more.

3.3.2 Evaluation procedure of measurement circuit for verification

As shown in **Fig. 3**, since the current detector by 1Ω resistor has low accuracy, the measurement system for verification including the current detector must be evaluated using a current probe.

Note: In high frequency bandwidth, by the parasitic inductance in a resistor and a point of contact, since the impedance of the current detector by 1Ω resistor is not 1Ω, there is not accuracy sufficient as a current detector for high frequency. Therefore, the current probe which can carry out verification is regarded as the primary standard of a current detector, the measurement circuit for verifying test equipment shall be evaluated before carrying out verification, and then, test equipment shall be verified.

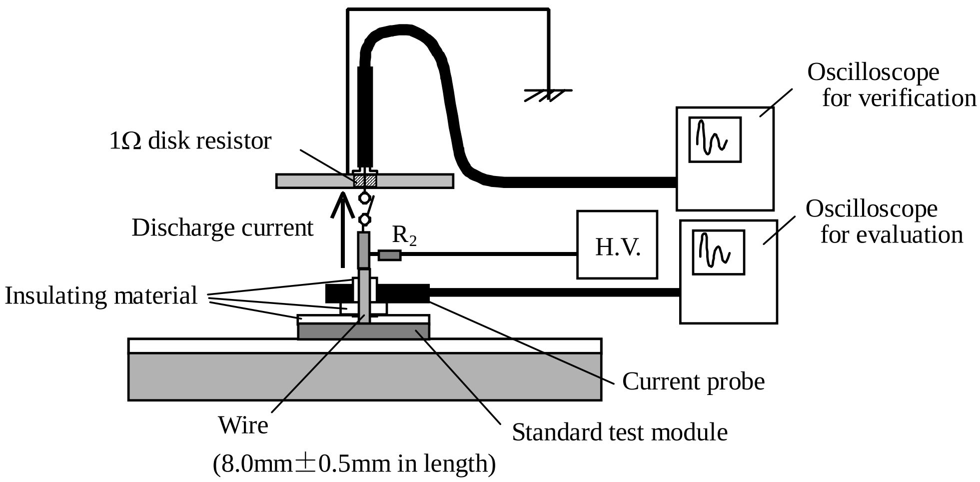


Fig. 3 Circuit for evaluating measurement circuit for verification

(1) Place a standard test module on an insulating sheet. And as shown in **Fig. 3**, put through the metal wire (lead wire) of 8.0mm ± 0.5mm length in a current probe, and place and contact it between a standard test module and the electrode of test equipment. Next, connect the coaxial cable connected to the oscilloscope to a current probe or the current detector of 1Ω disk resistor. Clean an insulating sheet etc. using Isopropyl alcohol etc. When an oscilloscope does not have two sets, carry out by one set.

(2) Set high voltage power supply to 100V, and hold the electrical potential of a standard test module. Next, close a switch and make it discharge from a standard test module. And measure the peak value of the discharge current that flows in a current probe and 1Ω disk resistor, respectively, and record it. The measurement shall be carried out to large and small standard test modules. When there is only one oscilloscope, it may be measured by turns.

(3) Next, assign the peak current values measured in **(2)** to a formula **(1)**, and obtain the correction coefficient C_r to the peak current.

$$C_r = \frac{I_{p\_c}}{I_{p\_r}} \qquad \dots \quad \textbf{(1)}$$

C_r: Correction coefficient

I_{p_c}: Measured peak current by the current probe

I_{p_r}: Measured peak current by the radial 1 ohm resistor
(current detector in test equipment)

(4) The correction coefficients C_r obtained for every large and small standard test module should be in the range of 0.8 to 1.2.

3.3.3 Verification of test equipment

In the verification of test equipment, the discharge current from the standard test module charged as shown in **Fig. 4** shall be detected with the current detector using 1Ω disk resistor, and shall be measured with an oscilloscope. However, before carrying out verification, the measurement circuit for the verification shown in **3.3.2** shall be evaluated, and correction coefficients shall be obtained. The verification procedure of test equipment is shown below.

(1) Standard test modules, an insulating sheet, etc. should be cleaned by Isopropyl alcohol etc.

(2) Place a standard test module on an insulating sheet, and as shown in **Fig. 4**, contact the electrode to it.

(3) Hold the electrical potential of a standard test module based on specified test procedure shown in **4.2**. Unless otherwise specified, an electrical potential shall be set to 500V and 1000V, and shall be carried out to the polarity of positive/negative.

Note: When testing exceeding 1000V, verification shall be performed with an electrical potential higher than it, for example, the electrical potential of the positive/negative of 2000V.

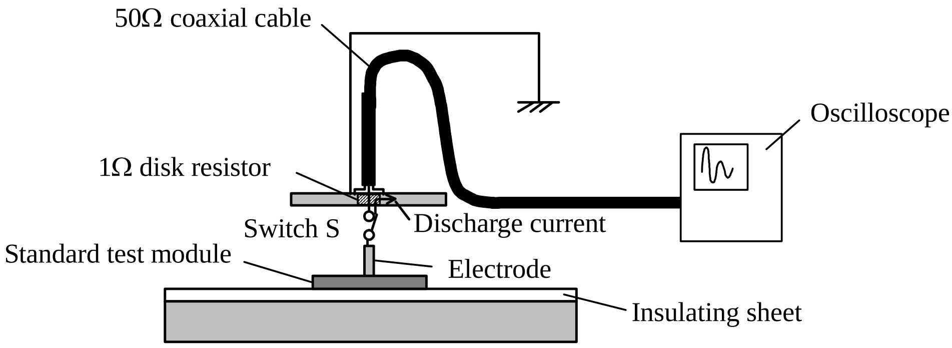


Fig. 4 Verification circuit of test equipment (circuit for charging standard test module is omitted)

(4) Close Switch S and measure the discharge current waveform from a standard test module with an oscilloscope. And acquire the value of t_r, t_d, I_{p2}, and I_{p3} shown in **Fig. 5** from the measured waveform. Acquire the values of the peak current I_{p1} by assigning the correction coefficients C_r for every standard test module obtained by **3.3.2**, and the measured peak current values to a formula **(2)**.

$I_{p1} = C_r \, I_{p1\_m}$ ... **(2)**

Here C_r: Correction coefficients obtained in **3.3.2**

I_{p1_m}: Peak current value corresponded to I_{p1} read from measured waveform

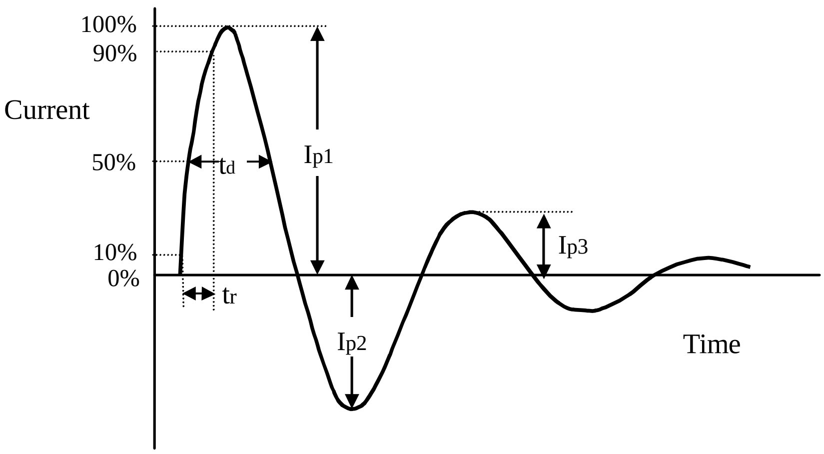


Fig. 5 Current waveform

Note: The measured waveform needs to be similarity at the waveform measured by **3.3.2**.

(5) The values of t_r, t_d, I_{p2}, and I_{p3} shall satisfy the values specified in **Table 2**. The peak current I_{p1} shall satisfy the values specified to **Table 3**.

Note: In the case of aerial discharge like **Fig 2**, since the peak current I_{p1} tends to be saturated with a high-voltage test, specified value may not be satisfied.

In such a case, test equipment shall be used within the limits of satisfying verification voltage.

Table 2 Specified current waveform

Item (unit)	Symbol	Specified values	
		Small standard test module	Large standard test module
Rise time (ps)	t_r	300 or less	400 or less
Pulse width (ps)	t_d	600 or less	800 or less
Peak current (A)	I_{p1}	(see **Table 3**)	(see **Table 3**)
Undershoot current (A)	I_{p2}	Less than 50% of I_{p1}	Less than 50% of I_{p1}
Overshoot current (A)	I_{p3}	Less than 25% of I_{p1}	Less than 25% of I_{p1}

Table 3 Specification of peak current I_{p1}

Verification voltage (V) ([1])	Renge of peak current I_{p1}	
	Small standard test module	Large standard test module
500	4.0A ± 10%	5.5A ± 10%
1000	8.0A ± 10%	11.0A ± 10%

Remark([1]): I_{p1} is proportional to a verification voltage value. When verifying exceeding 1000V, I_{p1} shall be proportional to the value of a table.

4. Test Procedure

4.1 Initial measurement

It shall be carried out according to the item and conditions that were specified to relevant specification.

4.2 Test

(1) Place a DUT on an insulating sheet. When placing, all the terminals of a DUT must be contacted to a resistive material R_3. In the case of the structure where the whole DUT can be charged only by the charge from a terminal under test, contact of a resistive material R_3 has an unnecessary inside of a DUT. The ambient temperature under test shall be 25 ± 5C°.

Note: In the inside of a DUT, the charge from all the terminals by contact of a resistive material R_3 is required for a DUT having the portion electrically isolated from the terminal under test.

(2) Contact the electrode of test equipment to the terminal under test of a DUT. In the case of the test equipment of **Fig. 1**, Switch S shall be opened and the electrode shall contact to the terminal under test of a DUT.

(3) Set high voltage power supply to the test voltage specified to relevant specification, and maintain the electrical potential of all the terminals of a DUT at the test voltage.

Note 1: Test voltage recommends 500V.

2: When all the terminals of a DUT need to be charged and a resistive material R_3 cannot contact all the terminals of a DUT, the electrical potential of one power supply terminal of a DUT and a terminal under test may be made to hold by the following method of not using a resistive material R_3, and a test may be carried out.

First, contact the electrode for one power supply terminal (power supply terminal common to DUTs, such as GND or V_{cc}) of a DUT. And set high voltage power supply to specified voltage, and maintain the electrical potential of the power supply terminal at specified value. Next, where the electrical potential is outputted to the electrode, separate the electrode from the power supply terminal, and where an electrical potential is outputted to the electrode, connect the electrode to a terminal under test. Repeat this operation for every terminal under test and test voltage.

(4) In the case of **Fig. 1**, close Switch S, in the case of **Fig. 2**, contact the tip of a metal bar/board to the terminal under test of a DUT, and make it discharge toward a metal bar/board from a DUT.

Note: While carrying out the test, the electrode or the tip of a metal bar/board needs to check being certainly contacted to the terminal under test of a DUT with viewing, a camera, etc.

(5) The number of times of discharge shall be 1 time unless otherwise specified in the relevant specification. When plural number of discharge is specified, the procedure of **(3)** and **(4)** shall be repeated. However, the interval of discharge shall be 0.1s or more.

Note: When specified in the relevant specification, the procedure of **(5)** may be performed after changing the polarity of test voltage.

(6) By changing a terminal under test, the procedure of **(2)** to **(5)** must be repeated and all the terminals of the DUT must be tested.

(7) The polarity of test voltage shall be changed and then **(2)** to **(6)** shall be repeated.

Note: In the stage that the procedure of **(6)** ended, intermediate measurement may be carried out, or DUTs may be exchanged and the procedure of **(7)** may be carried out.

4.3 Final measurement

Measure according to the items and conditions specified in the relevant specification.

5. Alternative verification method of test equipment

Although the verification method of test equipment was specified to **3.3**, since the new test equipment which can equip a metal bar/board with the current detector using 1Ω disk resistor shown in **Fig. 3** and **Fig. 4** has not fully spread when this standard is published, when there is specification of relevant specification, the equipment may be verified on condition that the following.

5.1 Standard test module

The standard test module specified in **3.2** must be used.

5.2 Measurement conditions for test equipment verification

By the circuit shown in **Fig. 5**, test equipment shall be verified by measuring the discharge current from a standard test module with the oscilloscope and current probe specified in **3.3**.

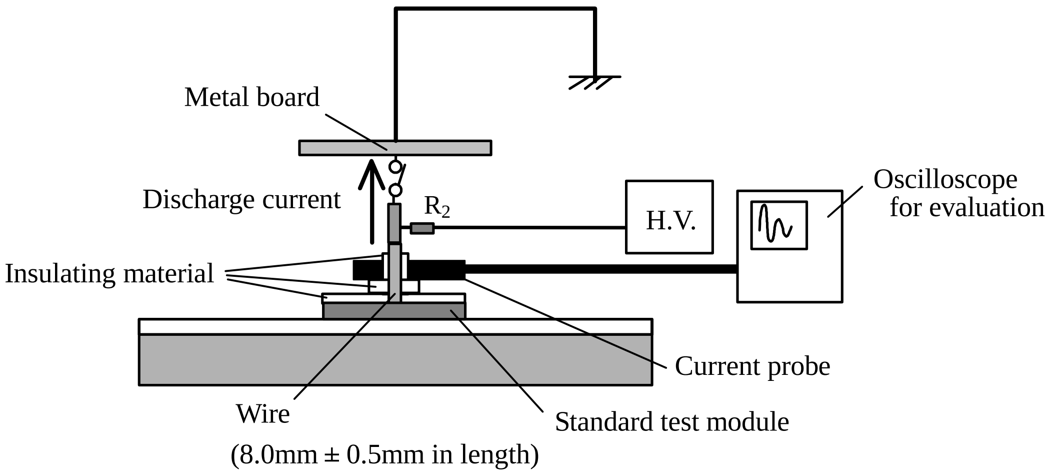


Fig. 5 Example of measurement circuit for alternative verification method

5.3 Verification procedure

The current measurement procedure using the current probe specified in **3.3.2** shall be applied. The voltage for verification should be 500V and 1000V.

Note: Since a current probe cannot bear the high voltage, when applying this method, it fully needs to maintain the insulation between the current probe and the high-voltage circuit.

5.4 Specification of waveform

The value except the peak current should satisfy **Table 2**. And the peak current shall satisfy **Table 4**.

Note: In this measuring method, from the method specified to **3.3**, since a metal bar/board is in a high place only 8mm, a peak current value becomes small. Most of the test equipment spreading now are considered that in general good correlation between the values of **Table 4** and **Table 3**.

Table 3 Specifications of peak current I_{p1} for alternative verification method

Verification voltage (V)	Renge of peak current I_{p1}	
	Small standard test module	Large standard test module
500	3.5A ± 10%	4.5A ± 10%
1000	7.0A ± 10%	9.0A ± 10%

6. Information to be given in the relevant specification

(1) Voltage for verification [Refer to **3.3.3**]

(2) The items and conditions of initial measurement [Refer to **4.1**]

(3) Ambient temperature during test (when other than specified) [Refer to **4.2 (1)**]

(4) Test voltage [Refer to **4.2 (3)**]

(5) The number of times of discharge (when other than specified) [Refer to **4.2 (5)**]

(6) Repetition interval of discharge (when other than specified) [Refer to **4.2 (5)**]

(7) Procedure of changing polarity of test voltage (when other than specified) [Refer to **4.2 (5)** and **(7)**]

(8) The items and conditions for intermediate measurement (when required) [Refer to **4.2 (7)**]

(9) The item and conditions for final measurement [Refer to **4.3**]

(10) Appling alternative verification (if necessary) [Refer to **5.**]

REFERENCE　DESCRIPTION ABOUT TEST METHOD

1. The progress of establishment

Progress of this test method establishment is shown below.

1.1 Charged package model of EIAJ IC-121

Generally the charged package model test method (similar to the Field induced CDM) classified into a charged device model test method was being accepted for the reason of the test method which reproduces correctly the ESD damage phenomenon which happens during device handling.

And “the charged package model (proposal)” was written together in the description of the “test method 20 electrostatic discharge test” in Electronic Industries Association of Japan (**EIAJ**) standard **EIAJ IC-121** published in 1988. Then, “the charged package model test method (proposal)” was written together as reference in the “test method C-111 electrostatic discharge test” in standard **EIAJ ED-4701** by integration with **EIAJ IC-121**, and **EIAJ SD-121**, published in 1992

1.2 Charged device model test method of EIAJ ED-4701 (provisional standard)

Since the charged package model was written together in 1988, the research on the test has progressed and test equipment has also spread in Japan, revision of the “C-111 electrostatic discharge test” of **EIAJ ED-4701** was determined as a main theme of the semiconductor reliability committee in 1992-1993, and deliberations were advanced.

Since the charged package model test method and the charged device model test method had the same transient phenomenon under discharge in the electrical circuit theory, they could be classified as the same test method, therefore they were made into same name called the test method of charged device model electrostatic discharge, and were published in 1994 as test method separated from the test method C-111 human body model electrostatic discharge. However, the charged device model test method simulated several GHz discharge, therefore it needed advanced high frequency measurement technology for the verification of test equipment, and since it had not solved the problem, it was published as a provisional standard.

1.3 Present charged device model test method

It had deliberations for publishing a charged device model test method as a regular standard as a theme in 2001 and 2002. The main changed parts to the former are shown below.

(1) The verification method which measures current at the metal bar/board side using the standard test modules of the shape of a disk made with the metal specified in **JEDEC** standard **JESD22-C101** was adopted.

(2) In order to compensate the inaccuracy of 1Ω current detector, the evaluation technique of 1Ω current detector for verification that used the current probe was adopted.

(3) The peak current values of a discharge waveform based on the new verification method were determined.

(4) The small capacity discharge test method that was being written together as an alternative test was abolished.

2. Progress of deliberations

Revision of this test method deliberated by the above-mentioned meaning by the semiconductor reliability sub-committee of the semiconductor reliability group. The contents of deliberation were advanced having reported to the semiconductor reliability group and obtaining recognition. Deliberations were advanced about change of the verification method, obtaining the technical cooperation of two companies of domestic test equipment makers.

3. Technological background of test method

Below, the technical items in this test method are explained.

3.1 Change of the thickness and dielectric constant of insulating sheet

Although the thickness of the insulating sheet between the metal plate and DUT (see **Fig. 1** and **Fig. 2** of this test method) was conventionally specified as 1.0 ± 0.2mm, and its dielectric constant was specified as 2.0 ± 0.5, they were revised into 0.40 ± 0.04mm in thickness and 4.0 ± 0.5 (1GHz) in dielectric constant under the necessity of harmonizing with **JEDEC** standard this time. However, since this value is a reference value, even if it is outside the range, test equipment will not deviate from this standard, if verification passes.

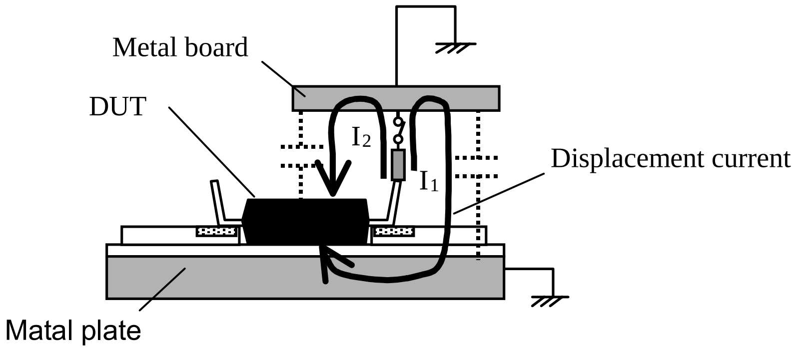
Although the dielectric constant in low frequency band influences the charge to a DUT, since the discharge current that damages a DUT is in high frequency band (1GHz or more etc.), the dielectric constant value in high frequency is suitable as specification. For example, although the dielectric constant in the low frequency of the glass epoxy (FR-4) is about 4.8, it becomes 4.5 or less in 1GHz. When it is assumed that the value in 1GHz is 4.3, the capacitance of the DUT or the standard test module will be 0.9 times (= 4.3/4.8 time) the capacitance in low frequency. In this case, it means that 90% of the electric charge of the charged the DUT or the standard test module discharges at high speed (high frequency), and 10% of the remaining electric charges discharge gently (low frequency). Since the CDM discharge that damages devices is in high speed, the value in high frequency should be used for specification of a dielectric constant used for the CDM test.

3.2 Expression of the discharge current and test circuit

Since the CDM discharge current consists of high frequency current, it not only flows the inside of conductors, but flows in the capacitance between conductors as displacement current.

The main discharge currents of a charged device model consist of the current I_1 which flows the inside of the capacitance between a metal bar/board and a metal plate, and the current I_2 which flows the inside of the capacitance between a metal bar/board and a DUT, as shown in **Reference fig. 1**.

As shown in **Fig. 1** and **Fig. 2** of this test method, although the test circuit was conventionally expressed with the circuit diagram by symbols, such as a resistor and a capacitor, as explained above, since the form of a metal plate or a metal bar/board becomes important, in CDM, the test circuit figure is expressed by external view.



Reference fig. 1 The main element of the discharge current

3.3 How to place DUT

In order to generate the capacitance of DUT, DUT is placed on the insulating sheet stuck on the metal plate. Since the capacitance and inductance that are parasitic on the IC socket and the wiring connected to it will be added to the electrical characteristics of the DUT when the IC socket is used for set of DUT, don’t use the IC socket.

Moreover, as shown in following **(1)** to **(4)**, in the actual environment, it is reported that thin devices have the tendency not to be charged rather than thick devices. However, when thin devices are placed in contact with a metal plate top, there is inconsistency that the amount of electric charges charged increases than that of thick devices since the capacitance is larger than thick devices. If a thick insulating sheet is used, the increase of capacitance of thin devices can be suppressed. Therefore, the thickness of an insulating sheet is specified as 1mm. However, since the effect is not enough, even now, the CDM test for thin devices is severe.

Thus, generally, since thin devices are damaged in low test voltage, they have been misunderstood that they have the tendency to be easily charged at an actual handling process. When testing thin devices, it is necessary to understand these well and to carry out the CDM test.

(1) It is rare to be charged in the state where devices are in contact with metal. It is thought that it is charged in the state where it separated with metal. The capacitance of the devices in this case is small, and does not depend on the thickness of a package.

(2) In a triboelectrification, the amount of electrical charge is unrelated to a capacitance of devices depending on material, a friction speed, friction force, etc. If it is charged by friction etc. during thin devices have touched metal, the electrification voltage V of thin devices with a large capacitance C will become low by a formula **(1)**. Moreover, when a charged object approaches the devices that touched metal and static induction happens, the induction voltage of a thin device with a large capacitance becomes low.

$$V = Q/C \qquad \dots \quad \textbf{(1)}$$

(3) Since the amount Q of electric charges does not change even if devices move, when devices approach metal after being charged, when capacitance C of devices increases, the electrification voltage V becomes low [refer to formula **(1)**]. The electrification voltage of thin devices with the large capacitance when approaching metal tends to become low.

(4) If thin devices are placed on conductors, electrification voltage will tend to fall by creeping discharge etc.

3.4 Electrical potential of metal plate, and division

Since the discharge current is in high frequency, a test circuit must be equivalent in high frequency bandwidth. It is necessary to maintain a DUT at a test electrical potential and to maintain a metal bar/board at a standard electrical potential (the ground or electrical potential of a case) for that purpose, just before discharge.

Moreover, since the alternating current of high frequency of the discharge current is main, low frequency current and direct current that do not cause damage can be disregarded. Therefore, if the transitional state is equivalent, it is not necessary to limit the metal plate just before discharge to a grounding electrical potential, and it should just be maintained at the stable electrical potential. Moreover, as shown in **Fig. 2** of this test method, even if the metal plate is divided, since it is combined by the capacitance that exists among them, it has an effect equivalent to one metal plate.

The charged package model written together as a test method proposal in **EIAJ IC-121** and **EIAJ ED-4701** was a method of dividing a metal plate and maintaining a central metal plate to an test electrical potential as shown in **Fig. 2** of this test method. It is possible that the method is equivalent to other methods of having used one metal plate.

3.5 Grounding wiring of metal bar/board

In order to hold the metal bar/board just before discharge to a standard electrical potential (the ground or electrical potential of a case), it is necessary to connect a metal bar/board to a standard electrical potential by the wiring. The resistor may be connected in series to grounding wiring if needed. The resistor needs to be less than 10kΩ. Since grounding wiring becomes an antenna and emits a noise, the resistor is effective in preventing generating of an unnecessary noise. However, when the mercury lead switch of a high withstand voltage is not used as a switch S, an electric charge moves to a metal bar/board from a DUT by the corona discharge just before CDM discharge, and cautions are required when using the resistor, since the electrical potential of a metal bar/board becomes unstable.

Since the metal bar/board, the metal plate, and the DUT are mutually combined by the capacitance, like **Reference fig. 1,** the main discharge currents do not flow grounding wiring, but flow the inside of space (capacitance) as the displacement current, and reach a DUT. The main current influences directly the values of t_r, t_d, and I_{pl} that have been specified to **Table 2** and **Table 3** of this test method.

3.6 Impression method of an electrical potential to DUT

Since there is the following problem, it is necessary to connect all the terminals of DUT to high voltage power supply through resistor R_3, and to maintain all terminals to test voltage.

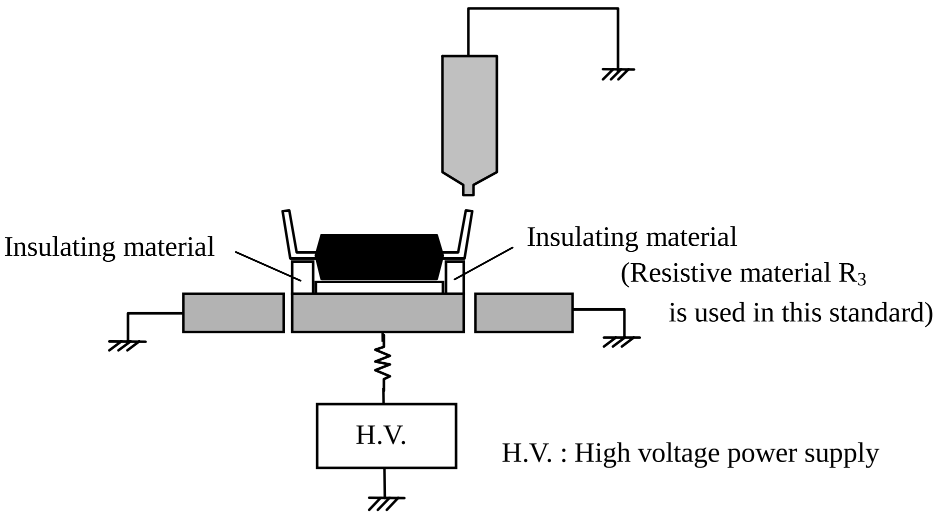
(1) There are the following problems in the electrical potential impression method to the DUT by field induction of **Reference fig. 2**.

(a) Given the capacitance C_2 between a DUT and a metal plate, the capacitance C_1 between a DUT and a metal bar/board, and the voltage V of high voltage power supply, the electrical potential V_{DUT} of a DUT will become clearly lower than test voltage V from a formula **(2)**.

$$V_{DUT} = \frac{C_2 \cdot V}{C_1 + C_2} \qquad \cdots \quad \textbf{(2)}$$

(b) When the DUT and the insulating sheet are contaminated, the electrical potential of a DUT falls by generating of leak current etc.

(c) Since there is a tendency for corona discharge (minute discharge) to happen just before discharge, and for the electric charge of a DUT to begin to leak generally, the electrical potential of a DUT falls. It is aerial discharge, and the impression method of the electrical potential to DUT in a floating state tends to be influenced of contamination, and test results become unstable.



Reference fig. 2 The impression method of the electrical potential to DUT by field induction

(2) When the large portion isolated from input/output terminals is in the inside of a DUT, if all terminals are not charged (for example, back bias circuit of DRAM etc.), it charges unevenly, and test results may differ. Therefore, it is necessary to connect to all the terminals of a DUT the resistive material R_3 shown in **Fig. 1** and **Fig. 2** of this test method, and to make them into the same electrical potential.

The problem shown in **(1)** was discussed when revising **EIAJ IC-121** in 1988, and application of the resistive material (B) equivalent to a resistive material R_3 was specified in “the charged package model test method/ **Reference fig. 4**” of **EIAJ IC-121**. On the other hand, about the problem of **(2)**, since it was confirmed by the experiment by committee members that test results becomes unstable by the heterogeneity of the electrical potential inside a DUT when high voltage power supply was not able to be connected to all the terminals of DUT, even if it was the method of connecting high voltage power supply to a DUT directly, it is shown that the resistive material R_3 of **Fig. 1** and **Fig. 2** of this test method needs to be applied.

In the revision in 2003, since many of devices do not have the portion isolated inside, application of a resistive material R_3 is not indispensable, and when it is judged that it is unnecessary, a resistive material R_3 does not necessarily need to be used.

3.7 Method of discharge

In the case of aerial discharge, corona discharge happens just before CDM discharge, and the electrical potential of a DUT falls. The fall is remarkable when impressing an electrical potential by induction shown in **Reference fig. 2**. In the case shown in **Fig. 2** of this test method, since an electrical potential is maintained through a resistive material R_3, the electrical potential of DUT is stable, but since corona discharge will become remarkable if 1000V are exceeded, it becomes unstable. However, even if it is the case of aerial discharge, verification specified to **3.3** of this test method is carried out, and it is applicable if the conditions are satisfied.

3.8 Adoption of new standard test module

In the provisional standard, the capacitance value in the low frequency of the old standard test module made with a glass epoxy board, and the foil of a circular metal of the both sides was specified, and it used for verification. However, since discharge of an actual DUT was dependent on the capacitance of the DUT in the state where it placed on the insulating sheet, there was a problem in specifying the capacitance of a standard test module.

In the revision in 2003, since the discharge current measurement from the capacitance of the standard test module placed on the insulating sheet was considered to be appropriate as the verification method, the coin module of two sizes adopted in the **JEDEC** standard was adopted. However, although 1GHz conditions need to prescribe the capacitance of the standard test module placed on the insulating sheet, since the measurement is difficult and just measurement of the discharge current is enough as verification, it has not specified in this test method. Although there was some error with the present **JEDEC** standard about the size of standard test modules for use of SI unit, agreement with **JEDEC** determined. It is thought that **JEDEC** will also adopt this size in the future.

3.9 Adoption of 1Ω disk resistor for current detectors

The disk resistor used for detection of the discharge current is converted into 1Ω from 50Ω resistor used for the termination of a coaxial cable.

Although 50Ω resistor for termination has frequency bandwidth 10GHz or more, since 1Ω disk resistor is made to lower only resistance and has not lowered the parasitic inductance, it is not in high frequency bandwidth.

Scalar value |Z| of the impedance Z of 1Ω disk resistor can be expressed with the formula **(3)** in this reference by Resistor R (= 1Ω), Inductance L, and frequency f.

$$|Z| = \sqrt{R^2 + (2\pi fL)^2} = \sqrt{1 + (2\pi fL)^2} \qquad \cdots \quad \mathbf{(3)}$$

Since the waveform measured becomes i(t) |Z| when the discharge current is i(t), the amplitude of waveform measured by disk resistor becomes larger than that of measured by ideal 1Ω resistor.

Therefore, since the amplitude of the measured waveform by 1Ω disk resistor is not true value and the amplitude measured by the current probe shown in **3.3.2** of this test method is judged to be close to true value, the true peak current value can be acquired by rectifying the measurement amplitude value by 1Ω disk resistor.

3.10 Adoption of evaluation of current measurement circuit using current probe

As **3.9** in this reference showed, the current detector by 1Ω resistor cannot detect peak value of the discharge current correctly by the influence of the it's parasitic inductance.

Therefore, it is necessary to newly adopt the current probe which can detect the peak current correctly within 1.5GHz, to compare the peak current value measured by the measurement system by 1Ω disk resistor, and the measurement system by a current probe, and to obtain a correction coefficient by the formula **(1)** in this test method, and it necessary in **3.3.2** of this test method to obtain the true value of the peak current by multiplying the measurement result by 1Ω disk resistor by the correction coefficient.

In order to measure the discharge current with a current probe, the wire needed to be put through in the current probe and the length was specified as 8.0mm ± 0.5mm (refer to **Fig. 3** in this test method). The wire put through to inside needs to isolate from a current probe electrically. Since the wire of 8mm length is used, the position of a metal bar/board becomes high and the capacitance shown in **Reference fig. 1** becomes small, a current value is small generated a little in verification.

In consideration of the withstand voltage of a current probe, the discharge current in 100V is detected by both the current probe and 1Ω disk resistor, and it measures with an oscilloscope. This is carried out about both standard test modules of large and small. It is not necessary to measure simultaneously and may be measured by turns.

As for the value of correction coefficients, it is desirable to go into the range of 0.8 to 1.2. Moreover, it is necessary to verify a current probe periodically.

3.11 Compensation of the peak current in verification

Since the accuracy of the value of the peak current detected by 1Ω disk resistor is low as shown above, the value cannot be used for the verification of test equipment. Therefore, as shown in **3.3.3** of this test method, it is necessary to multiply the peak current value measured by 1Ω disk resistor by a correction coefficient, and to acquire a true value.

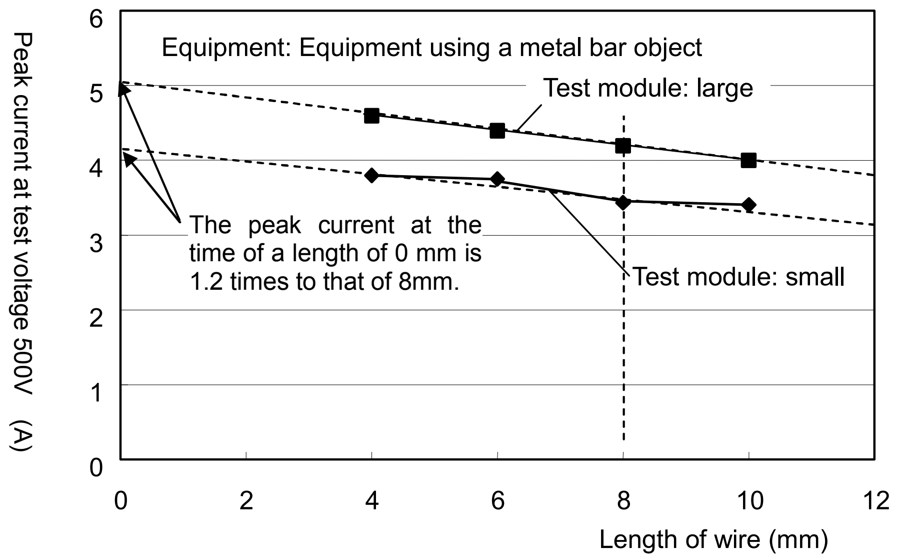
3.12 Alternative Verification Method

Since the test equipment which equipped with 1-ohm disk resistor the metal bar/board shown in **Fig. 3** and **Fig. 4** had not spread in Japan when establishing this standard, implementation of the verification method of the regulation to **3.3** was difficult. Then, the alternative verification method which can be enforced also to conventional equipment was examined, and it wrote together to **5**.

As shown in **Fig. 5**, the method of measuring the discharge current from the module for verification with a current probe via a wire with a length of 8mm was adopted as an alternative method.

In this case, since the metal bar/board for electric discharge is in a position higher about 8mm than a regular method using a wire with a length of 8mm, peak current becomes small from the value specified to **Table 3**. Therefore, the correlativity was examined.

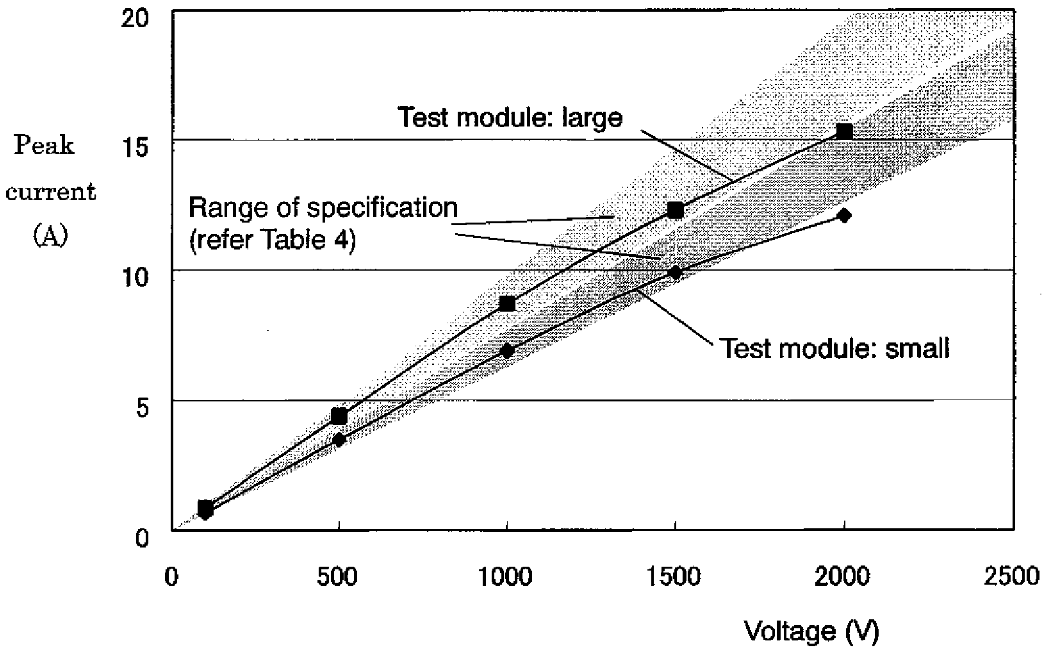
It is thought that implementation of verification with the regular test equipment using a metal bar with difficult attachment of 1-ohm disk resistor is difficult. Then, peak current is measured changing the length of a wire and the example which presumed the peak current value in case length is zero is shown in **Reference fig. 3**. This example shows that a peak current value in case there is no wire can be estimated in general at 1.2 times to the case where the length of a wire is 8mm. Although it was considered by the kind of equipment for the values to differ a little, in order to utilize effectively the equipment which has spread now, the value which carried out verification of the value of **Table 3** by about 1.2 was written together to **Table 4** as a value of the alternative verification method.



Reference fig. 3 Relation between peak current and the length of a wire

Here, when it put through a wire without insulated covering pass in a current probe, it became a problem that the withstand voltage guarantee between a wire and a current probe is low (for example, a maker guaranteed performance is 30V etc.). In **Fig. 3** and **Fig. 5**, insulated covered wire is used and the value adding the withstand voltage of insulated covering is the withstand voltage of the measuring method by a current probe.

By the regular verification method, measurement by 100V is specified and the withstand voltage can be secured easily. By the alternative verification method of impressing actual high test voltage, it is expected to it that the withstand voltage becomes a problem. The measurement result at the time of using as a wire the Teflon covered wire considered that a withstand voltage is high by **Reference fig. 4** is shown.



Reference fig. 4 Example of relation between the voltage and the peak current measured by the alternative verification method

In the example of **Reference fig. 4**, when 1500V are exceeded, it is in the tendency for peak current to be saturated, but the leak current of insulated covered wire or the charge circuit of test equipment etc. can be considered to the reason. In this example, 1500V are in a standard and it can say that they can test.

Although it is thought with the very small leak current generated while using the covered wire of sufficient withstand voltage that a possibility that a current probe will break thermally is low, it is necessary to check the existence of destruction periodically by verification of a measurement system including a current probe.

Test Method 306
Latch up

1. SCOPE

This standard defines the test methods for evaluating the latch-up susceptibility of a semiconductor device (mainly a CMOS devices), by using the constant current pulse and the overvoltage test. The test methods consist of Pulse Current Injection test (Test method I) and V_{supply} Overvoltage test (Test method II). Note that this test is destructive. This test method should not be applied to the devices that have not a parasitic thyristor structure.

2. DEFINITIONS OF TERMS

(1) Clamp voltage (V_{cl})

Voltage limit of the constant current pulse source. The setting of the clamp voltage can greatly affect test results. (Refer to **4.1.6**)

(2) DUT

Device under test

(3) GND (Ground pins)

Common electrical point of the reference potential.

Note: GND is normally at zero potential.

(4) Input pins

Clock, address, data-in and control pins of an LSI. In the case of an analog IC, voltage reference pins (V_{ref}) are also included.

(5) I/O pins

Device pins that can be made to operate in a high-impedance state or to operate as an input or output, depending on the internal or external logic states. Also referred to as bi-directional pins.

(6) Supply current (I_{supply})

The total supply current in each power supply (or ground) pin of the DUT. Also referred to as the supply current flowing into or out of the LSI when latch-up has occurred.

(7) Pulse current injection method (I-test)

A latch-up test that supplies constant current pulses to the pin under test of the DUT. Both positive and negative pulses are applied to the pin under test. The latch-up resistance is measured by the maximum current to which extent the DUT is immune to latch-up.

(8) Latch-up

A state in which electrical overstress such as noise from I/O or power supply pins triggers a parasitic thyristor structure, causing an excessive current to continue to flow between the power and ground lines even after the removal of the triggering condition until power is removed from the LSI.

(9) Logic levels

Logic levels applied to the input pins of the DUT during latch-up testing.

Note: The input pins must be maintained at the GND (ground) or V_{supply} (power supply) pin potential. The pins for which another potential is needed other than GND or V_{supply} such as analog pins shall be defined as per DUT specification in latch-up testing.

(10) Maximum operating voltage (Maximum V_{supply})

The upper limit of the recommended operating voltage range for the DUT.

(11) NC (No connect pin)

A pin that has no internal connection within a semiconductor package.

Note: The application of any external signal or voltage supply to an NC pin of the semiconductor package or the printed circuit board does not disturb the function of the chip. All NC pins shall be left in an open (floating) state during latch-up testing.

(12) Nominal I_{supply} (I_{nom})

The measured dc supply current for each V_{supply} pin (or pin group) with the DUT. If the DUT has multiple power supplies, I_{nom} will also be multiple defined. Latch-up criterion will be defined as an increase from I_{nom}.

(13) Output pin

A device pin that generates a signal or voltage level as a normal function during the normal operation of the device. Output pin is left in an open (floating) state during testing of other pins, except for the case when it is latch-up tested.

(14) Preconditioned pin

A device pin that has been placed in a defined state or condition (input, output, high impedance, etc.) by applying control vectors to the DUT, in order to achieve stable I_{nom}.

Note: The preconditioned pin should be placed in a defined state prior to starting latch-up test.

(15) Power supply

All DUT power supply and external voltage source pins (excluding ground pins), including both positive- and negative-potential pins.

Notes:

1. The DUT sometimes requires multiple voltage levels. The external voltage source must keep its fluctuation within a specified level even when it sinks latch-up trigger current via IO pins in I-test.
2. Generally, it is permissible to treat equal potential voltage source pins as one V_{supply} pin (or pin group) and connect them to one power supply. When forming V_{supply} pins (or pin groups), the combination of V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low supply current pins.

(16) Testing of dynamic devices

Latch-up trigger testing of a device in a known stable state, at the minimum-rated clock frequency applied to the device.

(17) Test condition

Various test conditions during latch-up test.

Note: The test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages, sample size, and preconditioning vectors applied to the DUT are to be recorded during latch-up testing.

(18) Timing-related input pin

A pin such as clock crystal oscillator, PLL, charge pump circuit, etc., required to place the DUT in a normal operating mode.

Note: Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

(19) Trigger pulse

The positive or negative current pulse (I-Test) or voltage pulse (V_{supply} overvoltage test) applied to any pin under test in an attempt to induce latch-up.

Note: The term of "trigger" is used for the definition of the pulse because it may "trigger" thyristor action which may induce latch-up. The latch-up immunity is generally measured by the trigger current level (I-test) or the trigger voltage (V_{supply} overvoltage test).

(20) Trigger duration

The duration of an applied pulse from the trigger source. It is the pulse width of the positive or negative trigger current pulse (in I-test) or voltage pulse, generally positive(in V_{supply} overvoltage test).

Note: The trigger duration has both maximum and minimum specification limits. Longer trigger duration may induce thermal effect on latch-up test result or may induce thermal damage, while shorter trigger duration may not induce latch-up even in the case that latch-up occurs when the duration is a little bit longer.

(21) V_{supply} overvoltage test

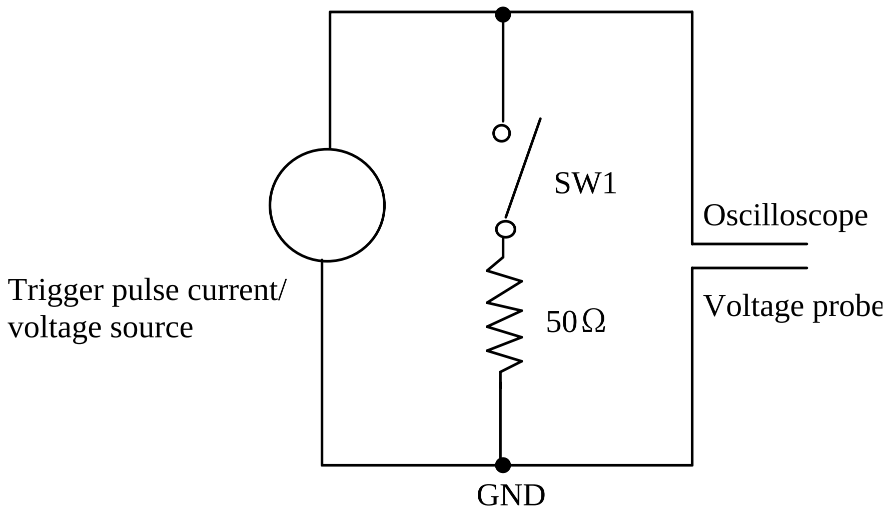
A latch-up test that supplies overvoltage pulses to the V_{supply} pin under test. The criterion will be defined by the pulse height of the overvoltage pulse.

3. TEST EQUIPMENT

The test apparatus for the latch-up test should consist of a power source for generating a current or voltage specified in section **4.1** and **4.2**, a pulse generator, a current detector, and a change-over switch. The waveform of trigger pulse is measured by a circuit (see **Figure 1**), which has a resistor of 50Ω as a standard load with SW1 closed, in order to confirm the compliance with the specification as described in **4.1.3** or **4.2.3**. In the current pulse injection method, ±200mA current pulse is used, and the method also requires the confirmation in which the voltage clamp response to a ±100mA pulse with SW1 open in **Figure 1**, in order to verify the compliance with the specification as described in **4.1.3**. For these confirmations, the pulse generator should be set the clump voltage as ± 15V.

If a device under test (DUT) requires multiple power supply voltages, the apparatus should be equipped with multiple independent power supplies connecting to each power pin, individually.

The test apparatus should also have the capability to supply bias or control vectors to input pins and/or system clock to DUT, if needed, for the purpose of stabilizing I_{nom} (supply current).



Note 1. Load 50Ω ± 5%

Note 2. Probe impedance ≧ 10kΩ

Figure 1 Trigger Pulse Waveform Measuring Circuit

4. TEST PROCEDURE

There are two methods for latch-up testing: Test method I and Test method II. Test method I is Pulse current injection type, which is described in **4.1**, and Test method II is Supply overvoltage type, which is described in **4.2**. The selection of the two methods is determined by the DUT individual specification.

4.1 Test method I (Pulse current injection)

This method is used to evaluate the latch-up immunity against constant current injection to the I/O terminals of the biased semiconductor device. The sample size of the test is determined by the DUT individual specification.

4.1.1 Preprocessing

(1) Input pins shall be biased as the appropriate logic states in order to stabilize I_{nom}, but no rigid control is necessary for a logic state as long as I_{nom} is stable, including the case of testing dynamic devices.

(2) The contact resistance between a DUT and its socket, or non-biased (floating) input pin except for NC pin may affects the test results. Before latch-up testing, the device continuity in the socket and non-biased input pin should be checked to avoid the false latch-up testing.

Notes: All pins on the DUT including timing-related pins, with the exception of “no connect” pins and power supply pins, shall be subjected to the current pulse latch up test. The power supply pins shall be subjected to the V_{supply} overvoltage test. All “no connect” pins on the DUT shall be left open (floating) at all times and are not latch-up tested. It should be noted that Hi-Z (high impedance) I/O terminals may have the worst case in latch-up susceptibility.

4.1.2 Initial measurement

Should be performed according to items and conditions specified in the DUT individual specification. I_{nom} shall be measured.

4.1.3 Test circuit and electrical characteristics

Figure 2 and **Figure 3** show the test circuits for the Test method I. The trigger pulse waveforms should meet the specification as shown in **Table 1**, **Figure 4**, **Figure 5**. Measurement timings are defined as **Figure 6**, **Figure 7** and **Table 1**.

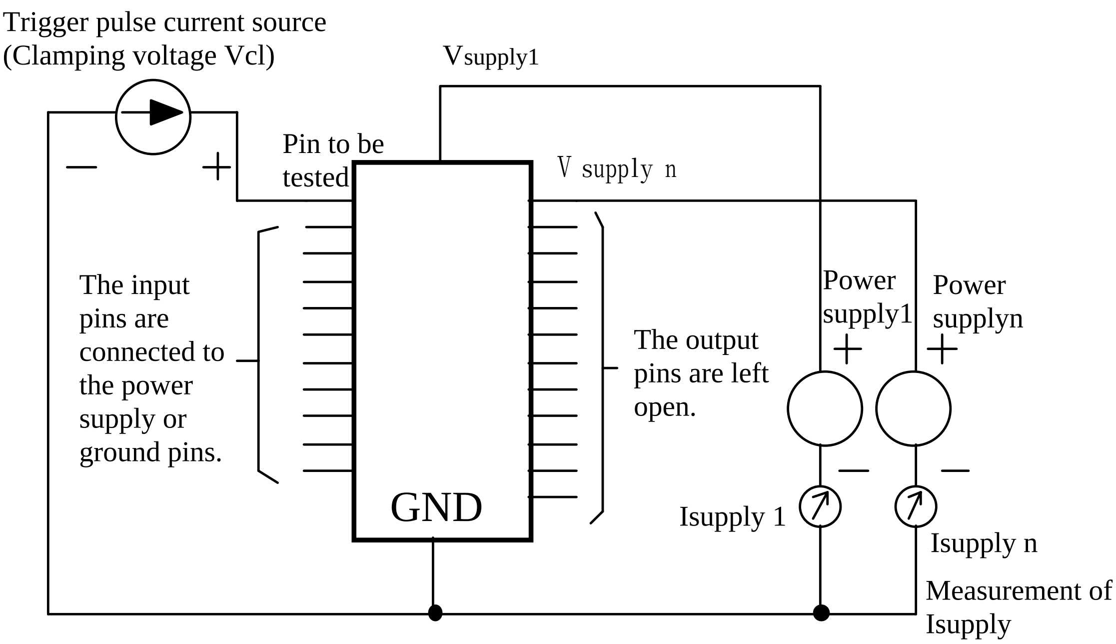


Figure 2 Test Circuit for Test Method I (Positive Current)

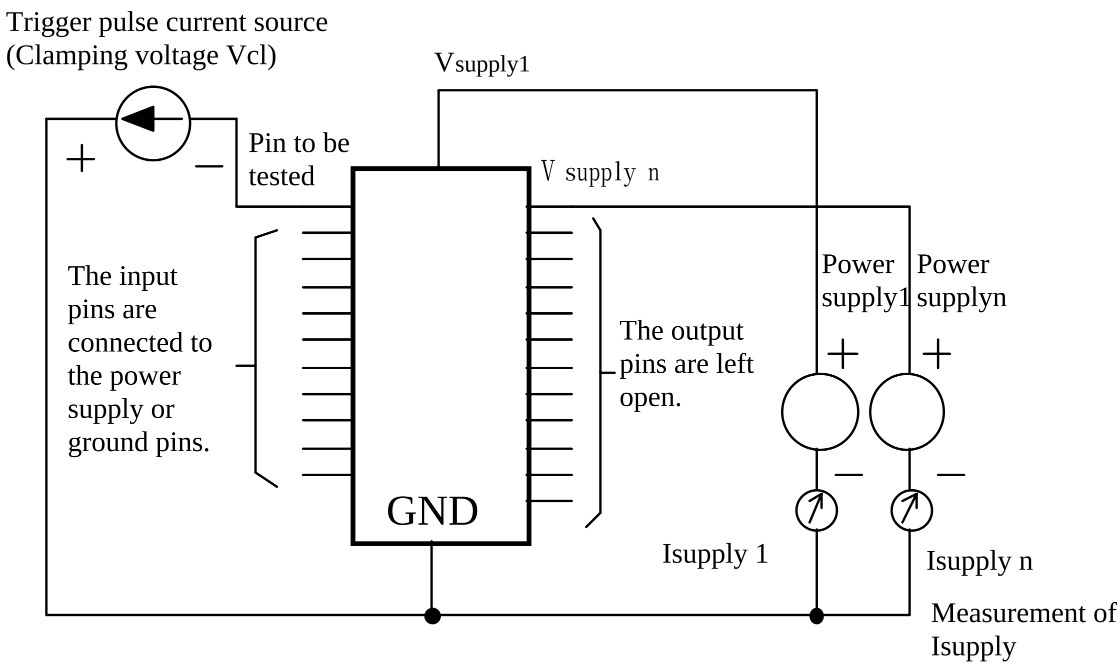


Figure 3　Test Circuit for Test Method I (Negative Current)

Remarks:

1. In case a DUT requires multiple power supply voltages, independent power supplies are required and I_{supply} n shall be measured independently.
2. Output pins shall be left open with the exception of the pin being tested, during the test.
3. The logic level of the inputs shall be H = V_{supply} n and L = GND.

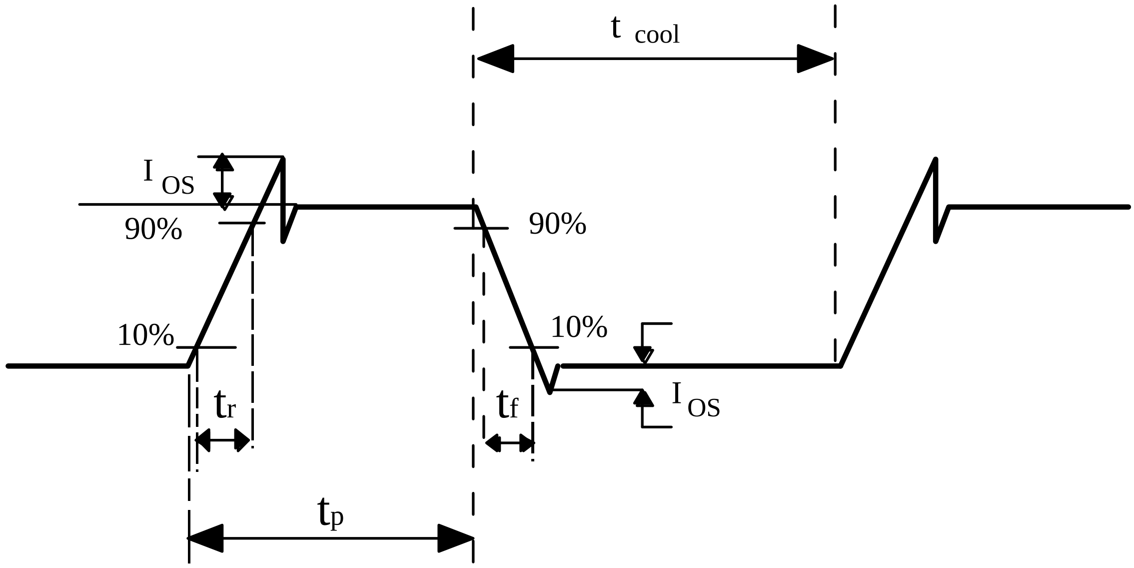


Figure 4　Waveform of Trigger Pulse Current (Positive Current)

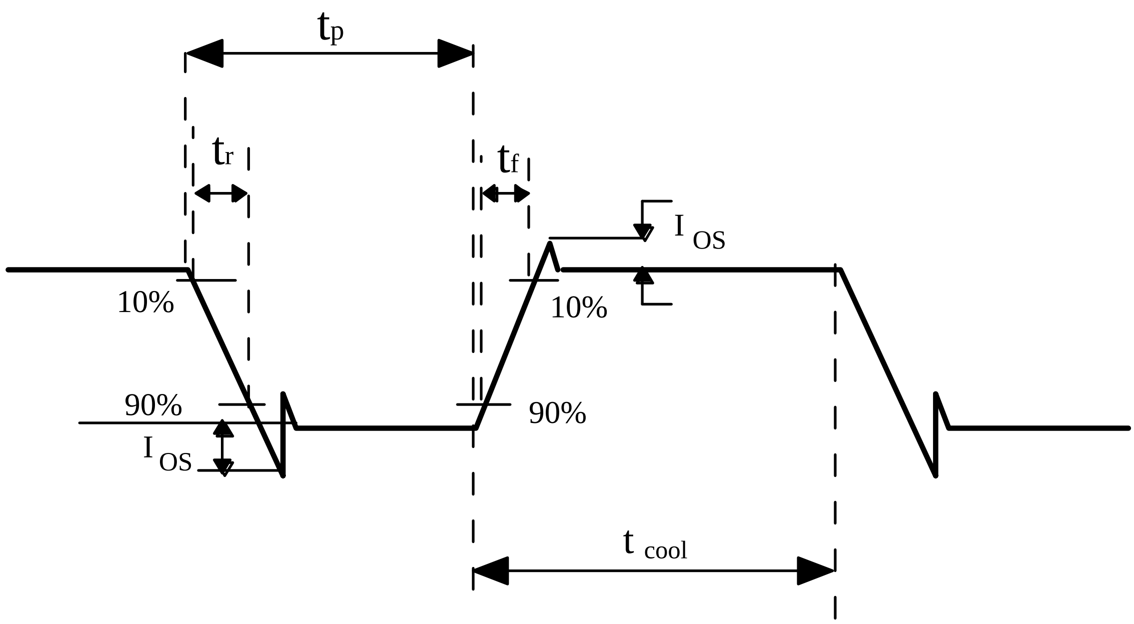


Figure 5　Waveform of Trigger Pulse Current (Negative Current)

Remark: **Figure 4** and **Figure 5** define a portion of the pulse parameters (t_r, t_f, t_p, I_{os}, t_{cool}) that are described in **Figure 1**, **Figure 2**, and **Figure 3**. Electrical characteristics of the parameters shall be compliant with **Table 1** requirements.

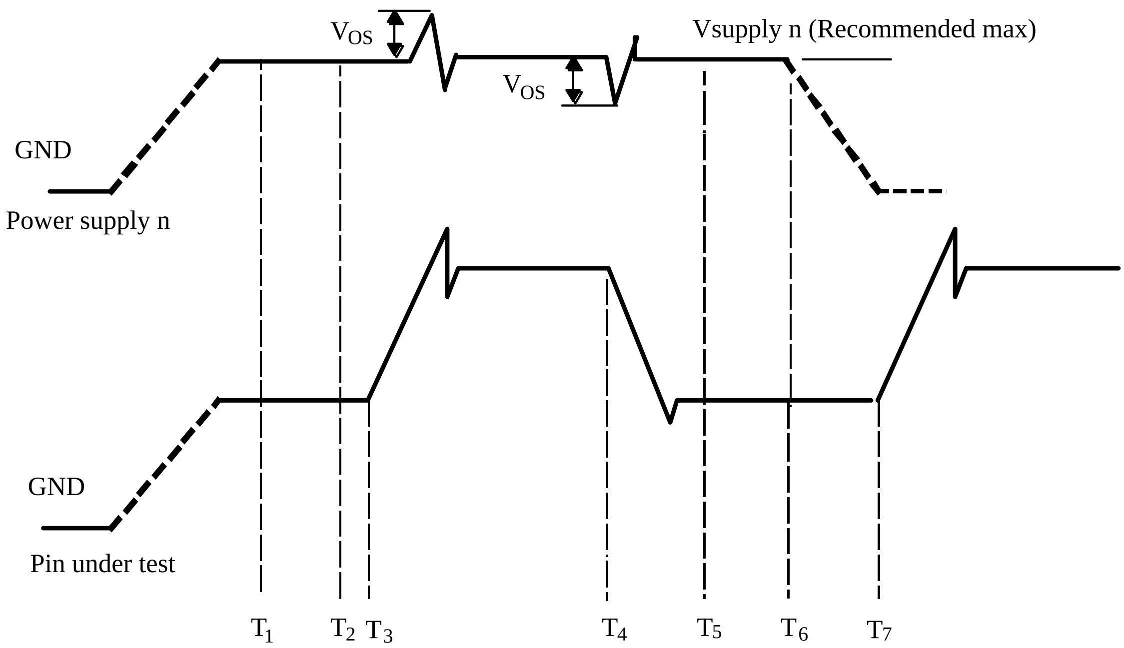


Figure 6 Measurement timing definitions and voltage waveforms of power supply and a pin under test (Positive Current)

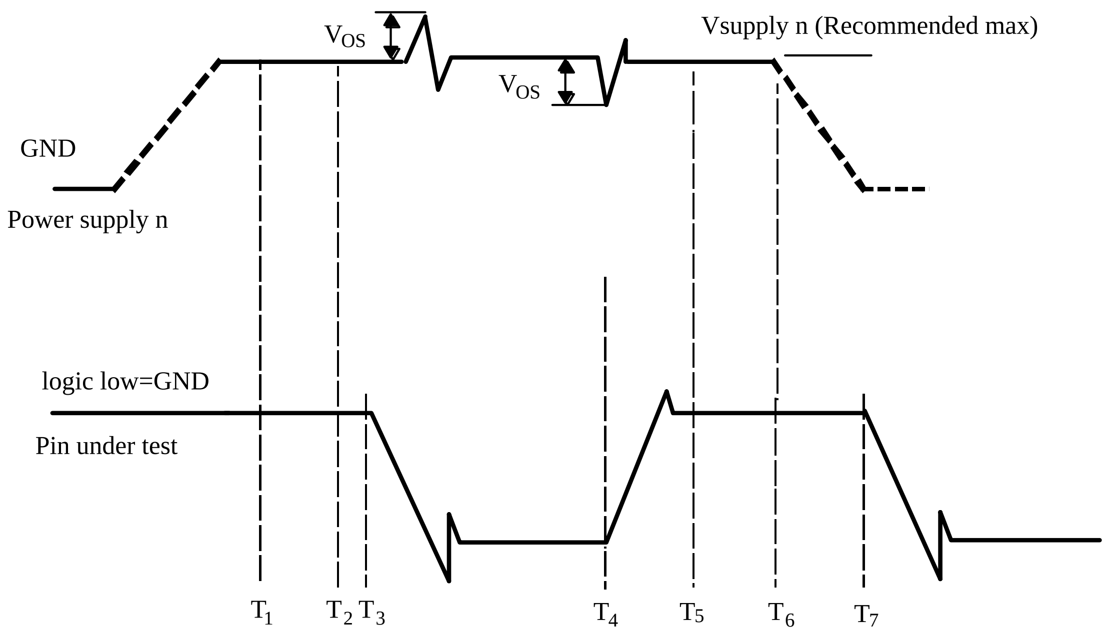


Figure 7 Measurement timing definitions and voltage waveforms of power supply and a pin under test (Negative Current)

Remarks:

1. **Figure 6** and **Figure 7** show the measurement timings that are defined in **Remark 2**. As for $V_{os,}$ its calibration shall be made using the test circuit as shown in **Figure 8**.

2. The timings between T_1 and T_7 shall be defined as follows.

Time	Operation
$T_1 \rightarrow T_2$	measure I_{supply} as I_{nom}
$T_4 \rightarrow T_7$	Cool down time (t_{cool})
$T_4 \rightarrow T_5$	Wait time prior to I_{supply} measurement
T_5	Measure I_{supply}
T_6	If any I_{supply} > failure criteria defined in **4.1.4**, latch up has occurred and power supply must be removed from DUT.

Table 1 Trigger pulse electrical characteristics

Parameter	Symbol	Figure	Timing	Limits		Unit	Remarks
				min.	max.		
Pulse width	t_p	1, 4, 5		2X t_r	10	ms	
Rise time	t_r	1, 4, 5		0.005	2	ms	(10-90%)
Fall time	t_f	1, 4, 5		0.005	2	ms	(90-10%)
Measure I_{nom}	t_w	6, 7	$T_1 \rightarrow T_2$	0.05	5	s	
Cool down time	t_{cool}	1, 4, 5	$T_4 \rightarrow T_7$	t_p		s	If repetitive
Wait time to measure I_{nom}		6, 7	$T_4 \rightarrow T_5$	0.003	5	s	
Power shut down		6, 7	T_6				
Measure strobe point	t_{stb}	6, 7	T_5			s	
Trigger pulse overshoot	I_{os}	1, 4, 5		5% of I_{trg} or less			
Trigger pulse accuracy	I_{trg}	1, 4, 5		Value specified ± 5%			
Power supply bounce	V_{os}	6, 7, 8		Value specified ± 5%			*1
Clamp voltage	V_{cl}	1		Value specified ± 5%			

Note *1: t_r and t_f shall be so controlled as to minimize power line bounce (V_{os}), by referring to the test circuit in **Figure 8**.

4.1.4 Procedures to apply trigger pulses

(1) Apply power supplies and pulse generator to a DUT as shown in **Figure 2** and **Figure 3**. The applied voltages should be the maximum recommended supply voltages according to the individual specification. The current limit of the power source should be more than a reference current for the latch up judgment but less than the breakdown current which causes permanent damage on the DUT.

(2) Set all of the input pins (including timing-related pins) to the appropriate bias conditions which make I_{nom} stable, referring to **4.1.1**. In case a DUT has dynamic node, clock pulse is applied to the timing pins. Only one logical combination is enough for the testing of the latch up with the exception of logic state sensitive case. For the logic states “L”, “H” which are mentioned here, are GND and power supply, respectively. In case the DUT requires multiple supply voltages, $I_{supply}n$ shall be measured for each supply pin independently prior to the test, and the value measured is regarded as $I_{nom}n$. The terminals with identical potential supplied can share the same power supply. Ambient temperature during the test is room temperature (25 deg C ± 5 deg C), unless otherwise specified. High temperature test will be done if individual specification requires.

(3) Supply a specified trigger pulse current to the test pin of the DUT. The number of trigger pulse applied is once. The polarity of the pulse shall be set positive or negative, not both in one sequence of the test on the pin. It should be noted that the test should be stopped immediately after the voltage of the pulse reaches clamp voltage (V_{cl}). As for the clamp voltage, refer to **4.1.6**.

Remarks:

1. Recommended trigger pulse current is I_{nom} + 100mA.
2. Trigger pulse width shall be set as narrow as possible in order to avoid the effect of heating up of the DUT.
3. As for latch-up failure criteria, refer to **5. Common notes for Test method I and Test method II**.

(4) After the trigger source has been removed, return the pin under test to the state it was in before the application of the trigger pulse, and measure the I_{supply} n for each power supply pin. If latch-up has occurred or if the DUT has been damaged or destroyed, stop the test. Replacing the DUT, return to step **(1)**.

Remarks:

1. Care must be taken to ensure that extra noise will not be introduced to the pin under test when returning it to the state it was in before the application of the trigger pulse.
2. Even if the I_{supply} is greater than or equal to the failure criteria, it is necessary to determine whether the measured I_{supply} is a true indication of latch-up, as described in **4.1.6** and **5**.

(5) If latch-up has not occurred, after the necessary cool-down time (t_{cool}), repeat steps **(3)** and **(4)** for the next pin to be tested. Alternatively, stress on the pin may be increased until latch-up occurs or until a predefined maximum trigger pulse current level is reached.

(6) Repeat steps **(2)** to **(5)** for all pins to be tested (except power and ground pins). Pins to be tested include I/O pins, Hi-Z pins, timing-related pins and analog pins. If specified, some particular pins may be excluded from latch-up testing.

(7) Change the polarity of the trigger pulse, and repeat steps **(1)** to **(6)**.

4.1.5 Final measurement

Perform the final measurement according to items and conditions specified in the DUT individual specifications. Check whether the DUT is defective or not, if necessary.

4.1.6 Notices of pulse current injection method

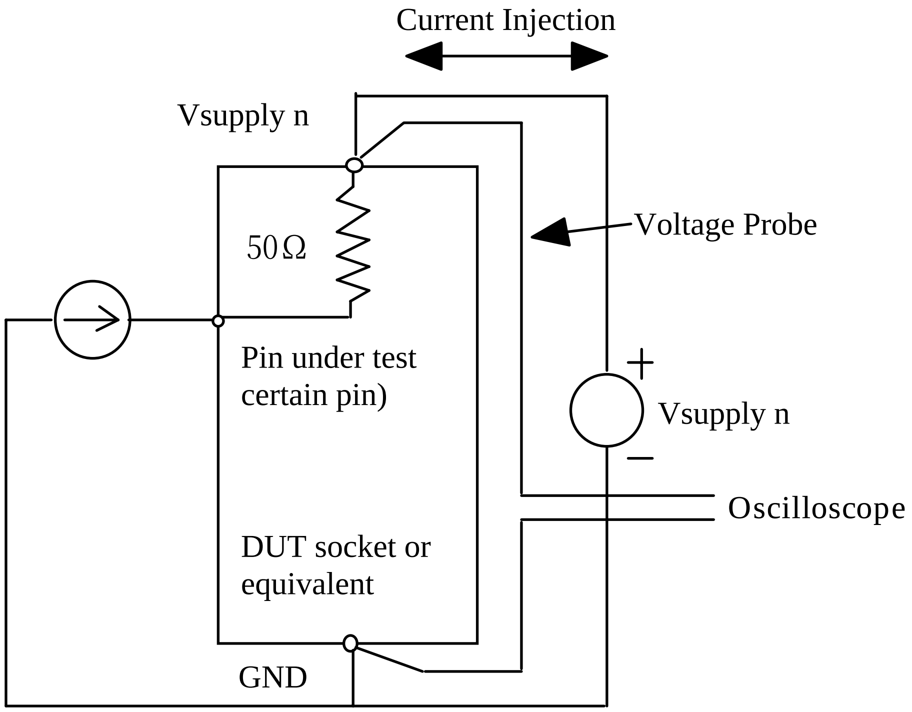
(1) Clamp voltage for constant-current pulses

The voltage should be clamped at 1.5 × | V_{supply} | for positive trigger pulses and at 0.5 × | V_{supply} | for negative trigger pulses. If the pin under test has high input impedance, even a small trigger pulse will cause a quite high potential to be induced on the pin. This could have an undesirable impact on test results. Therefore, the key to correct latch-up testing is to know how the clamp voltage affects test results. High current will not flow in normal use condition into the pin whose input impedance is too high to inject prescribed trigger pulse current to the pin.

(2) Trigger rise and fall times

When a trigger pulse is applied to the pin under test, a part of the trigger current might be superimposed on the voltage supply (V_{supply}), causing overshoot (V_{os} in **Figure 6** and **Figure 7**). The V_{supply} overshoot (V_{os}) must be reduced to within (10% of the specified supply voltage by adjusting the rise time of the trigger pulse. V_{os}, which can be evaluated by the circuit shown in **Figure 8**, can generally be reduced by increasing the rise time.

(3) In case an input pin is tested, just before the pin is connected to trigger current source the pin might be in a floating state for a certain period, which may cause the DUT to be unstable and to oscillate. In that case, the input pin being tested can be tied up to V_{supply} or tied down to GND via resistors to suppress oscillation. The resistance of the resistors should be so selected as to have no effect on the trigger pulse current.



Note 1. Load 50Ω ± 10%

Note 2. Probe impedance ≧ 10kΩ

Figure 8 Method for Evaluating the Impact of Reverse Trigger Current (V_{os}) on the Supply Voltage

4.1.7 Items to be specified in the DUT individual specification (for Method I)

(1)	Testing method	(Refer to **4.**)
(2)	Sample size	(Refer to **4.1**)
(3)	Preprocessing (if necessary)	(Refer to **4.1.1**)
(4)	Items and conditions of initial measurement	(Refer to **4.1.2**)
(5)	Supply voltage (when not specified in the standard)	(Refer to **4.1.3**)
(6)	Supply current limit	(Refer to **4.1.4**)
(7)	Latch-up failure criteria (current)	(Refer to **4.1.4**)
(8)	Ambient temperature (when not specified in the standard)	(Refer to **4.1.4**)
(9)	Handling of input and output pins except for test pins	(Refer to **4.1.4**)
(10)	Pins to be tested (when not specified in the standard)	(Refer to **4.1.4**)
(11)	Number of trigger pulses (when not specified in the standard)	(Refer to **4.1.4**)
(12)	Polarity of trigger pulse	(Refer to **4.1.4**)
(13)	Trigger pulse current	(Refer to **4.1.4**)
(14)	Clamp voltage (when not specified in the standard)	(Refer to **4.1.4**)
(15)	Current sense resistor (when not specified in the standard)	(Refer to **5.**)
(16)	Final measurement (if necessary)	(Refer to **4.1.5**)

4.2 Test method II (Supply overvoltage)

This method is used to evaluate the latch-up immunity against transient extremely high voltage onto the power pin of the biased semiconductor device. The sample size of the test is determined by the DUT individual specification.

4.2.1 Preprocessing

Refer to **4.1.1.**

4.2.2 Initial measurement

Should be performed according to items and conditions specified in the DUT individual specification. I_{nom} should be measured.

4.2.3 Test circuit and electrical characteristics

Figure 9 shows the test circuit for the Test method II. Its electrical characteristics to be satisfied are shown in **Table 2** and **Figure 9**, and the measurement timings to be satisfied are shown in **Table 2** and **Figure 10**.

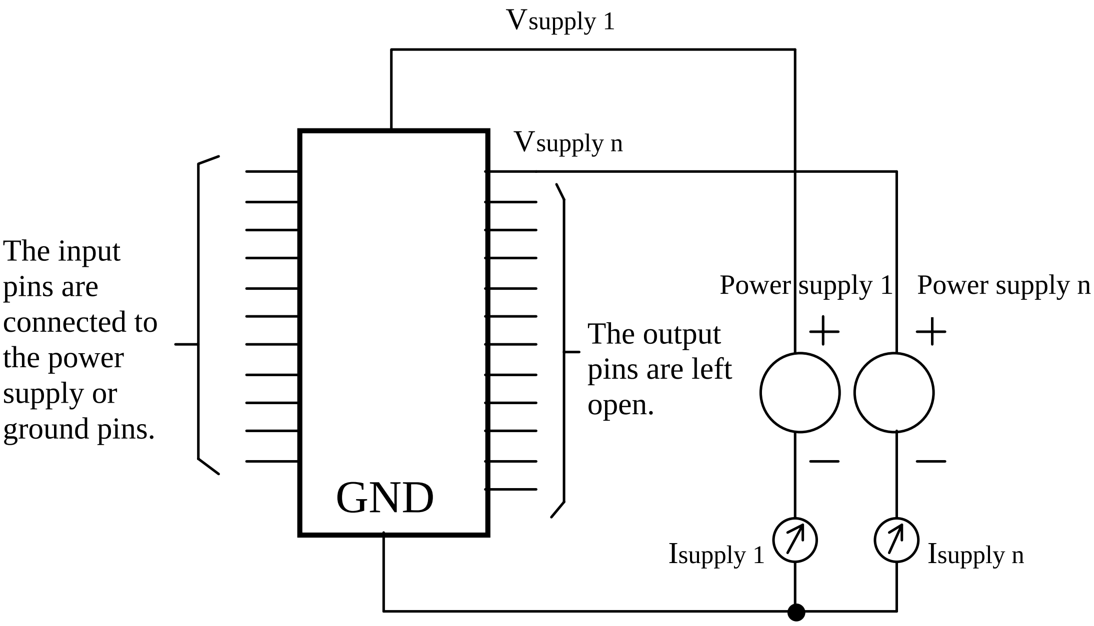


Figure 9 Test Circuit for Method II

Table 2 Electrical Characteristics of Trigger Pulse Current

Parameter	Symbol	Timing	Limits min.	Limits max.	Unit	Remarks
Pulse width	t_p	$T_3 \rightarrow T_4$	$2 \times t_r$	5	s	
Rise time	t_r		0.005	5	ms	(10%-90%)
Fall time	t_f		0.005	5	ms	(90%-10%)
Waiting time	t_w	$T_1 \rightarrow T_2$	*1			
Holding time	T_{cool}	$T_4 \rightarrow T_7$	t_p		s	
Power shut down		T_6				
Position of supply current measuring strobe	t_{stb}	T_5	0.003	5	s	
Overshoot	V_{os}		5% of V_{trig} or less			
Accuracy of trigger pulse current	V_{trg}		Value specified ± 5%			

Note *1: Time waiting for the device to be in the specified logic state, if needed, should be specified in the DUT individual specification.

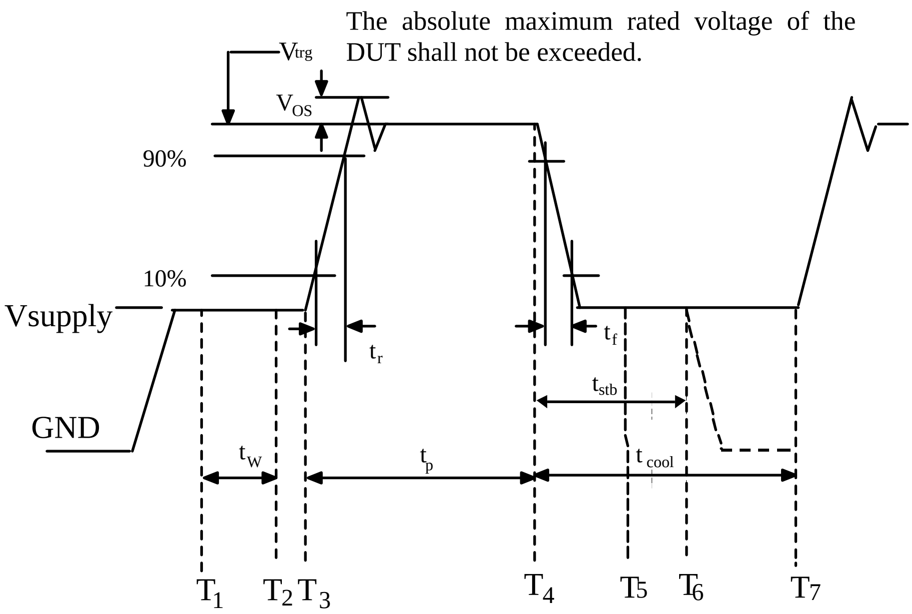


Figure 10 Trigger Pulse Voltage Waveform

Remarks: The timings between T_1 and T_7 shall be defined as follows.

Time	Operation
$T_1 \rightarrow T_2$	Measure I_{supply} as I_{nom}. Wait time (t_w).
$T_3 \rightarrow T_4$	Pulse width
$T_4 \rightarrow T_7$	Cool-down time (t_{cool})
$T_4 \rightarrow T_5$	Wait time before measuring I_{supply}
T_5	Measure I_{supply} (t_{stb})
T_6	Remove V_{supply} if $I_{supply} \geq$ failure criteria (t_{off})

4.2.4 Procedures to apply trigger pulses

(1) Apply a supply voltage V_{supply} to the DUT. The supply voltage should be the maximum recommended supply voltage specified in the DUT specification. The current limit of the power source should be more than a latch-up failure criteria but less than the breakdown current which causes permanent damage on the DUT. The ambient temperature during testing should be 25°C ± 5°C, unless otherwise specified.

(2) Set all of the input pins (including timing-related pins) to the appropriate bias conditions which make I_{nom} stable, referring to **4.2.1**. In case a DUT has dynamic node, clock pulse is applied to the timing pins. Only one logical combination is enough for the testing of the latch up with the exception of logic state sensitive case. For the logic states “L”, “H” which are mentioned here, are GND and power supply, respectively. In case the DUT requires multiple supply voltages, I_{supply} n shall be measured for each supply pin independently prior to the test, and the value measured is regarded as I_{nom} n. The terminals with identical potential supplied can share the same power supply. Increase the voltage of the trigger source up to the trigger pulse voltage (V_{trg}) relative to GND. Apply the trigger pulse once (and only once) unless otherwise specified. The trigger pulse voltage should not exceed the absolute maximum rating of the DUT.

(3) As specified in **4.2.3**, after the application of the trigger pulse voltage, decrease the supply voltage to the maximum recommended operating voltage. Wait for the DUT to stabilize and measure the supply current (I_{supply}) of the DUT at the strobe point of t_{STB}. If the measured supply current I_{supply} is greater than the latch-up failure criteria specified in the DUT individual specification or the failure criteria specified in **5. (1)**, it is judged that latch-up has occurred at the applied trigger pulse voltage. The power supply must be shut down immediately. If the measured supply current I_{supply} is under the latch-up failure criteria, go on to the next step of the latch-up test. In this case, wait until the DUT is fully cooled, then restart the latch-up test from the test timing T_1.

Remarks: In case the DUT has two or more power supply pins, apply the specified voltage to all of the power supply pins, then apply trigger pulses to each power supply pin.

4.2.5 Final measurement

Perform the final measurement according to items and conditions specified in the DUT individual specification.

Remark: Check whether the DUT is defective or not, if necessary.

4.2.6 Items to be specified in the DUT individual specification (for Method II)

(1)	Testing method	(Refer to **4.**)
(2)	Sample size	(Refer to **4.2**)
(3)	Preprocessing (if necessary)	(Refer to **4.2.1**)
(4)	Items and conditions of initial measurement	(Refer to **4.2.2**)
(5)	Waiting time	(Refer to **4.2.3**)
(6)	Supply voltage (when not specified in the standard)	(Refer to **4.2.4**)
(7)	Supply current limit	(Refer to **4.2.4**)
(8)	Temperature (when not specified in the standard)	(Refer to **4.2.4**)
(9)	Handling of input and output pins	(Refer to **4.2.4**)
(10)	Number of trigger pulses (when not specified in the standard)	(Refer to **4.2.4**)
(**11)**	Absolute maximum ratings	(Refer to **4.2.4**)
(12)	Trigger pulse voltage value (when not specified in the standard)	(Refer to **4.2.4**)
(13)	Current detecting resistor (Other than a recommended value)	(Refer to **5.**)
(14)	Reference current value for latch-up judgment	(Refer to **4.2.4**)
(15)	Final measurement (if necessary)	(Refer to **4.2.5**)

5. Common notes for Test method I and Test method II

(1) The latch-up failure criterion is defined as a change in I_{nom} by measuring I_{supply}, which is specified in the individual specification. If there is no specification in the individual specification, the failure criterion is defined as either $I_{nom} \times 1.4$ or $I_{nom} + 10mA$, whichever is greater.

(2) Measure the I_{supply} by using an ammeter with internal resistance of 1Ω or less, or by measuring the potential difference between the ends of a resistor of 1Ω or less.

(3) The wiring parasitic capacitance between the DUT and the test apparatus should be as small as possible to have no effect on the voltage pulse waveform and the current pulse waveform applied to the DUT.

(4) The current threshold, which causes latch-up, varies according to the temperature of the DUT. Therefore, the temperature of the DUT should be kept as constant as possible.

(5) As the latch-up test forcibly applies high electric stress to the DUT, the DUT is sometimes damaged by the electric overstress (EOS) and supply current may dramatically increase. In this case, it seems that latch-up occurs, but substantially it is due to the destruction of the DUT. Identify the phenomenon carefully. Data should be recorded when the DUT is damaged due to EOS (even if latch-up doesn’t occur).

(6) In some cases, when latch-up occurs, a large current flows between the power supply and the ground (GND), burns out power lines in the DUT, and consequentially open the circuit between the power supply and the ground (GND). In such case, no more supply current flows and it looks that latch-up will never occur in the succeeding test of the DUT. Identify the phenomenon carefully.

(7) The supply current limit should be such that it will not break the DUT when latch-up occurs. While, if the preset supply current value is equal to or less than the latch-up retaining current, latch-up will never occur even when trigger pulses are applied. Therefore, set carefully the supply current limit, fully considering the characteristics of the DUT.

(8) A sample which is subjected to a test can be applicable to the next test sequence (in case it passed the final test), but it should be noted that the latch-up test is basically destructive.

REFERENCE 1.
SUPPLEMENTARY MATTERS RELATED TO THE TEST METHODS

1. PERPOSE OF THE ESTABLISHMENT

This document of the testing method is a revised version of the **EIAJ ED-4701/306**, established in August 2001. The August 2001 version of the **EIAJ ED-4701/306** is, however, essentially the same as the June 1994 version of the **EIAJ ED-4701-1**, and in between those two periods, no thorough discussion had been made on how to latch-up test the device until 2001-2002 term. **The section 2**, below, summarizes in a time sequence how the discussion has been made on the latch-up testing method since August 2001.

2. PROCESS OF DELIBERATION

At the time of revision of the **ED-4701**, August 2001, focusing on the regrouping of the individual specifications, no thorough discussion had been made on latch-up testing method, and August 2001 version of the latch-up testing method took over the June 1994 version with no essential alterations. While, as to international standards, **JEDEC Standard No.17** was revised to **JEDEC Standard No.78** (March, 1997). **IEC** is studying the standardization based on **IEC/PAS 62181** (July, 2000) and is coming closer to the final stage, FDIS documentation from CDV as per **IEC 60749-29**.

Based on this background, August 2001 version of the specification emphasized, in the "**REFERENCE-1, Section-4. PROBLEMS TO BE SOLVED**", that the **JEITA** should review the specification and revise it appropriately with a sense of urgency. Semiconductor Reliability Subcommittee took the latch-up testing method as one of the 2002 main subjects, and made a thorough discussion. How the discussion has been made is described in a time sequence, below.

December 2001

The latch-up testing method was selected for one of the 2002 main subjects at No.41 Reliability Subcommittee.

April-May, 2002

The questionnaire-based survey was conducted on practical aspects of the latch-up testing method, on all subcommittee members.

August 2002

The first draft of the revision of the latch-up testing method was presented and deliberated, focusing on changes in the document.

September 2002

JEITA presented and explained the highlights of the revised (draft) version of the **JEITA** spec, comparing with **JEDEC Standard No.78**.

August to December 2002

To generate the revised version of the latch-up testing method specification, the base experimental data were assembled, such as, in I-test, the supply voltage level stability right after the current injection into IO , or the current pulse overshoot phenomenon in case the pulse is clamped.

December 2002

The draft version of the revision was issued and distributed to all Subcommittee members for review.

3. SUMMARY OF THE RESPONSES TO THE LATCH-UP QUESTIONNAIRES

In the following are summarized the responses from 11 companies to the latch-up questionnaires, which were taken April through May 2002.

(1) The reference pin settings for the current supply source in I-test

JEITA August 2001 version specifies the V_{supply} (VCC) terminal as a reference terminal in the positive pulse injection case in order to prevent the injected current from sinking into the V_{supply} source, but it doesn't take into account the devices with multiple power supplies, and doesn't mention how to test them. While, **EIA/JEDEC Standard No.78** allows the injected current sinking into the V_{supply} source and specifies the Ground (GND) terminal as a reference terminal in both positive and negative pulse injection cases.

Which specification does your company comply with in the reference pin setting ?

JEITA	6 companies
JEDEC/IEC	3 companies
Both	2 compnnies

Many supported **JEITA** method, but in the following question;

Which specification does your company think that it SHOULD comply with in the reference pin setting ?

JEITA	5 companies
JEDEC/IEC	4 companies
No answer	2 compnnies

As shown above, the voting result was almost half-and-half.

(2) Implementation status for V_{supply} overvoltage test

Already implemented	9 companies
NOT implemented yet	2 companies

Almost all voting companies have already implemented V_{supply} overvoltage test, but the testing procedure details are much different among them. Considering the individual device specification and the limitation of the test equipment, they determine for themselves the setting of the input pin logic levels and the power-up sequence for the device, which needs multiple power supplies.

In addition, more than half companies are thinking that the maximum overvoltage to which latch-up free is guaranteed is the absolute maximum supply voltage specified in the device specification (as per August 2001, **JEITA** specification). While, there are two companies which are following **EIA/JEDEC** compliant 1.5 × max. V_{supply} specification.

(3) Waveform monitor

Although there is only one company, which measures the trigger pulse waveforms at every test, seven companies are measuring the waveforms at a certain period, such as an annual calibration time.

(4) Clamp voltage setting

As to the device with multiple power supplies, more than half companies set the level of the clamp voltage for each pin, taking into account which power network the pin belongs to. The setting level of the clamp voltage is differently determined on a company-to-company basis.

(5) Logic state of the device during latch-up test

Before and after the stimulus input(current or voltage pulse input), is the logic state of output pins checked ?

Check	1 company
No check	10 companies

Does your company think no problem as long as the static current of the DUT is small enough and stable, irrespective of the logic state of output pins ?

Do not need to care about the logic state	7 companies
Should care about the logic state	3 companies
No answer	1 company

Thus, most companies do not care about the logic state of output pins because of the limitation of the test equipment capability and the thought that the internal logic state has little effect on the latch-up immunity.

(6) Input voltage level (Logic level of input pins)

In **EIA/JEDEC**, all input pins shall be tied to the maximum logic-high level or minimum logic-low level, which is specified in the device specification. In normal device specification, it is often seen that ;

Maximum logic-high level = VCC (supply voltage) + 0.3V

Minimum logic-low level = GND (ground voltage) - 0.3V

In the testing, does your company strictly follow the spec of VCC + 0.3V and GND - 0.3V for logic-high and logic-low, respectively ?

Follow VCC + 0.3V/GND - 0.3V	None
Do not follow VCC + 0.3V/GND - 0.3V	10 companies
No answer	1 company

None considers +/- 0.3V is necessary. Almost all companies think that VCC or GND is enough for logic-high or logic-low, respectively, as to input logic level in the testing.

REFERENCE 2.

SUPPLEMENTAL MATTERS RELATED TO PULSE CURRENT INJECTION METHOD

1. CONSTANT CURRENT PULSE SOURCE

A constant-current source is an ideal element, which is capable of keeping the current constant, whatever kind of circuit load is connected between the ends of the element. The voltage between the ends of the current source is determined by the circuit load. A current source in actual, however, has somewhat different behavior from idealistic operation, and therefore, it is important to know an unidealistic behavior of the source such as voltage fluctuation right after the current pulse injection, overshoot or undershoot.

2. CLAMPING VOLTAGE

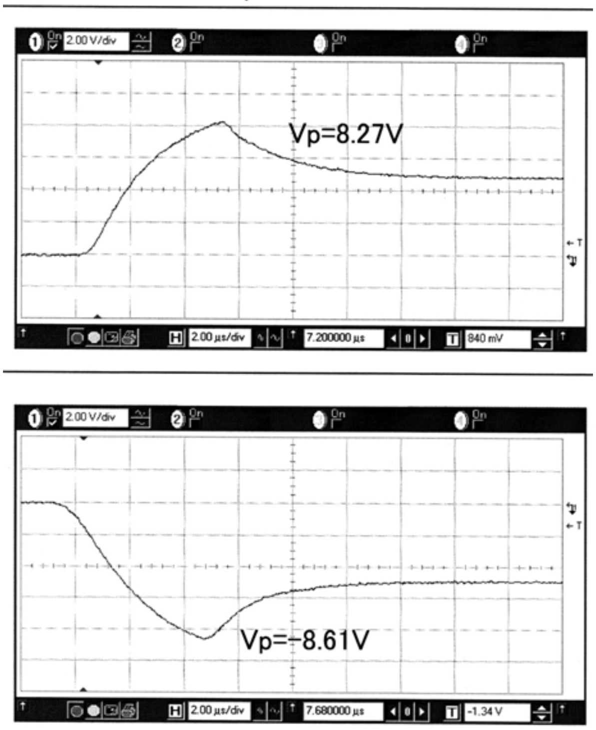
A constant-current source has a function of clamping voltage, which specifies the upper limit of voltage supplied to the pin. Some test equipment is capable of high voltage setting of the clamping voltage such as 100V. If 100V is directly supplied to the DUT, even instantly, the DUT is mostly broken. Therefore care must be taken for the clamping voltage setting, which should not be so high as to break down the high impedance pin of the DUT. Tri-state I/O pin and the pin with polysilicon resistance in the protective circuits are some examples.

3. CLAMPING VOLTAGE AND OVERSHOOT

In case of measuring a pulse waveform by the test circuit specified in **Figure1**, some test equipments show anomaly high voltage that exceeds the clamping voltage as shown in **Appendix Figure1**. A constant-current source controls a voltage with feedback of its own output, so if the trigger pulse rises so fast that overshoot appears because the feedback circuit cannot follow. In such a case, slower rise and fall of the trigger pulse, within the range specified in **Table 1**, may suppress the overshoot.

T_r = 5μs is too fast to suppress the overshoot, in case of **Appendix Figure1**.

Ip=200mA



Measurement conditions ;

Vcl = 5.0V, RL = 50Ω

t_r = 5µs

Force Current = +200mA

Vcl = -5.0V, RL = 50Ω

t_r = 5µs

Force Current = -200mA

Appendix Figure 1 Rise Time (t_r) and Overshoot

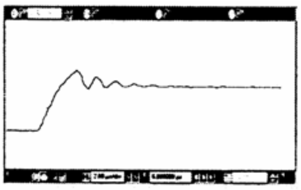
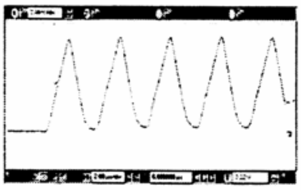
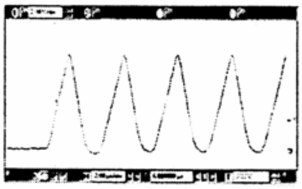
4. TANDARD LOAD FOR WAVEFORM MEASUREMENT

JEITA has been applying “50Ω” as a typical load for the calibration of the pulse since the first establishment. It has been discussed weather or not much larger resistance should also be used in the calibration. In conclusion,

(1) In terms of the verification of the linearity to the current applied, use of one resistance of 50Ω is enough.

(2) The lower resistance is more desired because of the stability of the waveform, otherwise the DUT shows an oscillation caused by the combination of the resistance, clamping voltage, and the rise-time. So the 50Ω is specified as usual.

In **Appendix Figure 2** and **3**, the examples of the waveforms are shown, when measured at t_r = 5μsec, or 50μs with load resistance (t_r) varied.

RL	Waveform
50Ω	
500Ω	
1kΩ	

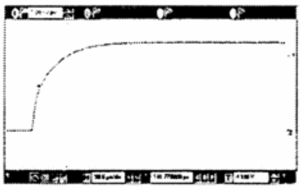
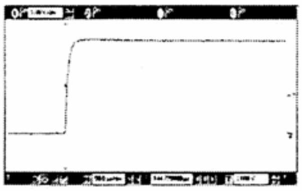
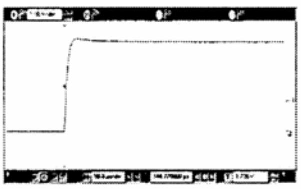
Measurement conditions ;

RL = 50Ω, 500Ω, 1kΩ

V_{c1} = 5.0V

As RL increases, trigger current waveform starts to oscillate and does not settle down.

Appendix Figure 2 Waveform for t_r = 5μs

RL	Waveform
50Ω	
500Ω	
1kΩ	

Measurement conditions ;

RL = 50Ω, 500Ω, 1kΩ

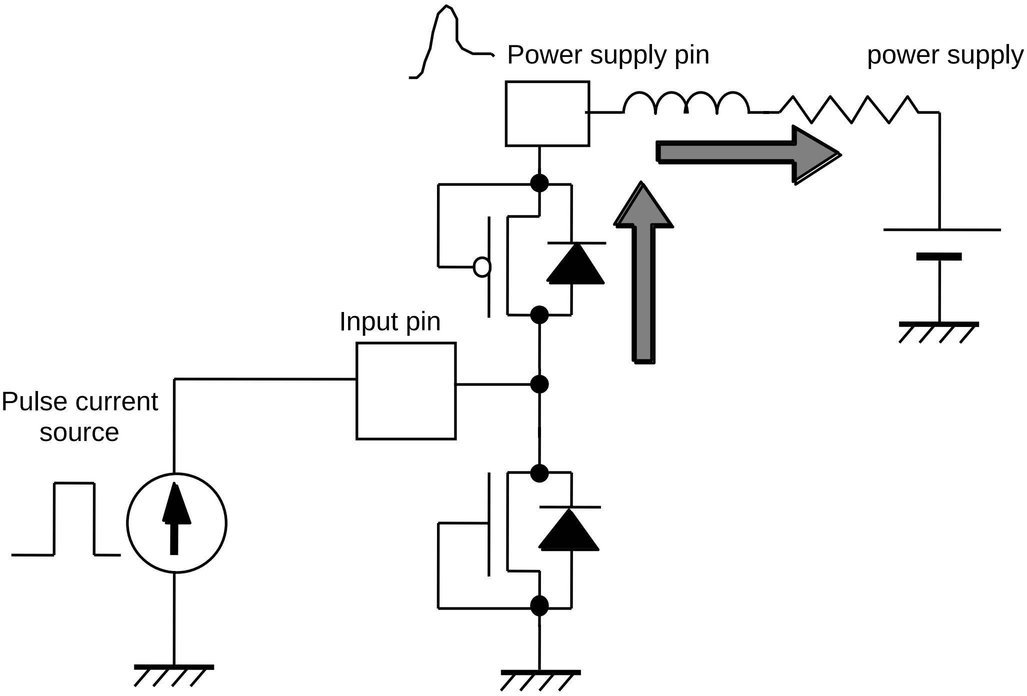
V_{c1} = 5.0V

Even if RL increases, trigger current waveform doesn't show any oscillation.

Appendix Figure 3 Waveform for t_r = 50μs

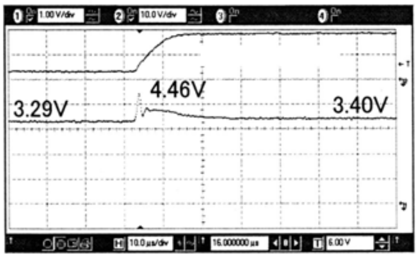
5. REVERSE CURRENT FLOW TO POWER SUPPLY

In this revision, a reverse current flow to the power supply is permitted, considering the DUT with multiple power supplies, but the output voltage of the power supply should be stable enough that the fluctuation, if any, must be suppressed within the specification as described in **Table 1**. The reverse current flow is explained in the **Appendix Figure 4**. Especially the fluctuation should not exceed the absolute maximum ratings.



Appendix Figure 4 A reverse current to the power supply

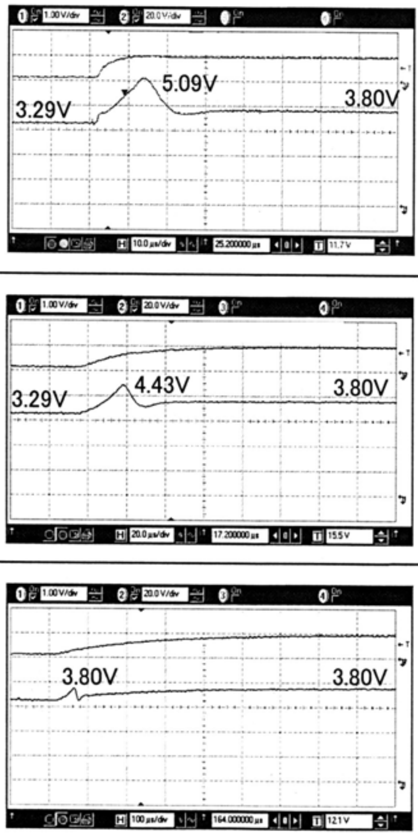
In **Appendix Figure 5** and **6**, the waveform observed by the measuring method in **Figure 8** is shown. In **Appendix Figure 5**, the data with the test equipment (t_r; 8μm fixed) made by Company A and in **Appendix Figure 6** the data with the test equipment (t_r; variable type) made by Company B are shown. In case t_r is short, the voltage of the power supply sometimes exceeds the absolute maximum ratings. Therefore it is desirable that t_r is as long as possible in order for the influence to the voltage of the power supply to be minimized.



Measurement circuit ; Refer to **Figure 8**
VCC = 3.3V
Waveform (upper): trigger pulse
(lower) : power supply

t_r = 8μs

Appendix Figure 5　VCC waveform by the test equipment from company A



Measurement circuit ; Refer to **Figure 8**
VCC = 3.3V
Waveform (upper): trigger pulse
(lower) : power supply

t_r = 5μs

t_r = 50μs

t_r = 500μs

Appendix Figure 6　VCC waveform by the test equipment from company B