JEITA

Standard of Japan Electronics and Information Technology Industries Association

EIAJ ED-4701/300

Environmental and endurance test methods for semiconductor devices

(Stress test I)

Established in August, 2001

Prepared by

Technical Standardization Committee on Semiconductor Devices

Published by

Japan Electronics and Information Technology Industries Association

11, Kanda Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan

Printed in Japan

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Standard of Japan Electronics and Information Technology Industries Association

Environmental and endurance test methods for semiconductor devices (Stress test I)

1. SCOPE

These standards provide for environmental test methods and endurance test methods (especially stress tests) aimed at evaluating the resistance and the endurance of integrated circuits (hereinafter generically called semiconductor devices) and discrete semiconductor devices used in electronic equipment mainly for general industrial applications and consumer applications, under the various environmental conditions of various kinds that occur during their use, storage and transportation.

2. DEFINITION OF TERMS

The definitions of the technical terms used in these standards and in the detail specifications are given in **EIAJ ED-4701/001** "Environmental and endurance test methods for semiconductor devices (General)."

3. PRECAUTIONS

The precautions used in these standards and in the detail specifications are given in **EIAJ ED-4701/001** "Environmental and endurance test methods for semiconductor devices (General)."

4. TEST METHODS

Refer to the Appendix for the test methods.

Remarks:

The various test methods are arranged independently for the sake of more convenient use of these standards.

COMMENTS

1. PURPOSE OF ESTABLISHMENT OF THESE STANDARDS

Before the establishment of these standards, the standardization referring to **EIAJ ED-4701** "Environmental and endurance test methods for semiconductor devices" established on Feb., 1992, and EIAJ has issued amendments, whenever the revision and also new test method establish. However, it is recondite where the latest test methods are entered, it was resulting the confusion of users. So establishment of new numbering system that is easy to use both users and manufacturers was decided, and reached to the issuance in this time.

Electronic Industries Association of Japan (EIAJ) and The Japan Electronic Industry Development Association (JEIDA) have merged effective November 1,2000, the Japan Electronics and Information Technology Industries Association (JEITA).

2. EVOLUTION OF THE DELIBERATIONS

The revision of the standards and new numbering system have been deliberated by "Sub-Committee on Semiconductor Devices Reliability" of the Technical Standardization Committee on Semiconductor Devices/Semiconductor Devices Reliability Group from Apr., 2000. Though to issue as a separate standard every each test method was considered, it made to issue with the system like the following.

(a) EIAJ ED-4701/001 Environmental and endurance test methods for semiconductor devices (General)

(b) EIAJ ED-4701/100 Environmental and endurance test methods for semiconductor devices (Life test I)

- **101** Steady state operating life
- **102** Temperature humidity bias (THB)
- **103** Temperature humidity storage
- **104** Moisture soaking and soldering heat stress series test
- **105** Temperature cycle
- **106** Intermittent operating life

(c) EIAJ ED-4701/200 Environmental and endurance test methods for semiconductor devices (Life test II)

- **201** High temperature storage
- **202** Low temperature storage
- **203** Moisture resistance (Cyclic)
- **204** Salt mist

(d) EIAJ ED-4701/300 Environmental and endurance test methods for semiconductor devices (Stress test I)

- **301** Resistance to soldering heat for surface mounting devices (SMD)
- **302** Resistance to soldering heat (excluding surface mounting devices)
- **303** Solderability
- **304** Human body model electrostatic discharge (HBM/ESD)

305 Charged device model electrostatic discharge (CDM/ESD)
306 Latch-up
307 Thermal shock

(e) EIAJ ED-4701/400 Environmental and endurance test methods for semiconductor devices (Stress test II)

401 Terminal strength
402 Mounting strength
403 Vibration (Sinusoidal)
404 Shock
405 Acceleration (Steady state)

(f) EIAJ ED-4701/500 Environmental and endurance test methods for semiconductor devices (Miscellaneous)

501 Permanence of marking
502 Flammability tests of plastic-encapsulated devices (Externally induced)
503 Seal
504 Low air pressure

Both life and stress tests are divided into two standards as "I" and "II". "I" is including test method that is thought that revision occurs comparatively from now on.

3. DELIBERATING MEMBERS

Deliberation of this standard has been made by "Sub-Committee on Semiconductor Devices Reliability" of the Technical Standardization Committee on Semiconductor Devices/Semiconductor Devices Reliability Group.

Below are listed the members of deliberation of this standard.

<Technical Standardization Committee on Semiconductor Devices/Semiconductor Devices Reliability Group>

Chairman	Mitsutoshi Ito	NEC Corp.

<Semiconductor Devices Reliability Group>

Chairman	Kazutoshi Miyamoto	Mitsubishi Electric Corp.

<Sub-Committee on Semiconductor Devices Reliability>

Chairman	Tetsuaki Wada	Matsushita Electronics Co., Ltd.
Vice Chairman	Masaki Tanaka	Hitachi Ltd.
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	Takeshi Watanabe	NEC Corp.

APPENDIX

TEST METHOD 301
RESISTANCE TO SOLDERING HEAT SURFACE MOUNTING DEVICES (SMD)

1. SCOPE

This standard provides for the method to evaluate to soldering heat of SMD used in electronic equipment for consumer application and industrial application in general.

2. TEST EQUIPMENT

2.1 High temperature furnace

The high temperature furnace must be capable of keeping temperature specified in Sub-clause **4.2** for long time.

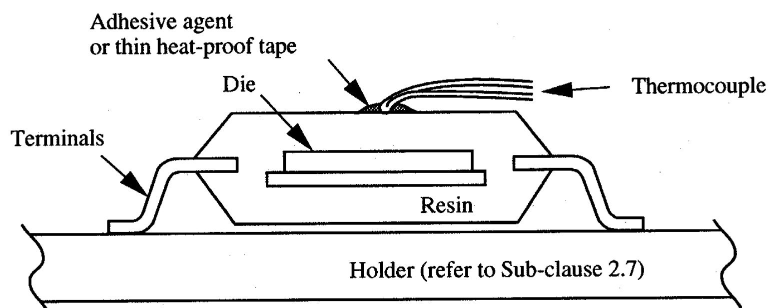
2.2 Moisture chamber

The moisture chamber must be capable of keeping temperature and relative humidity specified in Sub-clause **4.2** for long time. The material composing the chamber must not react under high humidity conditions. Water to be used in the tests must be distilled water or deionized water, with pH from 6.0 to 7.2 and resistivity of 500 Ωm or more at 23°C.

2.3 Infrared reflow soldering/Convection reflow soldering furnace

The infrared and the convection reflow soldering furnace must be capable to meet the temperature profile specified in Sub-clause **4.4(1)**. The temperature profile is specified in terms of the temperature of top surface of the specimen placed on the holder (refer to Sub-clause **2.7**). The temperature at the top surface of the specimen shall be measured as shown in **Figure 1**.

Figure 1 Method of measuring the temperature profile of a specimen



2.4 Vapor phase reflow soldering furnace

The vapor phase reflow soldering furnace must be capable to meet the temperature profile specified in Sub-clause **4.4(2)**. The temperature profile is specified in terms of the temperature of top surface of the specimen placed on the holder (refer to Sub-clause **2.7**). The temperature at the top surface of the specimen shall be measured as shown in **Figure 1**.

2.5 Wave soldering furnace

The wave soldering furnace must be capable of keeping temperature of molten solder during the solder heating specified in Sub-clause **4.4(3)**. The molten solder must always be flowed. The preheat conditions in Sub-clause **4.4(3)(b)** are specified in terms of the temperature at the top surface of the specimen as shown in **Figure 1**.

2.6 Solder bath

The solder bath should have capacity enough to keep the temperature of molten solder within the prescribed values even during the solder heating described in Sub-clause **4.4(4)**. The dipping equipment should be capable to control the dipping depth and the dipping time of the terminals in the molten solder as specified in Sub-clause **4.4(4)(c)**.

2.7 Holders

Unless otherwise specified, the material of the holder, which the specimen is to be placed on during the solder heating in the reflow soldering and the wave soldering furnace, should be made from glass-reinforced epoxy resin, polyimide, or alumina substrate

3. MATERIALS

3.1 Perfluorocarbon

Use Perfluorocarbon (perfluoroisobutyrene) or equivalent in vapor phase reflow soldering furnaces.

3.2 Solder

Solders to be used in this test should be those ones specified in H60A, H60S, H63A of **JIS Z 3282** (SOLDER) or in **APPENDIX B** of **JIS C 0050**.

3.3 Flux

Flux to be used in this test should be 2-propanol (**JIS K 8839**) or ethanol (ethyl alcohol, **JIS K 8101**) solution of rosin (**JIS K 5902**) (the concentration should be from 10% to 35% of rosin in terms of mass ratio, and 25% unless otherwise specified) or the material specified in **APPENDIX C** of **JIS C 0050**.

4. TEST PROCEDURE

4.1 Initial measurement

In accordance with the relevant specification, the electrical characteristics of the specimen shall be measured, and the visual inspection for cracks and the other defects of the specimen shall be made with the assistance of a magnifier capable of giving 40 magnifications. The initial appearance for cracks and delaminations of inside of the specimen shall be inspected using scanning acoustic tomography (SAT) if necessary. (refer to Sub-clause **4.6**)

4.2 Baking

Unless otherwise specified in the relevant specification, baking under conditions of 125±5°C for 24h or more shall be performed if moisture soaking specified in Sub-clause **4.3** will be performed.

4.3 Moisture soaking

Moisture soaking specified in **(1)** or **(2)** of this Sub-clause shall be performed if the specimen is type of resin encapsulated SMD. The baking treatment specified in the relevant specification shall be performed instead of the moisture soaking if the baking before real soldering of electronic assembly process is specified in the relevant specification. Unless otherwise specified in the relevant specification, the solder heating specified in Sub-clause **4.4** shall be started within 4h[Note 1] after finishing this moisture soaking.

Note 1:

Longer time than 4h can be specified in the relevant specification if the specimen is a thicker SMD

because it does not affect the moisture absorption and the drying.

(1) Moisture soaking for dry packed SMD

a) Baking not performed before dry packing

The first stage moisture soaking corresponded to the worst atmospheric condition for long storage of SMD in the dry pack (the worst case is 30°C, 30%RH) shall be performed, and subsequently, the second stage moisture soaking corresponded to the allowable maximum storage condition after opening the dry pack (Floor life) shall be started within 4h after finishing the first stage moisture soaking. The temperature tolerance must be ±2°C and the relative humidity tolerance must be ±5%.In case of moisture density of a package for one time soaking is more than the density of amount of the first and the second stage moisture soaking, the first stage moisture soaking can be omitted.(Note 2)

b) Baking performed before dry packing

In case of the worst atmospheric condition for long storage of SMD in the dry pack is guaranteed less than 30°C, 10%RH because of baking performed before dry packing, the first stage moisture soaking can be omitted.(Note 3)

Remark 1:

If 30°C,30%RH for 1 year in the dry pack is specified as the worst atmospheric condition, conditions of the first stage moisture soaking can be made by rising temperature from 30°C to 85°C as shown in **Table 1** because moisture soaking speed can be accelerated by rising temperature. **Table 1** shows performing the first stage moisture soaking at 85°C, 30%RH, for 168h(Note 4) and the second stage moisture soaking at 30°C, 70%RH, for 168h.(Note 5)

Note 2:

The moisture density means the density at boundary of a structural object (i.e. chip, die paddle etc.) and resin. The one time soaking is a substitute way of the first and the second stage moisture soaking, and the data of the first and the second stage moisture soaking precede the data of the one time soaking.

Note 3:

The baking before dry packing must perform both of SMD and IC-trays, because IC-trays are also absorbed moisture.

Note 4:

When the specimen is a thin SMD and the first stage moisture soaking reaches enough saturation, its soaking time should be shortened below 168h. On the other hand, when the specimen is a thick SMD and the first stage moisture soaking does not reach saturation, their soaking time shall be extended to over 168h.

Note 5:

Conditions of the second stage moisture soaking should be determined corresponding to storage conditions between opening dry pack and the final soldering process.

Table 1 Example of moisture soaking conditions for dry packed SMD

Item	Moisture soaking conditions	Expected storage conditions	Remarks
First stage moisture soaking (Moisture soaking corre-sponded to long storage in the dry pack)	85°C, 30%RH, 168h (perform until saturation of moisture absorption)	30°C, 30%RH, 1year (Worst atmospheric condition in the dry pack)	If expected storage conditions in the dry pack are different from this case, moisture soaking conditions shall be changed into suitable conditions. The first stage moisture soaking can be omitted when the atmosphere in the dry pack is less than 30°C, 10%RH.
Second stage moisture soaking (Moisture soaking corre-sponded to storage after opening the dry pack)	30°C, 70%RH, 168h	30°C, 70%RH, 168h	

(2) Conditions for non-dry packed SMD

The moisture soaking conditions shall be selected from **Table 2**(Note 6). Unless otherwise specified in the relevant specification, the soaking time of 168±24h should be selected for the condition A.(Note 7)(Note 8)

Remark 2:

Storage time for non-dry packed SMD can be assumed as 1 year as upper limit because of some reasons such as degrading solderability.

Note 6:

Condition A should be selected from **Table 2** when SMD is stored in room in Japan (Mean temperature and humidity are below 30°C, 70%RH). Condition B should be selected from **Table 2** when SMD is stored in atmosphere of higher humidity (Mean temperature and humidity are below 30°C, 85%RH). When condition A is selected and the average temperature and humidity exceeds 30°C, 70%RH even if transportation period, SMD should be dry packed.

Note 7:

Unless otherwise specified in the relevant specification, the soaking time of condition A should be selected as 336h when the moisture soaking does not reach the saturation level as thick SMD.

Note 8:

When moisture soaking of below 168h can make saturation, soaking time of condition A and B can be shortened as within the saturated time as thin SMD.

Table 2 Moisture soaking conditions for non dry packed SMD

Condition code	Temperature (°C)	Relative humidity (%)	Soaking time (h)
A	85±2	65±5	168±24 or 336±24
B	85±2	85±5	168±24

4.4 Solder heating

In accordance with the relevant specification, solder heating method shall be selected from method I, II, III and IV in this Sub-clause. Unless otherwise specified, solder heating shall be performed twice. If another number of solder heating times may be required, the maximum repetition is 3 times and it shall be specified into the relevant specification. When second solder heating is performed, the specimen shall be cooled down below 50°C after the first solder heating. Unless otherwise specified, moisture soaking between the first and the second solder heating shall not be applied. If moisture soaking between the first and the second solder heating is applied, its conditions shall be specified in the relevant specification.

(1) Method I (infrared-convection or convection reflow soldering)

Solder heating by infrared-convection or convection reflow soldering shall be performed by the following procedures.

(a) Preparations

The specimen shall be put on the holder. Solder paste should not be applied on the holder.

(b) Preheat

The specimen shall be heated to a temperature between 140°C and 160°C for 90s±30s in the reflow soldering apparatus.

(c) Solder heating

Following the preheat, the specimen shall be continuously heated to the peak temperature, and subsequently the specimen shall be cooled down. Heating conditions shall be selected from **Table 3**. Unless otherwise specified, condition I-A of 235°C or more (but lower than 240°C) for 10s±3s shall be selected if volume of the specimen is below 2000mm^3, and subsequently temperature of the specimen shall be lowered to room temperature as shown in **Figure 2**. On the other hand, if the volume of specimen exceeds 2000mm^3, condition I-B of 220°C or more (but lower than 225°C) for 10s±3s should be selected, and subsequently temperature of the specimen shall be lowered to room temperatures. (Refer to **Figure 3**[(Note 9)]) If temperature of the SMD which reflects infrared rays is not raised, suitable conditions shall be specified in the relevant specification.

Note 9:

When many types of SMD which have different volumes are soldered on the same printed circuit board at the same time, the temperature of larger SMD whose volume is 2000mm3 or more rises slowly and their peak temperature do not reach 220°C because larger SMD have higher heat capacity.

Table 3 Heating conditions of the infrared reflow and the convection reflow soldering

Condition code	Temperature (°C)	Heating time (s)	Remarks
I-A	235^{+5}_{-0}	10±3	Peak temperature: 240°C or less (refer to **Figure 2**)
I-B	220^{+5}_{-0}	10±3	Peak temperature: 225°C or less (refer to **Figure 3**)

Figure 2 Temperature profile of infrared convection and convection reflow soldering (Condition I-A)

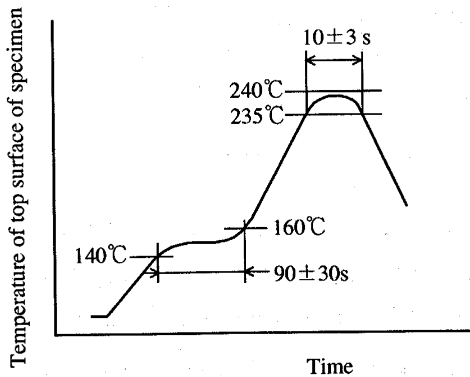
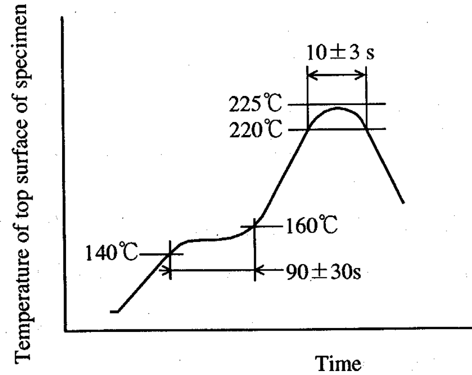


Figure 3 Temperature profile of infrared convection and convection reflow soldering (Condition I-B)



(2) Method II (Vapor phase reflow soldering)

When the specimens are heated by the vapor phase reflow soldering method, following procedure shall be applied. (Refer to **Table 4**, **Figure 4**)

(a) Preparations

The specimen shall be put on the holder. Solder paste should not be applied on the holder.

(b) Preheat

The specimen shall be heated to temperature from 140°C to 160°C for 90s±30s in the reflow soldering apparatus.

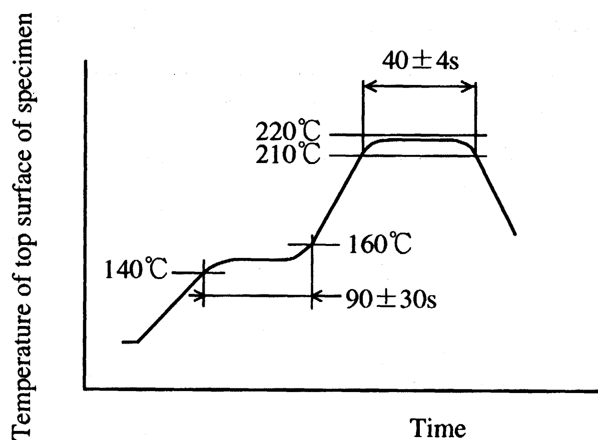
(c) Solder heating

Between 210°C and 220°C for 40s±4s as shown in **Table 4** and **Figure 4**, subsequently the specimen shall be cooled down.

Table 4 Heating conditions of the vapor phase soldering

Condition code	Heating temperature (°C)	Heating time (s)	Remarks
II-A	210	40±4	refer to **Figure 4**

Figure 4 Temperature profile of the vapor phase reflow soldering (Condition II-A)



(3) Method III (Wave soldering)

(a) Preparations

Bottom surface of the specimen shall be adhered to the holder by adhesive agent in accordance with the methods and conditions of the applying adhesive specified in the relevant specification. Unless otherwise specified in the relevant specification, flux shall not be applied to the holder and the specimen.(Note 10)

Note 10:

Inhibiting the latent heat of evaporation of the flux from rising the temperature of the specimen, the flux should not be applied to the body of the specimen even if applying the flux to the specimen is specified in the relevant specification. If applying the flux to terminals of the specimen, the amount of the flux should be a minimum.

(b) Preheat

The specimen adhered to the holder shall be heated to temperature between 80°C and 140°C for 30s to 60s in the wave soldering apparatus.

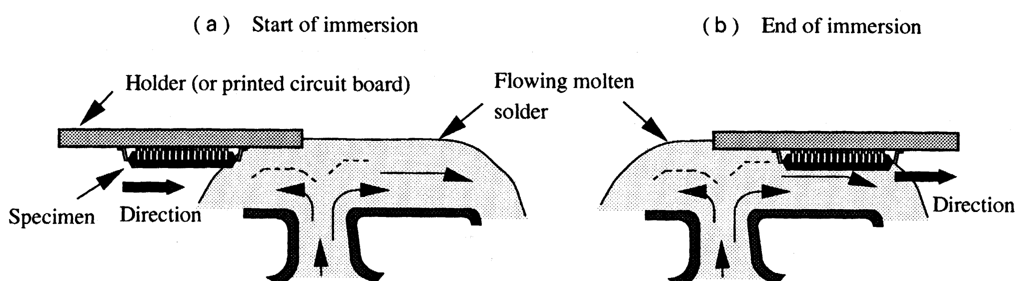
(c) Solder heating

After the preheat, the holder with the specimen shall be immersed into flowing molten solder as shown in **Figure 5(a)**, **(b)**. The immersion conditions shall be selected from **Table 5**, according to the real soldering process and conditions. The definition of the immersion time is from the part of the specimen starting immersion, as shown in **Figure 5(a)**, until the part of the specimen emerging from molten solder, as shown in **Figure 5(b)**. The package moving time to complete immersion into the molten solder or complete emergence from the molten solder shall be less than 2s.

Table 5 Heating conditions by the wave soldering

Condition code	Temperature of solder (°C)	Immersion time (s)	Remarks
III-A	260±5	5±1	for single wave
III-B	260±5	10±1	for double wave

Figure 5 Heating method by immersion using the wave soldering



(4) Method IV (Dip of terminals into molten solder)

This test method, dipping the terminals of the specimen in molten solder simulates heat by the soldering iron.

(a) Dipping into flux

Dip the terminals of the specimen into flux at room temperature.

(b) Cleaning the solder surface

Clean the surface of molten solder by scraping it with a spatula made of stainless steel and the like.

(c) Dipping into molten solder

Dip all terminals of the specimens, one side at a time, perpendicularly into the molten solder surface according to the conditions of **Table 6** (refer to **Figure 6**). The dipping depth should be up to the flat portion for solder joint or up to the effective soldering portion of the terminals. The moving speed for dipping and removing should be 25mm/s. The duration for movement should not be included in the dipping time.

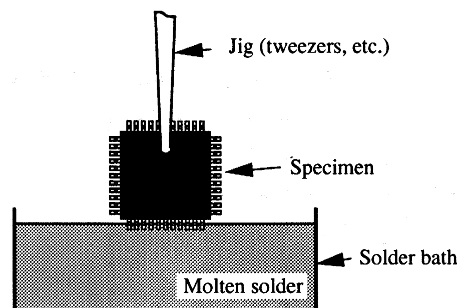
(d) Removing flux

Remove flux stuck on the specimens by washing it.

Table 6 Heating conditions for the dip of terminals into solder

Condition code	Temperature of solder (°C)	Dipping time (s)	Remarks
IV-A	350±10	3.5±0.5	

Figure 6 Method of the dip of terminals into solder



4.5 Recovery

If recovery is specified in the relevant specification, the specimen shall be stored under standard atmospheric conditions for the time given in the specification, after finishing the solder heating.

4.6 Final measurements

The specimen shall be judged by the results of electrical measurements, visual inspection of external cracks by 40X optical microscope, and internal cracks and/or delaminations by SAT according to the PASS/FAIL flow chart shown in **Figure 7**. The internal delaminations which come under Sub-clause **4.6.3** shall be judged by the results of the reliability test. A special package which can not apply to these test methods shall be judged by the relevant specification.

4.6.1 Electrical characteristic and visual inspection

A device is considered as a failure if it comes under any of the following:

(1) Electrical failure

(2) External cracks visible under 40X optical microscope

(3) Expansion and/or distortion of the package shape under visual inspection

Remark 3:

In the case that expansion and/or distortion of the package shape may cause assembly problems, it should be considered as a failure.

4.6.2 Inspection 1 by SAT

A specimen is considered as a failure if it comes under any of the following. If internal cracks are suspected based on SAT, polished cross sections shall be made to verify the suspected site.

(1) Internal cracks that intersect a bond wire, ball bond, or wedge bond.

(2) Internal cracks extending from any internal feature to any other internal feature (lead finger, chip, die attach paddle)

(3) Internal cracks extending more than two-thirds (2/3) the distance from any internal feature to the outside of the package.

4.6.3 Inspection 2 by SAT

A specimen is considered as good if it does not come under Sub-clause **4.6.2** and any of the following: A specimen shall be judged by the results of reliability test if it exhibits any of follows, except for delaminations on the back side of the die paddle or die (lead on chip etc.)

(1) Delaminations between the surface of die and the mold

(2) Delaminations of any other internal feature

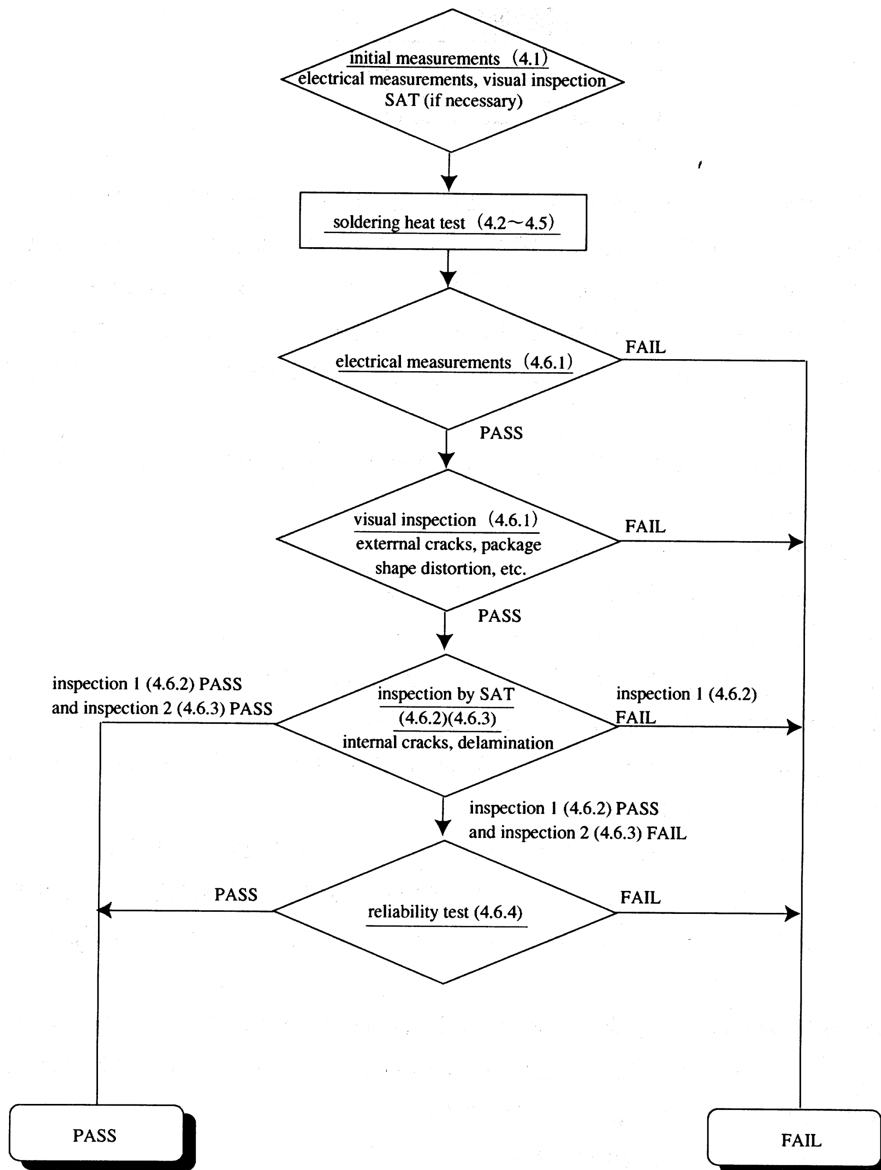
(3) Internal cracks which do not come under Sub-clause **4.6.2**.

4.6.4 Reliability test

The specimen shall be judged by the results of reliability test if it comes under item **4.6.3**.

Reliability test method referred to shall be Moisture soaking and soldering heat stress series test (test method **B-101**) and specified the relevant specification.

Figure 7 PASS/FAIL flow chart



5. STORAGE LIMIT FROM OPENING DRY PACK TO SOLDERING

The storage limit from opening dry pack to soldering classifies on 10 ranks. Baking before soldering is necessary if SMD stores over the storage limit.

In case of baking performed before dry packing, the floor life should be included the time from end of baking to dry packing, and baking before dry packing must perform both of SMD and a tray.

When rank S is used, moisture soaking condition, storage condition after unpacking and storage limit after unpacking should be specified in the relevant specification.

Table 7 Rank of resistance to soldering heat

Rank	Moisture soaking condition * the second stage moisture soaking	Storage condition after unpacking	Storage limit after unpacking
A	85°C, 85%RH, 168h	≤30°C, 85%RH	Unlimited
B	85°C, 65%RH, 168h	≤30°C, 70%RH	1 year
C	* 30°C, 70%RH, 672h(Note11)	≤30°C, 70%RH	4 weeks
D	* 30°C, 70%RH, 336h(Note11)	≤30°C, 70%RH	2 weeks
E	* 30°C, 70%RH, 168h(Note11)	≤30°C, 70%RH	168h
F	* 30°C, 70%RH, 96h(Note11)	≤30°C, 70%RH	96h
G	* 30°C, 70%RH, 72h(Note11)	≤30°C, 70%RH	72h
H	* 30°C, 70%RH, 48h(Note11)	≤30°C, 70%RH	48h
I	* 30°C, 70%RH, 24h(Note11)	≤30°C, 70%RH	24h
S	specified individually	specified individually	specified individually

Note 11:

Acceleration soaking such as 85°C, 65%RH may be used if moisture density under acceleration soaking condition is confirmed over the moisture density under 30°C, 70%RH condition. The simulation results may be used for confirmation.

6. INFORMATION TO BE GIVEN IN THE RELEVANT SPECIFICATION

(1) Holder (When it is different from the specified ones) [Refer to **2.7**]

(2) Composition of the solder (When it is different from the specified ones) [Refer to **3.2**]

(3) Mixing ratio of flux (When it is different from the specified ones) [Refer to **3.3**]

(4) Items and conditions of the initial measurements [Refer to **4.1**]

(5) Baking (When required) [Refer to **4.2**]

(6) Moisture soaking conditions (When it is different from the specified ones) [Refer to **4.3**]

(7) Time period between the moisture soaking and the solder heating (When it is different from the specified ones) [Refer to **4.3**]

(8) Allowable maximum conditions (temperature and relative humidity) in the dry pack and the first stage moisture soaking conditions corresponded to their conditions [Refer to **4.3(1)**]

(9) Storage conditions of SMD after opening the dry pack and the second stage moisture soaking conditions corresponded to their conditions [Refer to **4.3(1)**]

(10) Selection of moisture soaking conditions for non-dry packed SMD [Refer to **4.3(2)**]

(11) Moisture soaking time of condition A for non-dry packed SMD [Refer to **4.3(2)**]

(12) Moisture soaking time when moisture absorption is saturated less than 168h [Refer to **4.3(2)**]

(13) Baking treatment conditions instead of the moisture soaking (When it is necessary) [Refer to **4.3**]

(14) Number of times of solder heating (When it is different from the specified ones) [Refer to **4.4**]

(15) Moisture soaking conditions between the solder heatings (When it is necessary) [Refer to **4.4**]

(16) Selection of solder heating method and conditions, or another conditions different from **Table 3** [Refer to **4.4**]

(17) Adhesion method of specimen [Refer to **4.4(3)**]

(18) Application conditions of flux (When it is necessary) [Refer to **4.4(3)**]

(19) Time of the recovery (When it is necessary) [Refer to **4.5**]

(20) Items and conditions of the final measurements [Refer to **4.6**]

(21) Moisture soaking condition, storage condition after unpacking and storage limit after unpacking if rank S used [Refer to **5.**]

REFERENCE 1. SUPPLEMENTER MATTERS RELATED TO THE TEST METHODS

1. PURPOSE OF ESTABLISHMENT

At the beginning, SMD (surface mounting devices) used to be soldered on the printed circuit board by hand work using soldering iron. At that time SMD did not present any problem in particular related to thermal stress during soldering. Since 1980's, SMD began to attract the attention in view of its advantages related to high density mounting, and such methods as vapor phase reflow soldering, infrared reflow soldering, convection reflow soldering and wave soldering, etc., that heating the whole component part and surface of the printed circuit board (overall heating method) become widespread in view of their merits related to batch soldering of the component parts.

However, in these methods, not only the terminals but also the body of the SMD are heated up to temperatures above the melting point of the solder, and it was found that package crack may occur in the case of plastic encapsulated SMD. When SMD absorbing moisture during room storage are soldered, the package crack may be occurred by the high pressure water vapor generated internally due to the heat of the package during soldering. This problem tends to occur more frequently in IC and LSI containing large-sized dice, and is very rare in discrete semiconductors.

Then this test method was established by examining the problem of moisture absorption of SMD during the storage and the conditions of the soldering.

2. EVOLUTION OF ESTABLISHMENT

Since SMD for ICs and LSIs are more susceptible to soldering heat compared with other surface mounting components such as passive components, and they are more influenced by the effects of moisture absorption during storage before soldering, the provisional standards **EIAJ EDX-4701** (Test Methods for Resistance to Soldering Heat of Surface Mounting Devices for Integrated Circuits) were established on march, 1990. After that, the test method **A-133** in **EIAJ ED-4701** was established properly on February, 1992 by making partial modifications in **EIAJ EDX-4701**, so as to expand the scope of application to hermetic sealed SMD and discrete semiconductors.

And then, the test method **A-133A** was established on March, 1995 by revising the test method **A-133**, so as to correspond to the problem of storage after opening the dry pack and the problems which were found in infrared reflow soldering and wave soldering. And further, the test method **A-133B** was established on June, 1998 by revising the test method **A-133A**, so as to correspond to the problem of moisture absorption between plural times of soldering, classification of solder heating by the infrared reflow soldering and the convection reflow soldering depending on the package volume of SMD, and internal inspection method using by the scanning acoustic tomography (SAT).

In addition, the moisture sensitive rank and acceleration soaking were added with consideration of **JEDEC** level, and the standard was revised as **EIAJ ED-4701/300** test method **301** on October, 2000 in according to the reexamination of the standard system.

3. PRESETTING THE TEMPERATURE CONDITIONS OF THE SOLDER HEATING EQUIPMENT

3.1 Presetting the temperature conditions of the reflow soldering method

Damages occurring in the SMD during the soldering depend on the packaged body temperature and

the moisture concentration at the first interface in package. (It will be explained in detail later on.) In the infrared reflow soldering, convection reflow soldering and vapor phase reflow soldering, when heating conditions are preset by observing temperature of SMD terminals or atmosphere in these equipment, serious doubts about the repeatability of the test results occur because there are substantial differences of the packaged body temperature depending on such factors as the combination of temperature presetting conditions of the heating equipment and the speed conditions of the belt conveyor, types of the heating equipment, the type of the SMD, and material and size of the holder. Therefore, it is indispensable to specify the heating conditions in the reflow soldering method in terms of the temperature of the SMD body, (temperature of the top surface of the SMD) and the repeatability of the test results must be secured.

The solder heating conditions must be preset by measuring temperature of the top surface of the SMD that a thermocouple attached to its surface as shown in **Figure 1**, in the heating equipment according to the same steps of procedure as those ones of the test. A thermocouple must be attached to the SMD surface tightly with the adhesive agent or the thin heat proof tape. As long as the conditions are specified in terms of the surface temperature of the SMD, it is not necessary to specify the model of the heating equipment and to specified details of the holder.

Moreover, a thermocouple was attached to the top surface of the SMD by the adhesive agent in test method **A-133** and **A-133A**, however, the method of attaching a thermocouple to the package surface with the thin heat proof tape was added to the test method **A-133B**, because to be able to measure the temperature sufficiently with the thin heat proof tape was ascertained.

3.2 Presetting the temperature conditions of the wave soldering

The heating conditions related to the wave soldering are specified in terms of the molten solder temperature and dipping duration, because a quantity of heat conducted and conveyed from the molten solder to SMD is stable. However, the temperature conditions of preheat must be specified in terms of the surface temperature of the SMD.

4. TEST PROCEDURE

4.1 Baking

When saturated moisture soaking conditions are assumed as a premise, the baking is not needed. However, since moisture soaking conditions specified in Sub-clause **4.3** are set for the almost saturated conditions, are not set for the perfect saturated conditions, and the test results may depend on whether the baking is performed or not. Therefore the baking is needed to heighten reproducibility of the tests.

4.2 Moisture soaking

It was found that package cracks during solder heating were induced by pressure of water vapor from the moisture contained in the resin near the bottom surface of die pad or near top surface of the die (hereinafter called the first interface). Such being the case, moisture soaking conditions must be specified in such a way that the moisture concentration at the first interface coincides with the moisture concentration after the actual storage of SMD. Therefore moisture soaking conditions specified in Sub-clause **4.3** are specified in such a way that the moisture concentration at the first interface coincides with the moisture concentration of the allowable maximum storage conditions. Details related moisture soaking are explained below.

4.2.1 Method to obtain the moisture concentration of the resin at the first interface

Since the moisture concentration at the first interface can not be measured, the moisture absorption characteristics of the resin are analyzed by the fitting technique shown below, and the moisture concentration can be calculated from the numerical values of these characteristics.

In the first place, when a resin plate (having side areas as small as possible) with thickness d cm is stored under constant temperature and constant humidity conditions, moisture penetrates from the surface to the interior of the resin plate according to the diffusion law of Fick, given by the equation (1)

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x} \text{ .... (1)}$$

where C(x,t): Moisture concentration (mg/cm^3) at the point x (cm) of the thickness coordinate having its origin at the center of the resin plate, and at the time t (s)

D : Moisture diffusion coefficient (cm^2/s) of the resin.

Assuming that immediately after the storage the surface of the resin reaches the saturated moisture concentration Qs, the boundary conditions are given by the following equation.

$$\left.\begin{array}{ll} C(x,t)=0 & (-\frac{d}{2} < x < \frac{d}{2}, t = 0) \\ C(x,t)=Qs & (x = \pm\frac{d}{2}, t > 0) \end{array}\right\} \text{ .... (2)}$$

and the equation (3) is obtained as a result.

$$C(x,t) = Qs\left[1 - \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{(-1)^n}{2n+1}e^{-\frac{(2n+1)^2\pi^2 Dt}{d^2}}\cos\left(\frac{2n+1}{d}\pi x\right)\right] \text{ .... (3)}$$

On the other hand, given that area of the resin plate is S, amount of the moisture quantity W(t) (g) of the resin plate will be given by equation (4).

$$W(t) = S\int_{-\frac{d}{2}}^{\frac{d}{2}} C(x,t)dx = S \cdot d \cdot Qs\left[1 - \sum_{n=0}^{\infty}\frac{8}{(2n+1)^2\pi^2}e^{-\frac{(2n+1)^2\pi^2 Dt}{d^2}}\right] \text{ .... (4)}$$

Given Bolzmann factor k, absolute temperature T, pressure of moisture P, activation energy of moisture diffusion Ed, activation energy of moisture dissolubility Es, coefficient D0, n and S0, the moisture diffusion coefficient D and the saturated moisture concentration Qs can be obtained by equations (5) and (6).

$$D = D_0 e^{-\frac{Ed}{kT}} \text{ ....(5)}$$

$$Qs = P^n S_0 e^{\frac{Es}{kT}} \text{ ....(6)}$$

By comparing equation (4) and the values of measured amount of the moisture quantity that the resin plate is stored under constant temperature and constant humidity conditions, Es, Ed, D_0, S_0 and n which are the moisture soaking parameters can be obtain by fitting technique. These moisture soaking

parameters depend on the kind of resin. When these quantities are obtained, the moisture concentration at various places inside the resin can be obtained by equation (3). The moisture concentration at bottom surface of the die pad and top surface of the chip surface (first interface) can be obtained by substituting x=0 in the equation (the cos term becomes 1).

4.2.2 Characteristics of saturated moisture concentration of resin

The moisture concentration of resin at the saturation depends on the relative humidity clearly as shown in **Figure B1**. Although **Figure B1** is one of example, another type of resin has similar characteristics, too. So the condition of moisture soaking to be fit for the assumed storage environment can be obtained from **Figure B1**.

FigureB1 Examples of dependence, on temperature and relative humidity, of the saturated moisture concentration of the resin

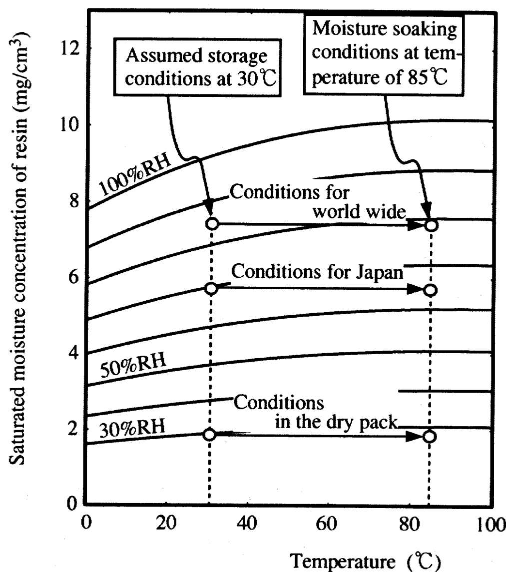
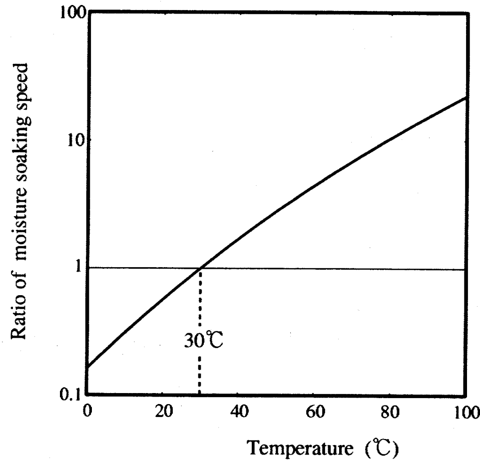


Figure B2 Example of moisture soaking speed depended on temperature (Speed at 30°C=1)



4.2.3 Moisture absorption speed

The moisture absorption speed in the resin is directly proportional to moisture diffusion coefficient D depended on temperature, therefore, the absorption speed increase according to temperature. When rising temperature from 30°C to 85°C, the absorption speed can be accelerated roughly to one figure as shown in **Figure B2**. By defining the resin thickness (length between surface of SMD to the first interface) as shown in **Figure B3**, the absorption speed at the first interface is inversely proportional to the square of the resin thickness (d/2 in the equation (3) corresponds to the resin thickness). Therefore the longer moisture soaking time is needed in order to saturate the moisture absorption of thicker SMD. (refer to **Figure B4**)

Figure B3 Definition of resin thickness

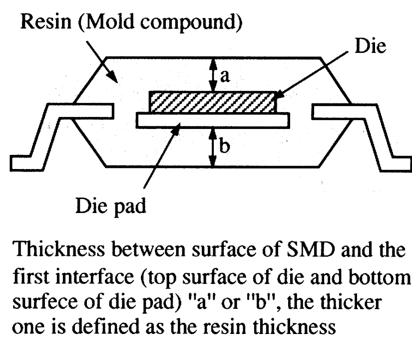
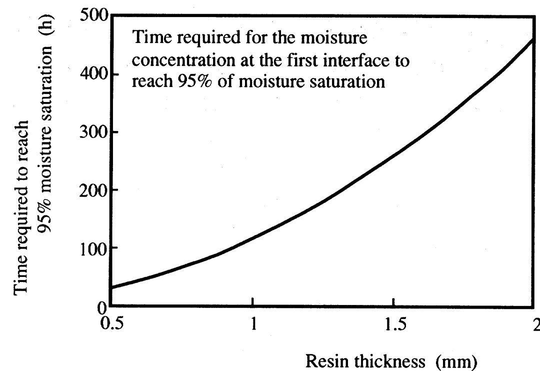


Figure B4 Example of dependence, on the resin thickness, of moisture soaking time at 85°C to reach moisture saturation



4.2.4 Necessity of saturated conditions of moisture soaking

Moisture sensitive SMD can be stored for long term in the dry pack, and absorb moisture toward moisture saturation under conditions in the dry pack that atmosphere in the dry pack stored for long time is stabilized to lower humidity. The moisture concentration absorbed in the dry pack will be higher than that between opening the dry pack and the soldering when SMD have medium and thicker thickness.

Therefore, the first step moisture soaking corresponded to storage condition in the dry pack specified in Sub-clause **4.3(1)** must simulate the above moisture saturation.

Moisture absorption of the non dry packed SMD which is stored in the room is unstable, and does over again to absorb and dry. The non dry packed SMD must be fit for long term storage under the worst condition of the average humidity in the storage atmosphere. So the moisture soaking which corresponds to the saturated moisture absorption of the worst condition is required.

4.2.5 Moisture soaking conditions for the dry packed SMD and rank of resistance to soldering heat

Dry packed SMD absorbed moisture not only after unpacking but also in a dry pack. Moisture absorption in a dry pack is negligible when baking performed before dry packing, however humidity control is necessary from end of baking to dry packing. These absorption stages should be considered when absorption condition decides.

The manufacturer controls the moisture concentration of SMD before packing, and then, seal up SMD in the dry pack composed of a moisture proof bag and desiccants. But the dry pack is not perfect (the relative humidity in the dry pack is not 0%RH). SMD, IC-trays, desiccants, etc. that are packed in the dry pack contain the moisture a little before the packing. The relative humidity in the dry pack differs in whether the baking of SMD and IC-trays is performed before packing, how do the humidity control, how to treat the contents. However the moisture control is performed, there are the pinhole and the damage of the bag, the unsealing and resealing a bag in the shipping.

Generally the humidity indicator is enclosed in the dry pack. This indicator is an exclusive type or the blue beads to be mixed with the desiccant. Generally the sensitivity of the humidity indicator which the Japanese semiconductor manufacturer uses is about 30%RH, and it is requested user to confirm that the humidity in the dry pack is less than 30%RH just after opening the dry pack.

And generally, for the dry pack, it is permitted to store a long term with SMD in the cabinet which is

controlled in less than 30%RH.

Besides, it can be considered that the moisture amount, which is absorbed in SMD during such operation for a short time as inspection or repacking of SMD, can be recovered to the original condition if SMD are sealed up in the dry pack or kept in the cabinet, which is controlled in less than 30%RH, after that operation.

As mentioned above, conditions of the first stage moisture soaking is 85°C, 30%RH, 168h (but, it should be saturated.) from **Figure A1** if the conditions of humidity in the dry pack or storage is controlled by 30%RH. However, **Table 1** is shown as a typical example as some of semiconductor suppliers specify other conditions from 30%RH. (In USA, EIA/JEP113-B specifies 20%RH for example.) The strict control, such as monitor of the weight gain of SMD in the dry pack, will not be required, if the first stage moisture soaking conditions are set at the worst condition of humidity in the dry pack. On the other hand, the first stage moisture soaking condition less than 30%RH to be saturated can be applied when the humidity in the dry pack is controlled strictly. (For example, the specimen may be soaked by 85°C, 10%RH if it is controlled below 10%RH.) In this case, several limited conditions, such as execution of the weight gain monitoring of SMD in the dry pack, or prohibition of opening and resealing of the dry pack, may be often required.

The maximum allowable storage conditions of SMD between opening the dry pack and soldering are different by the types of SMD, which will be specified by semiconductor suppliers. So, conditions of the second stage moisture soaking should be specified in the relevant specification. Conditions of 30°C, 70%RH, 168h are used as the maximum allowable storage conditions of SMD in Japan by many Japanese semiconductor suppliers. Accordingly, these conditions are shown in **Table 1** as the representative condition. (In Japan, 30°C of temperature is standardized, however, various conditions for humidity (60%RH to 85%RH) and soaking time (few hours to 336 hours) are applied).

The **Figure B5** shows comparison of the moisture calculation results between maximum allowable storage conditions and moisture soaking conditions shown in **Table 1**. Moisture absorption of all kinds of SMD will be saturated not related with the resin thickness when SMD are stored for a long term (1 year for example) in the dry pack. It is understood that the soaking condition of 85°C, 30%RH to be saturated (the first stage moisture soaking) can be applied. Besides, the soaking conditions of 30°C, 70%RH for 168h after the first stage moisture soaking can be applied to the case of that SMD are stored under conditions of 30°C, 70%RH for 168h after the storage in the dry pack for a long term. Then, the soaking conditions of two steps are required independent of the kinds of SMD due to correspond to the real storage conditions of SMD.

The rank of resistance to soldering heat is laid down. The rank is included **JEDEC's** level. A comparison between **JEDEC's** level and **JEITA's** rank is shown in **Table B1**.

The storage condition assumed 30°C, 60%RH in **JEDEC's** standard, and 30°C, 70%RH in **EIAJ 's**. So the classification of resistance to soldering heat in **JEITA's** is named "rank" and they have distinguished between **JEDEC's** level and **JEITA's** rank. Furthermore, lead free soldering is also considered when the rank is fixed.

Figure B5 Comparison between moisture soaking conditions and assumed storage conditions for dry packed SMD

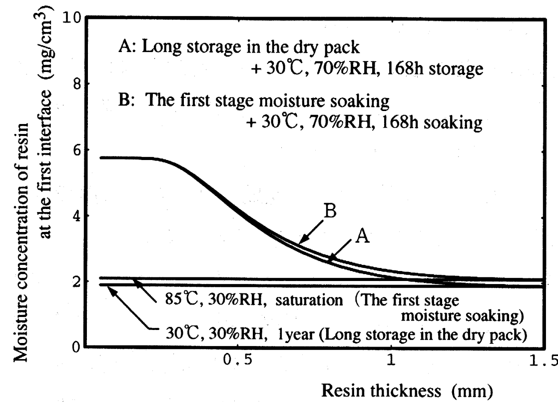


Table B1 Comparison between JEITA's rank and JEDEC's level

JEITA (EIAJ ED-4701/300-Test Method 301)			JEDEC(IPC/JEDEC J-STD-020A)		
Rank	Storage conditions	Storage time	Level	Storage conditions	Storage time
A	≤30°C, 85%RH	Unlimited	1	≤30°C, 85%RH	Unlimited
B	≤30°C, 70%RH	1 year	2	≤30°C, 60%RH	1 year
C	≤30°C, 70%RH	4 weeks	2a	≤30°C, 60%RH	4 weeks
D	≤30°C, 70%RH	2 weeks	—	—	—
E	≤30°C, 70%RH	168h	3	≤30°C, 60%RH	168h
F	≤30°C, 70%RH	96h	—	—	—
G	≤30°C, 70%RH	72h	4	≤30°C, 60%RH	72h
H	≤30°C, 70%RH	48h	5	≤30°C, 60%RH	48h
I	≤30°C, 70%RH	24h	5a	≤30°C, 60%RH	24h
S	specified individually	specified individually	6	≤30°C, 60%RH	TOL(1)

Note(1) TOL: Time On Label

Accelerated moisture soaking condition is studied since the test time of the two step moisture soaking is long. The one step moisture soaking can be substituted for the two step moisture soaking, if the moisture density under the one step moisture soaking is more than the density of the two step moisture soaking. The second step of the moisture soaking can be also accelerated moisture soaking. And a simulation result of moisture soaking is acceptable. In the case of rank E, the condition of the second step moisture soaking can be 85°C, 65%RH, 19h, and 85°C, 65%RH 38h for 1 time is also acceptable as shown in **Figure B6**. However the condition depend on the package type and a material of resin. Acceleration condition varies and the major conditions are as follows.

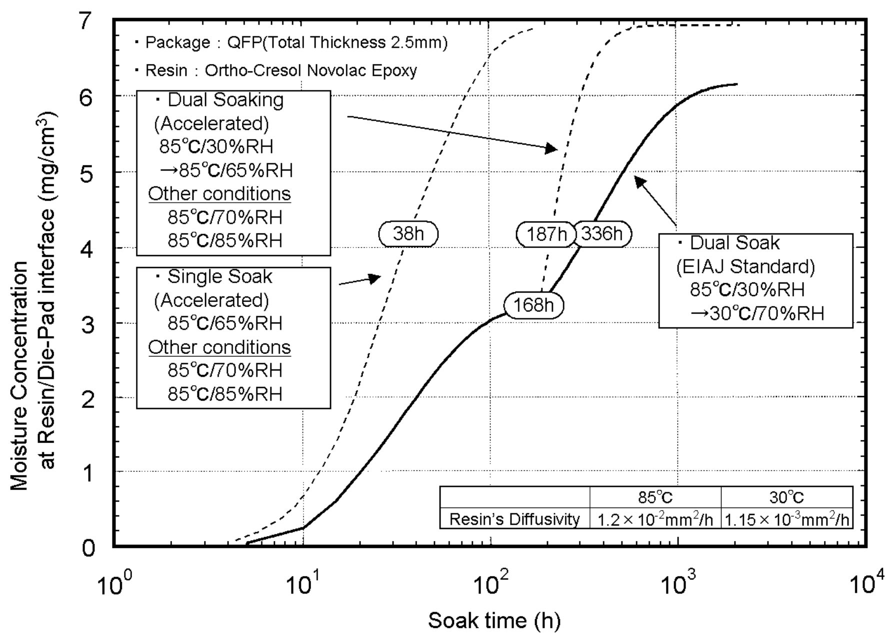
85°C, 65%RH

85°C, 85%RH

85°C, 70%RH

The temperature of acceleration condition does not exceed the glass transition temperature of a resin. MET (Manufacturer Exposure Time) is not stated in this standard, because it makes the procedure complicated. The worst temperature and humidity condition in a dry pack is stated as an alternative plan.

Figure B6 Example of accelerated moisture soaking conditions

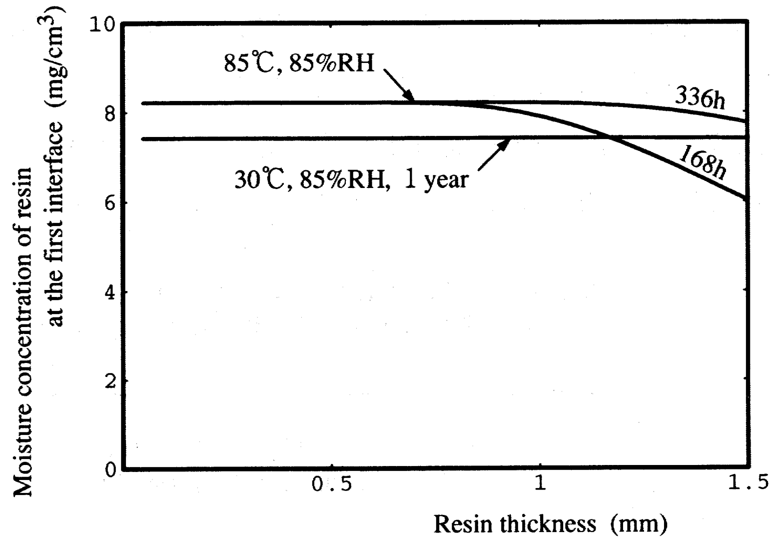


4.2.6 Soaking conditions for non-dry packed SMD

The moisture soaking conditions of 85°C, 65%RH to saturation is required for 30°C, 70%RH, which is the average value for several months (around five months) during summer season in Japan if SMD are kept in a room such as store house. (Refer to **Figure B1**.) Generally 168h of soaking time is needed or 336h of soaking time is needed for thicker SMD, which must be specified in the relevant specification.

However, the overseas environmental conditions should be considered because the case that electronic equipment is assembled at a foreign plant has increased recently. The average environmental conditions of 30°C, 85%RH will be enough for these cases, when SMD are stored in a room. The conditions of 85°C, 85%RH, which is used for temperature humidity test generally, can be applied as the soaking conditions for this case. **Figure B1** shows that the soaking conditions of 85°C, 85%RH is corresponded to the storage conditions of 30°C, 90%RH. So, the conditions of 85°C, 85%RH for 168h, not to saturation, can be applied for almost of SMD. (Refer to **Figure B7**.) The soaking conditions must be specified in relevant specification if a long soaking time is necessary for thick SMD.

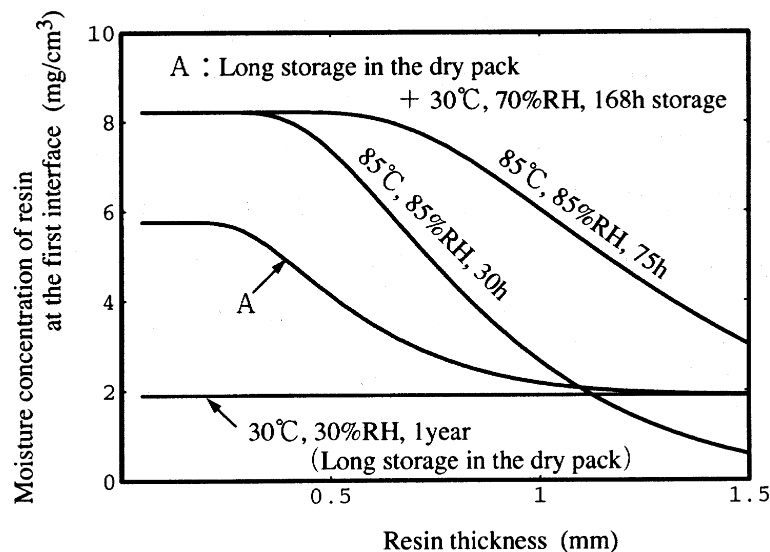
Figure B7 Example of comparison between storage of 30°C, 85%RH for 1 year and moisture soaking of 85°C, 85%RH



4.2.7 Case of that moisture soaking is not required

Moisture soaking is not required for hermetic packaged SMD because moisture is not absorbed in them. And, in accordance with the relevant specification the moisture soaking can be omitted for plastic molded SMD having a small die because moisture can not affect them.

Figure B8 Comparison between single stage moisture soaking and assumed storage condition



4.2.8 Other soaking conditions

Other conditions, 85°C, 85%RH for a short time, such as 30h or 75h, etc., were proposed during establishment of **EIAJ EDX-4701**. In these unsaturated conditions, thin SMD are soaked excessively and thick SMD are soaked insufficiently as shown in **Figure B8** because the first stage moisture soaking is omitted. The moisture concentration at the first interface after moisture soaking become lower than that after real storage if SMD are thicker. Accordingly, these conditions had not been adopted.

4.2.9 Moisture soaking condition in USA

In USA, moisture soaking conditions and storage conditions (Floor life) were specified in standards of **JEDEC-IPC/J-STD-020**, **IPC-SM-786A** and **EIA/JEP113-A** before 1999. A maximum allowable relative humidity in the dry pack that is 20%RH was specified in standards of **IPC-SM-786A** and **EIA/JEP113-A**, and further, it was specified that SMD after opening the dry pack can be stored for a long time into the condition of 20%RH. And then, moisture soaking conditions and storage conditions in the above standards were classified into 6 levels as follows.

(1) LEVEL-1 and LEVEL-2

LEVEl-1 of moisture soaking conditions requires 85°C, 85%RH, 168h for long term (limit free) storage at 30°C, 85%RH. And LEVEL-2 of moisture soaking conditions requires 85°C, 60%RH, 168h for long term (1 year) storage at 30°C, 60%RH. LEVEL-1 is almost corresponds with Condition B given in **Table 2** of Sub-clause **4.3**. But as **Figure B7** shows, there is a case that some SMD are short of moisture soaking time for long term storage at 30°C, 85%.

(2) LEVEL-2a to LEVEL-5

LEVELs 2a to 5 stipulate moisture soaking conditions to cover storage time at 30°C, 60%RH after opening the dry pack (it is defined as floor life and is classified into five parts of storage time). These levels require 24h for Manufacture's Exposure Time (MET) between bake and bag plus the maximum time allowed out of the bag at the distributor's facility. LEVEL-3 is for SMD to solder by 168h after opening the dry pack (it is mean that floor life is 168h) and moisture soaking condition is 30°C, 60%RH, 192h (floor life plus MET(=24h)) after baking of 125°C, 24h. LEVEL-4 requires moisture soaking time of 96h for floor life of 72h and LEVEL-5 requires soaking time of 48h or 72h for floor life of 24h or 48h, in the same way as LEVEL-3.

As stated above, these moisture soaking conditions are based on conditions that relative humidity in the dry pack is 0%RH because these consist of the baking, the MET and the floor life. Therefor SMD, IC trays and other materials in dry pack must be completely baked just before packing into the dry pack by semiconductor suppliers.

On the other hand, in **IPC-SM-786A** and **JEP113-A**, their permissible relative humidity in the dry pack was 20%RH, and further, it was specified that SMD can be stored for long a time (limit free) after opening the dry pack when relative humidity is below 20%RH. Therefore LEVEL-2a to 5 did not correspond with the conditions of **IPC-SM-786A** and **JEP113-A**.

Figure B9 shows comparison of moisture soaking conditions of LEVEL-3 and storage conditions (A: 0%RH in the dry pack, B: 20%RH in the dry pack). This figure shows the following. If SMD are stored in the perfectly dried dry pack for long a time (assumption: MET=0), moisture soaking condition of LEVEL-3 can cover floor life of 30°C, 60%RH, 168h after opening the perfectly dried dry pack. But when relative humidity in the dry pack become 20%RH, moisture soaking condition of LEVEL-3 can not cover the floor life of 30°C, 60%RH, 168h. In addition, it can not cover the floor life of thick package that relative humidity in dry pack become 10%RH.

As stated above, moisture soaking conditions of LEVEL 2a to 5 were based on ideal conditions that the contents in dry pack were dried completely and can not cover long time storage at permissible relative humidity 20%RH being stipulated by **IPC-SM-786A** in dry pack.

Therefore moisture soaking conditions of LEVEL 2a to 5 were not adopted at this committee

because these conditions did not fit real assembly environment because they can not guarantee relative humidity of 0%RH in the dry pack as follows.

(a) We do not have humidity indicator to correctly guarantee 0%RH in the dry pack

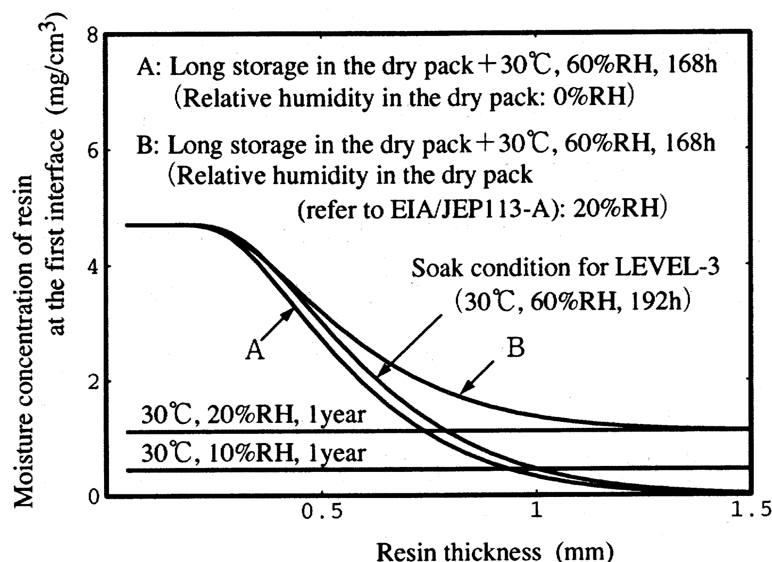
(b) It is very difficult to completely dry and pack all contents in the dry pack

(c) We do not have system to control packing the dry pack and temporary opening the dry pack in distributor's facility.

(d) We can not supply pinhole free or scratch free dry pack.

In addition, moisture soaking conditions of **JEITA** can cover one of customer's requirements that SMD are stored in dry cabinet controlled humidity (below 30%RH) instead of dry pack. On the other hand, the upper relative humidity limit in a dry pack was changed to 10% and revised as **J-STD-020A**, **JEP113-B** following the discussion of **JEDEC/JEITA** Joint Meeting. A little lack of moisture soak may result as a thick package with 10% of relative humidity. However it is conceivable that there is no contradiction in the moisture soak condition when the strength of a package is considered.

Figure B9 Comparison between moisture soaking conditions and assumed storage conditions for JEDEC Floor Life LEVEL-3



(3) LEVEL-6

This standard specifies that those SMD which should be soldered within TOL (Time on label) after baking, shall be stored at 30°C, 60%RH for 6h.

4.2.10 Moisture soaking between plural solder heating

Moisture soaking between plural solder heatings, a new proposal on moisture soaking conditions, as shown in **Figure B10 (B)** was given during discussion of revising this test method because SMD absorb moisture between real plural soldering process and it is practical as shown in **Figure B10 (A)**. Moisture soaking of Sub-clause **4.3 (1)** is performed as shown in **Figure B10 (B)** that the first stage moisture soaking corresponding to long storage in the dry pack is performed and subsequently, the second stage moisture soaking corresponding to the full amount of storage between opening the dry pack and final soldering is performed. Therefore real storage conditions after opening the dry pack,

the full amount of storage between opening the dry pack and final soldering, must be controlled within conditions of the second stage moisture soaking.

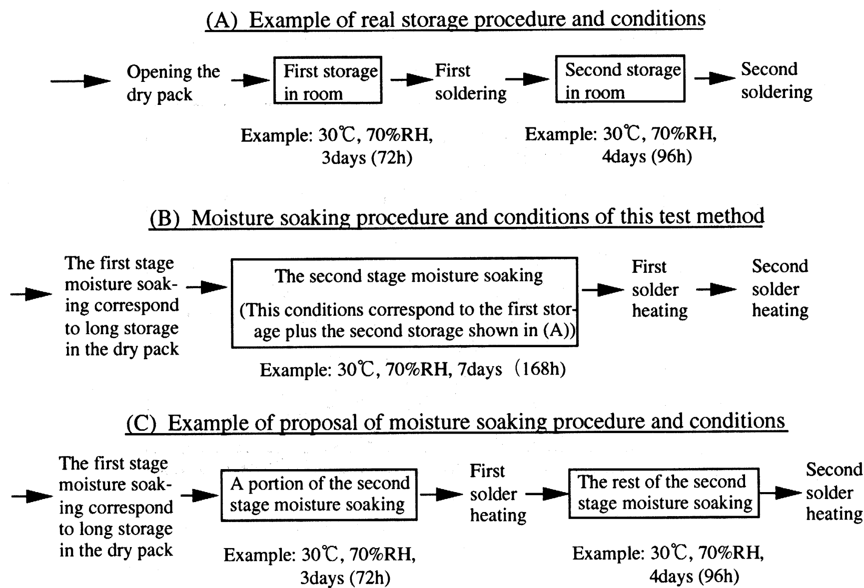
Our committee members made experimentations that the second stage moisture soaking of this test method mentioned above and the new proposal as shown in **Figure B10 (C)**. And the assumption of these experimentations is that conditions of the second stage moisture soaking coincide with the sum of soaking conditions between the first stage moisture soaking and final solder heating of the new proposal.

Consequently, two kind of experimentation results are obtained, on the hand moisture soaking of this test method is severer than new proposal, on the other hand the new proposal is severer than moisture soaking of this test method, it is understood that these experimentation results are depended on structure of the SMD.

In the new proposal, the second stage moisture soaking must be divided into two conditions, but semiconductor user have various storage conditions. Therefore the ratio of dividing the second stage moisture soaking can not be specified.

As mentioned above, our committee have decided that the new proposal, which can be adopted if required by the relevant specification, is not adopted.

Figure B10 Examples of real storage conditions and moisture soaking conditions in the event that twice soldering are performed



4.3 Solder heating

4.3.1 Plural solder heating

Number of times of the solder heating of this test method is twice. However real soldering process has possibility of three times of soldering, therefore three times of the solder heating can be applicable as the maximum times when it is specified into the relevant specification. In this case, if soldering temperature during rework is lower (temperature of SMD's body is below 200°C, or heating by the soldering iron), adding its number of times to that of the solder heating may be not needed.

The moisture soaking of this test method corresponds to the moisture soaking from opening the dry pack to the final soldering of the real soldering process. Therefore, moisture soaking is not carried out

between plural solder heatings (see Sub-clause **4.2.10**).

When the solder heating is carried out twice or more, the heating procedures specified in Sub-clause **4.4** must be repeated. For example, when solder heating of Method II at 215°C for 40s is repeated twice, heating of 215°C for 40s is made, subsequently, temperature must be cooled down to below 50°C, and temperature must be raised by the same conditions again. Substitute conditions such as 215°C for 80s are not appropriate though duration time is equal to twice of 40s.

4.3.2 Temperature profile method I (Infrared reflow, Convection reflow soldering)

Since the purpose of soldering is to connect SMD to the printed circuit board, measuring temperature of the terminals of SMD is an ideal for the soldering heat test. However, SMD's resistance to soldering heat depends on the surface temperature of the body. If conditions of the solder heating are defined by temperature of the terminals, test results will be unstable as mentioned in Sub-clause **3.1**. Therefore, in order to ensure test repeatability, conditions of the solder heating for reflow methods could not be help defining temperature of the body surface. Further, as temperature profile of these methods are unstable, temperature of SMD's body surface must be measured for each time of soldering heat test.

The maximum temperature at the body surface during solder heating depends on heat capacity, heat resistance of SMD. Therefore each members of this committee conducted experiments in correlation between surface temperature at the time of soldering, and body thickness and volume using various SMD, which indicated a good correlation between volume of SMD and body surface temperature. With considering circumstance mentioned above, it is decided that the heating condition I-A (peak temperature: from 235°C to 240°C) shown in **Table 3** is applied to small of medium size SMD whose volume is less than 2000mm^3, and the heating condition I-B (peak temperature: from 220°C to 225°C) is applied to large size SMD whose volume is over 2000mm^3.

For getting good solder junction, SMD terminals should be heated up to at least 210°C. When various SMD having differ in volume are soldered on the same printed circuit board, the larger the device volume is, the lower its peak temperature of terminals becomes. Therefore, soldering conditions must be set in terms of the terminal temperature of the largest SMD at least 210°C.

When terminal temperature of the largest SMD is set from 210°C to 215°C, body surface of larger SMD having over 2000mm3 in volume on the same printed circuit board do not reach 220°C, and that of small SMD having less than 2000mm3 on the same printed circuit board reach over 220°C. Therefore applying solder heating conditions are decided as mentioned above.

This test method had adopted solder heating condition I-A. In this case, if this condition is applied to large SMD, temperature of the printed circuit board reaches from 250°C to 280°C and foul smell is generated from heated printed circuit board, because power of reflow furnace must be increased in order to heat large SMD having tendency that raise speed of temperature is slower. Therefore condition I-B was added to Test Method **A-133A** as a corrective action against this problem, and can be selected one of two conditions.

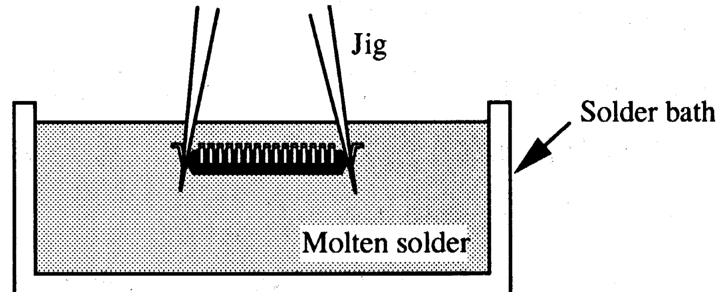
4.3.3 Temperature profile of method II (Vapor Phase Reflow)

Because that the upper temperature limit, which is the property of perfluorocarbon, reaches 210±5°C, the period while the upper temperature limit is to be kept should be longer, and **IEC-749** second edition adopted the period of 40s, the period is decided to 40s.

4.3.4 Method III (Wave soldering)

A test method that the entire of the specimen are immerse into molten solder as shown in **Figure B11** was specified in **EIAJ EDX-4701** and **EIAJ ED-4701**, **IEC-749** second edition.

Figure B11 Whole immersion method into molten solder



However, it is reported that the conventional method shown in **Figure B11** becomes too severe as a test method, because the entire body of SMD is immersed in the molten solder and the temperature of SMD itself goes up to higher degrees than that of actual soldering. Meanwhile, when the wave soldering method is used, the temperature of the inside of the package goes up slowly because only one side of SMD is immersed into the flowing molten solder, and the radiation effect from the other side of SMD is also recognized. Consequently, the peak temperature of the inside of the SMD is lower than that during immersing entire of SMD into solder bath.

Accordingly, the conventional method was abolished when the test method **A-133** was revised, and the new method, immersion into the flowing molten solder after the SMD is temporarily fixed on the holder as shown in **Figure 5**, was introduced in order to match the actual soldering condition.

The heating conditions were decided as Condition III-A (260°C, 5s) and III-B (260°C, 10s), corresponding to the single-wave and the double-wave soldering.

If flux is applied to the specimen, the flux vaporizes quickly during the immersion. At this time, the atent heat is deprived, which prevents the temperature of SMD from rising. Therefore, it is desirable that the flux is not applied. When the flux is applied, only a small amount should be applied to the terminals and the body of SMD should be avoided. More, when this method is used, the molten solder must be flowed all the time. The static solder bath should not be used because the temperature of the part of solder which the specimen contacts lowers.

4.3.5 The method IV (Terminal immersion into solder bath)

As the SMD is soldered by soldering irons in some cases, the method is provided as Condition IV-A.

4.3.6 Solder heating condition for the lead free soldering process

As the lead free soldering methods, which will need changing temperature condition of soldering, are under consideration now, solder heating conditions of this test method must cover their soldering conditions when their methods will be established and become widespread in the future.

5. SAT (Scanning acoustic tomography)

5.1 Background

JEITA decided to include SAT criteria in the test method because **IEC** and **JEDEC** have been studying SAT criteria for resistance to soldering heat and Japanese semiconductor companies have

already started using SAT.

Moreover, there is a SAT test standard of **EIAJ ED-4703-1** J-123.

5.2 Conformity to JEDEC SAT criteria

JEITA and **JEDEC** have discussed test methods in order to conform to the **JEDEC** standard in 1996/Sep. and 1997/Oct.. **JEDEC** suggested considering the specimen to be a failure if it should be an electrical failure, or has external cracks and internal cracks defined in item **4.6.2**. And to be judged by the results of reliability tests if it should have delaminations as given in the **JEDEC** SAT criteria (**J-STD-020A**)

5.3 Criteria

The committee considered the opinion survey results of 16 companies (shown in **Table C1**) for **JEDEC** criteria. Although there were many opinions to consider the specimen to be a failure if an entire delamination of the die surface should exist, the committee has decide that the delamination shall be judged by the results of reliability test with a view to conforming to **JEDEC** standard, because the entire delamination does not always cause reliability failure. Also, the committee has decided to match internal cracks criteria in **JEITA** to **JEDEC** criteria.

Table C1 Opinion survey results of JEITA reliability sub committee for JEDEC criteria

Inspection items	FAIL	PASS	Judged after reliability test
Electrical measurements	16	0	0
External crack	16 (1)	0	0
Internal crack 1 intersect wire, bond	16	0	0
Internal crack 2 to other feature	14	0	2
Internal crack 3 distance >2/3	12 (2)	0	4
Delamination 1 on die surface	12 (3)	1	5 (4)
Delamination 2 on wire bond surface	4	2	10
Delamination 3 (5) Polymeric film	0	3	13
Delamination 4 (6) die attach region	3 (7)	3	10
Delamination 5 (8) feature > entire length	1	1	13
Other delamination back side of die paddle	0	1	1 (9)
Other delamination PBGA: mold and PCB	1	0	0
Other: cracks (10) small internal cracks	1	0	0
Other: cracks (11) wire bond	1	0	0

Each opinion below was from one of sixteen companies.

(1) Visual inspection

(2) More than 2/3 distance shall be needed to discuss
It should be FAIL if it would be YES

(3) It should be FAIL if it would extend to Al PAD
Entire delamination shall be judged FAIL
Small delamination shall be judged PASS
Partial delamination shall be judged by reliability test

(4) Small delamination does not reach Al PAD

(5) No criteria

(6) Die attach delamination shall be eliminated from SAT criteria because it is difficult to measure die attach delamination

(7) It should be FAIL if cracks would be measured
Standard package results shall be referred
It should be FAIL if delamination more than 70% in thermal enhanced package would be measured.

(8) No criteria

(9) It should be FAIL if delamination would cause cracks

(10) Small internal cracks visible by SAT

(11) Internal cracks 3 toward wire

TEST METHOD 302
RESISTANCE TO SOLDERING HEAT EXCLUDING SURFACE MOUNTING DEVICES

1. SCOPE

This standard provides for the methods to evaluate the resistance to heat working on the semiconductor device during soldering.

2. TEST EQUIPMENT

2.1 Solder bath

The solder bath should be sufficiently large to keep the solder temperature at the value specified in section **4.2**

2.2 Immersion equipment

The dipping depth of the terminals and the dipping duration in the solder bath, specified in section **4.2**, should be controllable.

2.3 Radiator and thermal shield

When using radiator and/or thermal shield, details related to the material, dimensions, construction, mounting method and required protection devices should be specified in the detail specifications.

3. MATERIALS

3.1 Solder

Solder to be used in this test should be those ones specified in H60A, H60S, H63A of **JIS Z 3282** (SOLDER) or in APPENDIX B of **JIS C 0050**.

3.2 Flux

Flux to be used in this test should be the solution consist of 2-propanol (**JIS K 8839**) or ethanol (ethyl alcohol, **JIS K 8101**), and rosin (**JIS K 5902**) (the concentration should be from 10% to 35% of rosin in terms of mass ratio, and 25% unless otherwise specified) or the material specified in APPENDIX C of **JIS C 0050**.

Remarks

Use passive flux consisting of 2-propanol solution of rosin specified in section **3.2** when carrying out this test as a part of a series of tests, prior to the humidity resistance test.

4. TEST PROCEDURE

4.1 Initial measurement

Carry out the initial measurements in conformity with the items and conditions specified in the relevant specifications.

4.2 Tests

Clean the surface of the molten solder with a spatula (squeegee) made of an appropriate material, so as to keep it clean and glittering. In the first place, dip the terminals to be tested in the flux specified in section **3.2** at room temperature, and then dip them in the solder bath. The place where the terminals are dipped in solder should be 10 mm or more apart from the solder bath wall.

Unless otherwise specified, dip all terminals in the solder bath within 1 second. Next, keep the terminals dipped in the solder according to the temperature and duration mentioned in **Table 1**, in

conformity with the stipulations of the detail specifications. The conditions A are applicable, unless otherwise specified in the detail specifications.

The dipping depth should be up to the stopper when the specimen is provided with stopper, and up to 1 to 1.5 mm from the body of the specimen when it is not provided with stopper, unless otherwise specified in the detail specifications. The dipping should be carried out only once.

When specified in the relevant specifications, thermal shield plate consisting of insulator plate sized 1.5 mm in thickness, and provided with a hole sized according to the size of the terminals, could be placed between the specimen body and the molten solder.

Remarks: about flux dipping

As a general rule, this test requires no use of flux, but use of flux are specified in these standards with the object of preventing the occurrence of solder bridges and other troubles by dipping the specimen in flux, thereby facilitating the end-point measurements .

4.3 Flux cleaning

When the specimen is dipped in flux, cool it down naturally by leaving it standing after dipping in solder. After that, remove the slag of flux from all terminals submitted to the tests, by using the material specified in **JIS K 8839** (2-propanol) or **JIS K 8101** (ethanol).

Table 1 Conditions of the resistance to soldering heat test

Test condition code	Solder temperature (°C)	Immersion duration (s)
A	260±5	10±1
B	350±10	3.5±0.5

4.4 Post-treatment

After finishing the tests, the specimen should be stored in normal condition from 2 to 24 hours.

4.5 End-point measurements

Carry out the end-point measurements in conformity with the items and conditions specified in the detail specifications.

5. INFORMATION TO BE GIVEN IN THE RELEVANT SPECIFICATIONS

(1) Details of the heat shield plate and/or radiator when ever they are used (When required) [Refer to **2.3**]

(2) Solder composition (When solder other than the specified ones is used) [Refer to **3.1**]

(3) Mixing ratio of flux (When flux other than the specified ones is used) [Refer to **3.2**]

(4) Items and conditions of the initial measurements [Refer to **3.1**]

(5) Test conditions (When the test conditions are different from Conditions A of **Table 1**) [Refer to **4.2**]

(6) Terminals not to be tested (When terminals other than the specified ones are to be tested) [Refer to **4.2**]

(7) Solder dipping depth (When the dipping depth is different from the specified ones) [Refer to **4.2**]

(8) Post treatment (When the post treatment is different from the specified ones) [Refer to **4.3**]

(9) Items and conditions of the end-point measurements. [Refer to **4.4**]

6. REMARKS

6.1 Application of the test method to devices having special shape

Relevant specifications equivalent to the present test methods should be established for special devices that are directly soldered on the radiator.

TEST METHOD 303
SOLDERABILITY

1. SCOPE

These standard provides for the method to evaluate the solderability of the terminals of semiconductor devices that are generally connected by soldering.

2. TEST EQUIPMENT

2.1 Solder bath

The solder bath should have capacity large enough to keep the solder at the temperature specified in section **4.4.2**.

2.2 Dipping equipment

The dipping depth of the terminals and the moving speed, specified in section **4.4.2**, as well as the dipping time in the solder bath should be controllable.

2.3 Observation apparatus

The observation apparatus should be equipped with optical system capable of magnifications of 10 to 20 times.

3. MATERIALS

3.1 Solder

Solder to be used in this test should be H60A, H60S, H63A of **JIS Z 3282** (Solder) or solder specified in Appendix B of **JIS C 0050**.

3.2 Flux

Flux to be used in this test should be 2-propanol (isopropyl alcohol, **JIS K 8839**) or ethanol (ethyl alcohol, **JIS K 8101**) solution of rosin (**JIS K 5902**) (the concentration should be from 10% to 35% of rosin in terms of mass ratio, being 25% unless otherwise specified), or the product specified in JIS C 0050 Appendix C.

Flux also don't include any activator.

4. TEST PROCEDURE

4.1 Preparation of the specimen

4.1.1 The surface to be tested should be as it is when received, and it should not be touched with the fingers or other soiled objects.

4.1.2 The specimen should not be cleaned before the test. When specified in the detail specifications, however, greasy materials may be removed by dipping the specimen in neutral organic solvent at room temperature.

4.2 Initial measurements

The outer view of the specimen should be visually examined. When specified in the detail specifications, however, the electrical and mechanical properties should be measured.

4.3 Accelerated aging

When the accelerated aging is specified in the relevant specifications, in principle, one of followings should be performed to the specimen prior to the test.

Remarks

Steam aging corresponds to the influence of prolonged storage. High-temperature storage corresponds to the influence of burn-in, baking, etc.

4.3.1 Aging (1)

Aging should be carried out 4-hour aging in steam atmosphere using the method specified in **JIS C 0050**.

4.3.2 Aging (2)

Aging should be carried out 16-hour high-temperature storage at 150°C.

Remarks

Although IEC Publ. 749 specifies 155°C, the maximum storage temperature of most of the semiconductor devices is 150°C, and this standard adopts 150°C. The storage temperature applicable to devices with maximum storage temperature below 150°C is specified in the detail specifications.

4.3.3 Treatment after aging

After aging, the specimen is left under normal conditions for 2 to 24 hours.

4.4 Tests

4.4.1 Dipping into flux

Prior to dipping the specimen in solder, it should be dipped in flux specified in section **3.2**.
When specified in the relevant specifications, only the terminals and/or electrodes to be tested should be dipped in solder.

4.4.2 Soldering method

Carry out the solder dipping test in conformity with the method described below, unless otherwise specified in the detail specifications.
When executing the solder dipping test, use solder specified in section **3.1**, and rake the surface of the molten solder with an appropriate spatula (squeegee) right before each test, so as to keep it clean and glittering. After dipping the specimen in flux, and then dip it directly in the solder bath. The place to dip the terminals, should be 10 mm or more apart from the walls of the solder bath. Unless otherwise specified in the detail specifications, the specimen should be dipped up to a place 1 mm to 1.5 mm apart from its body.
Specimens of SMD should have their body dipped in the solder bath, and specimens of small-sized package devices with leads should be dipped in the solder bath up to the mounting position on the circuit board. The moving speed for dipping and removal form the solder bath should be 25 mm/sec ±2.5 mm/sec.
Pre-heating can be carried out when required. Time for movement should not be included in the dipping time. Solder dipping condition is shown in **Table 1**.

Table 1 Solder dipping condition

Condition Symbol	Dipping temperature (°C)	Dipping time	Remarks
A	235±5	5.0±0.5 (2±0.2)	Wave solder
B	215±5	10±0.5 (3±0.3)	Reflow

In principle, the test should be carried out for all terminals, unless otherwise specified, but the leads could be thinned out, by bending or cutting them off, when there is risk of formation of solder bridge between leads due to their fine pitch.

Remarks

As for the solder dipping conditions, 2±0.5 second dipping in 235±5°C solder bath is specified in these standards for the sake of realizing compatibility with **IEC 749**. Since the whole body is dipped in the case of such devices as SMD and the like, however, the terminals might not reach the specified temperature, and in such a case it is desirable to carry out pre-heating. Pre-heating should be carried out in conformity with the conditions specified in the detail specifications.

4.5 Removing flux

Remove flux slag in conformity with 2-propanol (**JIS K 8839**) or ethanol (**JIS K 8101**). If necessary, it could be removed by wiping the terminals or the electrode surface with soft cloth moistened with the above alcohols.

4.6 End-point measurement

Visual inspection should be carried out by using the observation apparatuses specified in section **2.3**. The specimen should have 95% or more of the dipped portion object of evaluation covered with solder, should have no concentration of pinholes, voids and other defects at one place, and more over these defects should not account for more than 5% of the overall surface. No plating places in the end of the leads and others should not be included in the judgment.

Terminals thinned out to prevent the formation of solder bridges should be tested with another specimen, and the judgment should be carried out for all terminals. The electrical and mechanical properties should be examined when specified in the detail specifications.

Remarks

1. In addition to the criteria mentioned in section **4.6**, it is recommendable to carry out the evaluation by taking into consideration also the peeling and separation of solder. The following test methods are available in this connection.
   Test Method 401, Terminal Strength Test Method
2. The dipped portions of SMD to be evaluated are shown in **Figures 1** to **5**.

5. INFORMATION TO BE GIVEN THE RELEVANT SPECIFICATIONS

(1) Composition of the solder (When using solders other than the specified ones) [Refer to **3.1**]
(2) Mixing ratio of flux (When using flux other than the specified ones) [Refer to **3.2**]
(3) Degreasing (When required) [Refer to **4.1.2**]
(4) Items and conditions of the initial measurements (when required) [Refer to **4.2**]
(5) Number of terminals to be tested (when required) [Refer to **4.4.2**]
(6) Accelerated aging method (when required) [Refer to **4.3**]
(7) Flux dipping method (when required) [Refer to **4.3**]
(8) Soldering method (When using soldering methods other than the specified ones) [Refer to **4.4.2**]
(9) Solder dipping conditions (When using solder dipping conditions other than the specified ones) [Refer to **4.4.2**]
(10) Pre-heating conditions (when required) [Refer to **4.4.2**]

(11) Removal of flux (When using flux removal methods other than the specified ones) [Refer to **4.5**]

(12) Items and conditions of the end-point measurements [Refer to **4.6**]

6. REFERENCE

(1) Accelerated aging conditions of 60°C 90% RH and 85°C 85% RH were also taken under consideration, but this time they have not been included in the stipulations of the present standards, because the actual using conditions and the acceleration data are not clearly known, and they are issues to be examined in the future.

(2) There are other soldering methods such as infrared ray reflow, vapor phase reflow, etc., but these methods have poor reproducibility because such factors as the temperature of the leads during soldering, the type of circuit board, the type of cream solder material, the lead coplanarity, etc. are involved therein, and as a consequence it is difficult to evaluate the solderability. Such being the case, the solder dipping method was adopted in these standards in view of good reproducibility.

(3) The wetting balance is a method for solderability evaluation, but it was not specified this time in view of its difficult evaluation, and it was postponed as an issue to be examined in the future.

Figure 1 Gull Wing Lead (The evaluation is carried out only at the L, R and B sides)

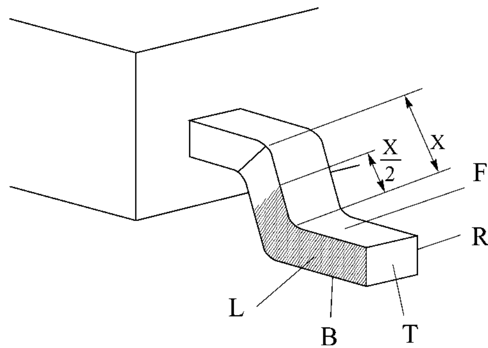


Figure 2 J-Lead (The evaluation is carried out only at the L, R and O sides)

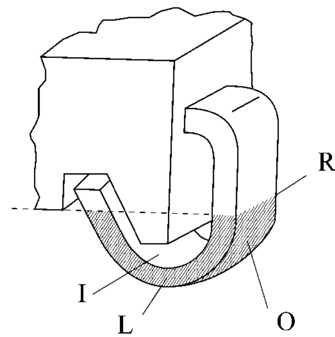


Figure 3 Leadless (The evaluation is carried out at all of the F, B, L, R and T sides)

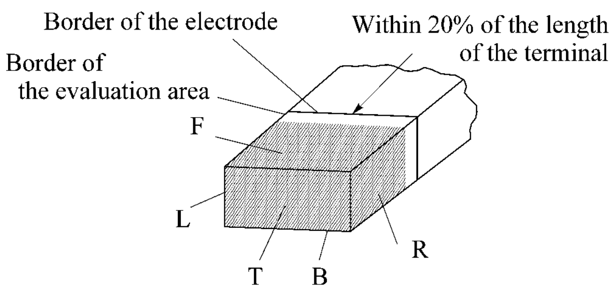


Figure 4 Rectangular Lead (The evaluation is carried out only at the B and O sides)

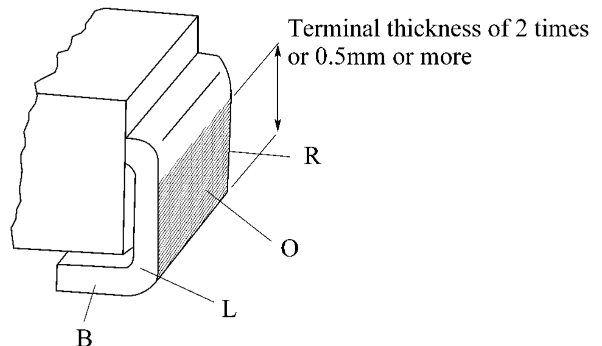
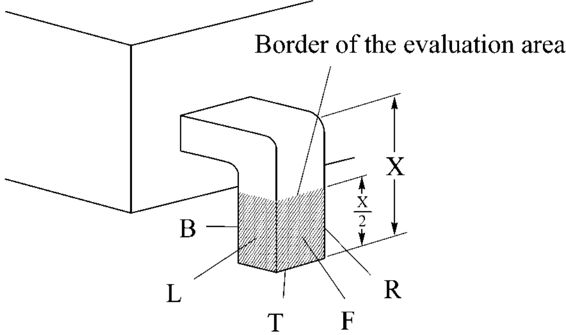


Figure 5 I-Lead
(The evaluation is carried out only at the F, B, L and R sides)



TEST METHOD 304
HUMAN BODY MODEL ELECTROSTATIC DISCHARGE (HBM/ESD)

1. SCOPE

This standard prescribes a procedure of evaluating the endurance of a semiconductor device to human body model electrostatic discharges while the semiconductor device is handled until mounting into electronic equipment.

Remarks:

The charged device model electrostatic discharge test is prescribed in provisional standard **TEST METHOD 305**.

2. TEST EQUIPMENT

This test uses test equipment containing a test circuit shown in Section **2.1** and satisfying conditions of calibration specified in Section **2.2**.

2.1 Test circuit

The test circuit shall satisfy the following specifications:

(1) The test equipment shall consists of a power supply, resistors of the specified resistances, a capacitor of the specified capacitance, switches for switching between charging and discharging, and wires for connecting these components in accordance with the basic test circuit shown in **Figure 1**.

(2) The protective resistor for charging R_1 should have a resistance of 1MΩ to 10 MΩ and shall endure the test voltage. However, when the requirements of calibration specified in Section **2.2** are satisfied, the resistance of the protective resistor R_1 can exceed 10MΩ.

(3) The resistance of the resistor R_2 shall be 1 500Ω±1%.

(4) The capacitance of the capacitor C shall be 100pF±10% and shall endure the test voltage.

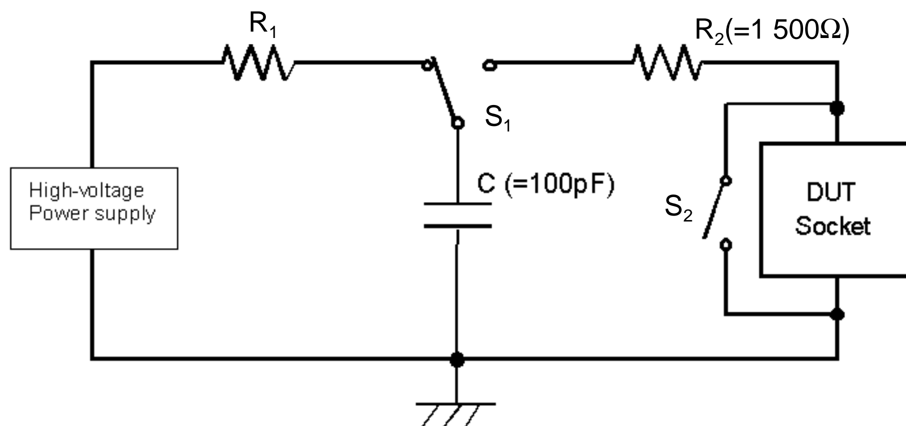
(5) The switch S_1 shall be a mercury relay or an equivalent switch without chattering and shall endure the test voltage. The bypassing switch S_2 shall endure the test voltage.

Remarks:

The capacitance of the capacitor C (100pF±10%) contains parasitic capacity of the wiring and measurement equipment. And current waveform shall meet each later described parameter after considering these capacity.

The switch S_1 should be of one transfer contact type or two normally-open contact types. The switch S_2 should be of the normally close contact type. Wires, sockets, and parts for safety and automation which are not visible in the basic circuit should be minimized to avoid influence on the electric characteristics of the basic test circuit and should satisfy the requirements for calibration specified in Section **2.2**. To satisfy the requirements, the basic test circuit can be added with a filter circuit for suppressing harmonic components.

Figure 1 Test Circuit (Basic)



2.2 Calibration of the test equipment

The test equipment shall be calibrated in the following procedures:

(1) As shown in **Figure 2**, prepare two kinds of jumpers to short-circuit the output terminals of the test apparatus (such as terminals of the socket): a jumper for directly short-circuiting the output terminals and jumper containing a resistor of 500Ω±1% connected in series.

Remarks:

The jumpers should be as short as possible. The serial inductance element and the parallel capacitance element of the 500Ω resistor should be as small as possible.

(2) Connect the jumper to the test terminals of the socket.

(3) As shown in **Figure 2**, open the switch S_2 set the switch S_1 to the high-voltage power supply position, and charge the capacitor C at voltage V. Then, set the switch S_1 to the another position to discharge through the test terminals, and measure the discharge current flowing through the jumper with the current probe connected to the oscilloscope. The current probe and the oscilloscope should be in the frequency band of 350 MHz or more. The setting method of voltage V shall be made by the same method as Section **3.2**.

Remarks:

Unless otherwise specified in relevant specification, select 500V, 1 000V, 2 000V, and 4 000V as a test voltage so as to satisfy the range of the test voltage. Calibration should be done in both positive and negative polarities.

(4) Repeat the above procedure using each kind of jumper and measure the rise time t_r, the decay time t_d, the peak current I_p, and the ringing current I_r shown in **Figure 3** to **5**.

(5) The test equipment shall satisfy all items listed in **Table 1**.

Figure 2 Typical equivalent HBM ESD circuit

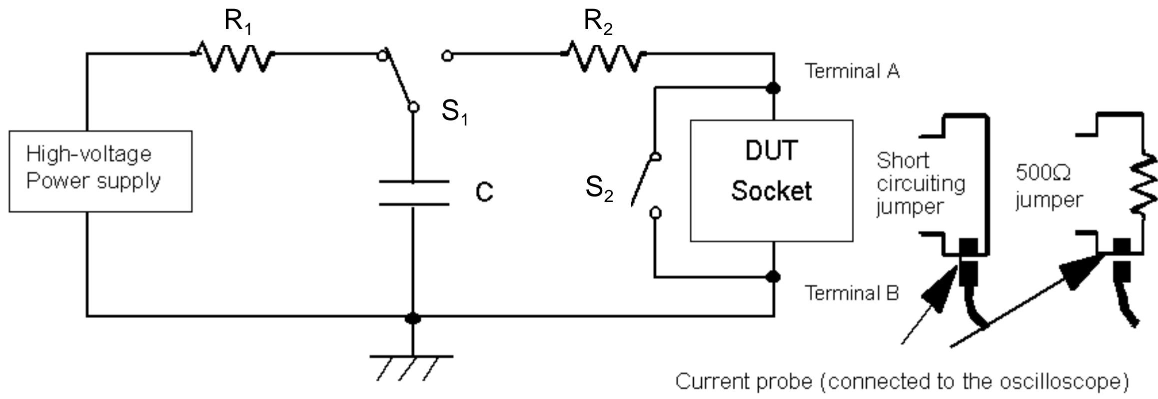


Figure 3 Current waveforms through a short circuiting jumper

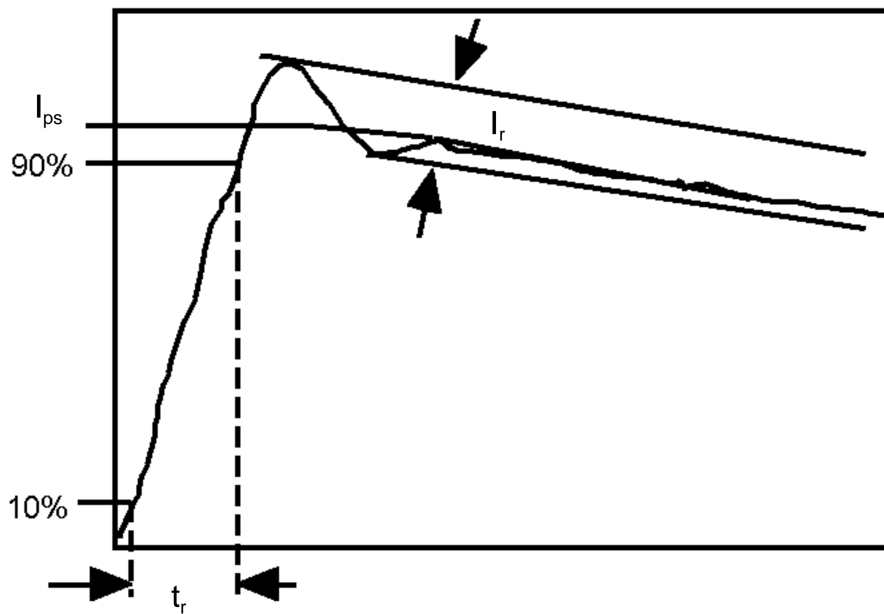


Figure 4 Pulse decay time through a short circuiting jumper

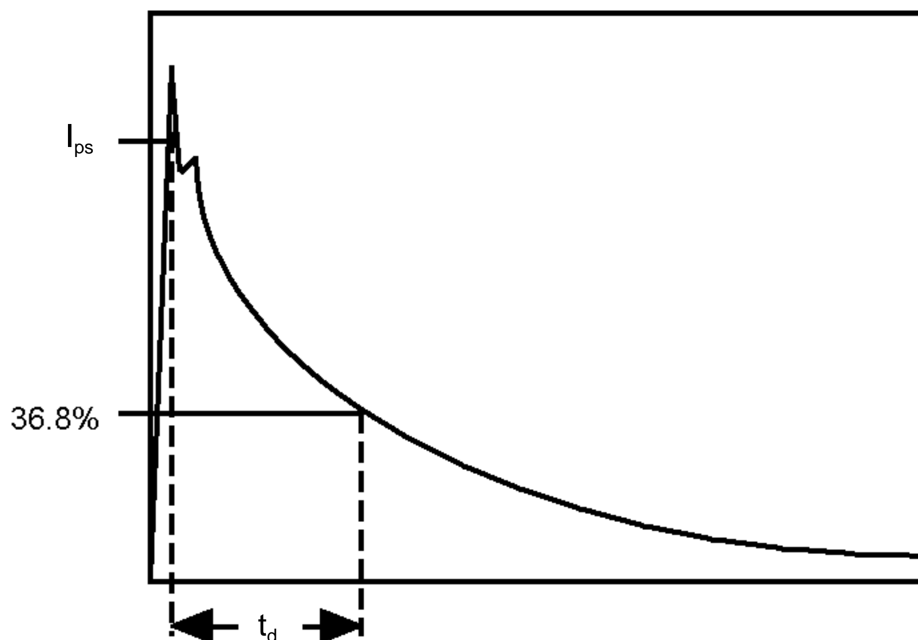


Figure 5 Current waveforms through a 500W jumper

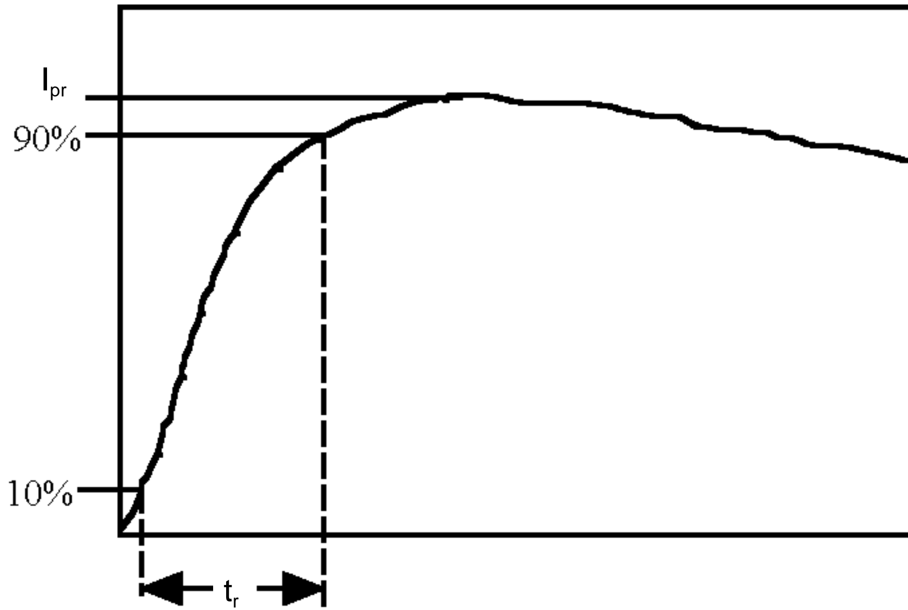


Table 1 Specification of Current Waveform

Item(Unit)	Symbol	Specified values	
		Short-circuiting jumper	500Ω jumper
Rise time (ns)	t_r	2-10	5-25
Decay time (ns)	t_d	150±20	200±40
Peak current (A)	I_{ps}/I_{pr}	See **Table 2**.	See **Table 2**.
Ringing current (A)	I_r	15% or less of I_p	15% or less of I_p

Table 2 Specification of Peak Current

Calibrating Voltage(V)	Specified value of Peak Current (A)	
	Short-circuiting jumper (I_{ps})	500Ω jumper (I_{pr})
500	100%±10% of 0.33	100%+10%, -25% of 0.25
1 000	100%±10% of 0.67	100%+10%, -25% of 0.5
2 000	100%±10% of 1.33	100%+10%, -25% of 1.0
4 000	100%±10% of 2.67	100%+10%, -25% of 2.0

3. TEST PROCEDURE

3.1 Initial measurement

Initial measurement shall be made for items and conditions specified in the relevant specifications.

3.2 Tests

(1) Set the DUT (device under test) in the socket.

(2) Connect the test circuit to the test terminal and the common terminal of the DUT. The test terminal of the DUT can be any other than the common terminal unless otherwise specified. The other terminals are all left open.

Remarks

1. When the DUT is an integrate circuit, the common terminal should be a GND or V_{ss} or V_{cc} power supply terminal of the DUT. [Refer to **2.3.1**]
2. It makes the power terminal which leads inside the IC with the metallic wiring an identical terminal and in the case except it, it treats as another terminal.

(3) Set a test voltage in accordance with the detailed specifications, open the switch S_2, set the switch S_1 to the high-voltage power source position, and charge the capacitor C. Then set the switch S_1 to the specimen position to discharge the capacitor. Repeat this charge and discharge cycle one times, reverse the polarity of the test voltage and repeat the above steps. After discharging is completed, close the switch S_2.

Discharging should be made at intervals of 0.3s or more and at ambient temperature of 25°C±5°C.

Remarks:

1. The recommended test voltage is 1 000V. [Refer to **2.3.2**]

2. No connection terminal shall not be discharged. [Refer to **2.3.3**]

(4) Test every terminal of the specimen one by one in relation to a selected common terminal by changing terminal to be tested and repeating above steps **(2)** and **(3)**. [Refer to **Table 3**]

Table 3 Pin Combinations for Integrated Circuits

Pin Combination	Connect Individually to Terminal A	Connect To Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, Except First power pin(s)	First power pin(s)	All pins except Pin under test and First power pin(s)
2	All pins one at a time, Except Second power pin(s)	Second power pin(s)	All pins except Pin under test and Second power pin(s)
3	All pins one at a time, Except Nth power pin(s)	Nth power pin(s)	All pins except Pin under test and Nth power pin(s)

Remarks:

The measurement specified in Section **3.3** can be performed at the end of testing on each terminal.

(5) The number of the examination samples

It examines the number which was prescribed by the individual standard.

3.3 Final measurement

Final measurement shall be made for items and conditions specified in the relevant specifications.

4. INFORMATION TO BE GIVEN IN THE RELEVANT SPECIFICATIONS

(1) Voltage for calibration (When voltage is different from specified one) [Refer to **2.2(3)** Remarks]

(2) Items and conditions of initial measurement [Refer to **3.1**]

(3) Combination of terminal to be tested (When combination is different from specified one) [Refer to **3.2(2)** and **(4)**]

(4) Conditioning of terminal except for test terminal (When conditioning is different from specified one) [Refer to **3.2(2)** and **(4)**]

(5) Test voltage [Refer to **3.2(3)**]

(6) Number of discharging (when number of discharging is different from specified one) [Refer to **3.2(3)**]

(7) Polarities of test voltage (When polarities are different from specified one) [Refer to **3.2(3)**]

(8) Ambient temperature (When temperature is different from specified one) [Refer to **3.2(3)**]

(9) The number of the examination samples [Refer to **3.2(5)**]

(10) Items and conditions of final measurement [Refer to **3.3**]

REFERENCE 1. REFERENCE TEST METHOD

1. REFERENCE TEST METHOD

1.1 Reason for unabolishing the reference test methods

The standards **IC-121**, **SD-121** (former editions of **ED-4701**), and **ED-4701** (**C-111**) have specified a testing method without using a discharging resistor R_2 (that is, under conditions of R_2=0Ω and C=200pF) (see **Figure 6**). This testing method simulates discharging from human bodies as test method specified in this standard and has been termed "Japanese model" or "Machine model" (in countries outside Japan since the latter half of 1980's) as this test method does not use the discharging resistor.

In this test method revision, the above test method is left unabolished as a reference test method on the premise that it will be abolished in the future because of the following:

(1) The discharging waveform is different from the human body discharging waveform.

(2) The discharging waveform is different from the discharging waveform of machines. The name of "Machine model" is inadequacy because it is easy to bring about misunderstanding.

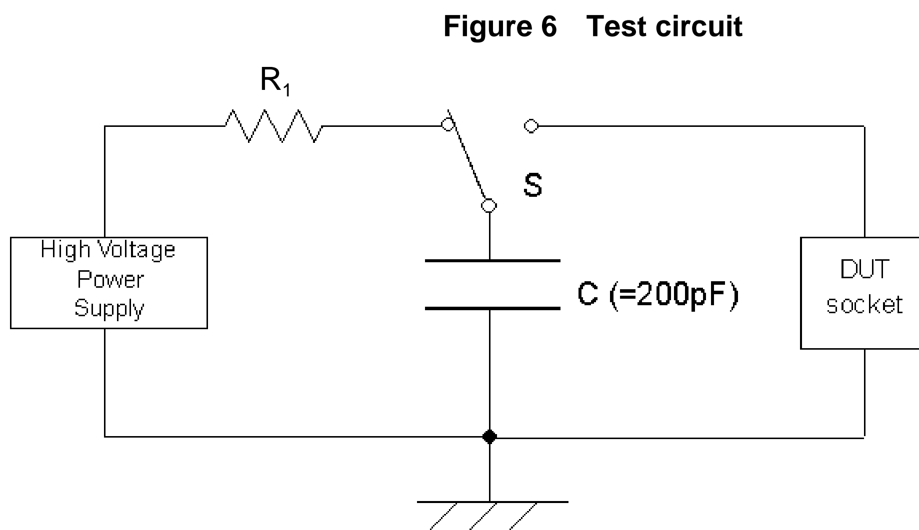
(3) The human body discharging should be part of the cause of electrostatic discharge failure. Two testing methods of simulating human body discharging are not necessary.

1.2 Outline of testing method

1.2.1 Test circuit

As shown in **Figure 6**, the test circuit contains a discharging capacitor of 200pF±10%. The wires connecting the capacitor and a specimen should be as short as possible.

Figure 6 Test circuit



1.2.2 Calibration of the test equipment

The test equipment shall be calibrated in the following procedures:

(1) Prepare two kinds of jumpers to short-circuit the output terminals of the test apparatus (such as terminals of the socket): a jumper for directly short-circuiting the output terminals and jumper containing a resistor of 500Ω±1% connected in series as shown in **Figure 7.**

Remark:

The jumpers should be as short as possible. The serial inductance element and the parallel

capacitance element of the 500Ω resistor should be as small as possible.

(2) Connect the jumper to the test terminals of the socket.

(3) As shown in **Figure 7**, open the switch S_2 set the switch S_1 to the high-voltage power supply position, and charge the capacitor C at voltage V. Then, set the switch S_1 to the another position to discharge through the test terminals, and measure the discharge current flowing through the jumper with the current probe connected to the oscilloscope. The current probe and the oscilloscope should be in the frequency band of 350MHz or more.
Unless otherwise specified, the discharge current should be measured at 100V, 200V and 400V if use a short circuiting jumper, and at 400V if use 500Ω jumper as shown in **Table 4** and **5**.

(4) Read peak current (I_p), ringing current (I_R)(short circuiting jumper only), current after 100ns (I100) (500Ω jumper only), resonance frequency ($1/t_{fr}$) (short circuiting jumper only). (See **Figure 8** and **9**)

(5) The test equipment shall satisfy all items listed in **Table 4** and **5**.

Figure 7 Calibrating circuit

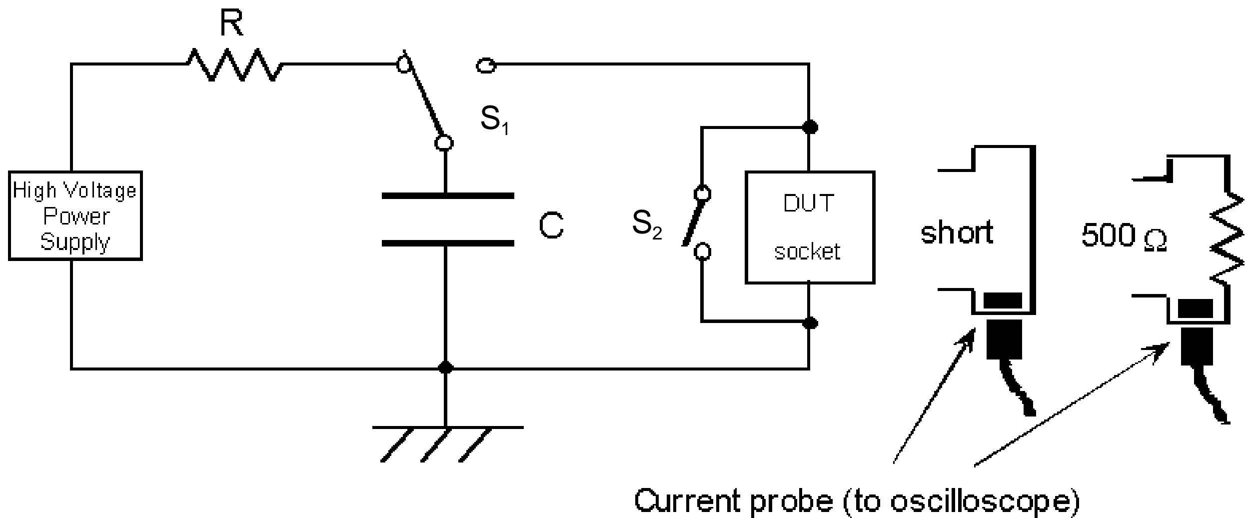


Table 4 Specification of current waveform (short circuiting jumper)

Item (unit)	Symbol	Calibration voltage (V)		
		100	200	400
Peak current (A) Note 1	I_{prl}	1.45-2.0 Note 2	2.9-4.0 Note 2	5.8-8.0 Note 2
Ringing current (A)	I_R	≤30% of I_{prl}	≤30% of I_{prl}	≤30% of I_{prl}
Resonance frequency (MHz)	$1/t_{fr}$	11-16	11-16	11-16

Note 1 : The value including a ringing current.

Note 2 : The theoretical peak current is 1.5A at 100V, 3.0A at 200V and 6.0A at 400V.

Table 5 Specification of current waveform (500W jumper)

Item (unit)	Symbol	Calibration voltage (V)
		400
Peak current (A)	I_{pr}	$\leq I_{100}$ x 4.5
Current after 100ns (A)	I_{100}	0.29±20%

Figure 8 Calibrating waveform (short circuiting jumper, 400V)

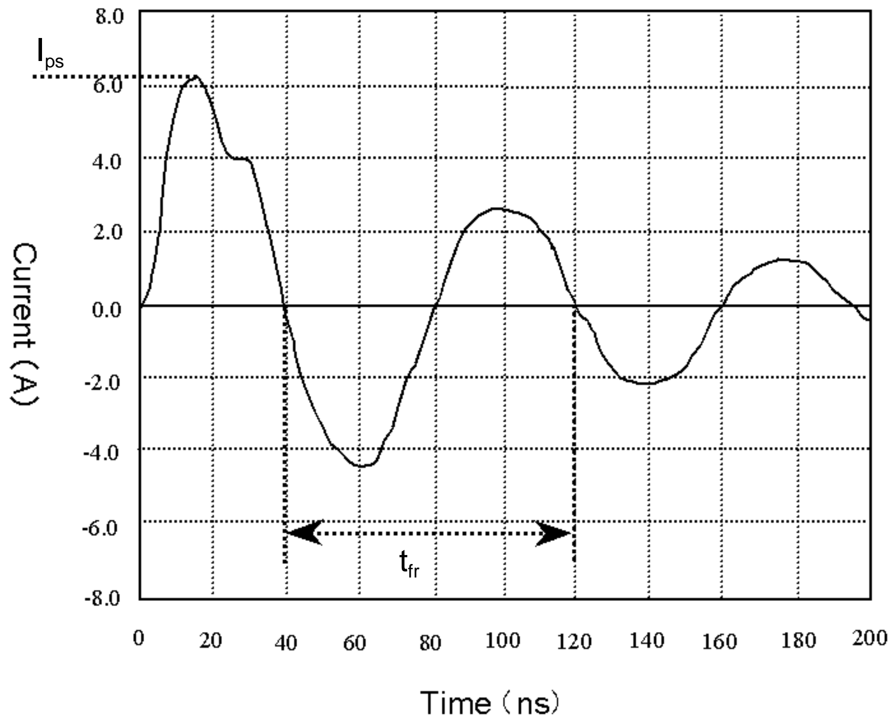
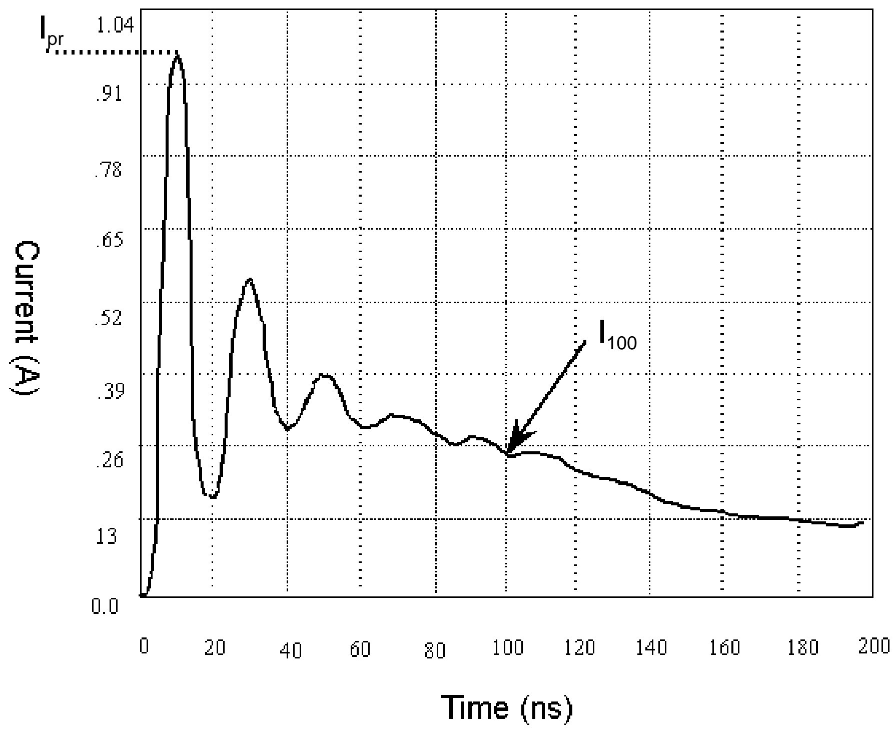


Figure 9 Calibrating waveform (500W jumper, 400V)



1.2.3 Test procedure

The test procedures are the same as those specified in Section **3** but discharging time is only one for positive and negative. The standard test voltage is 150V. The discharging duration is 0.3s or over.

REFERENCE 2. SUPPLEMENTARY MATTERS RELATED TO THE TEST METHOD

1. HUMAN BODY MODEL

1.1 The purpose of the revision

With revision of IEC which is situated on higher rank of the Japan Electronics and Information Technology Industries Association (**JEITA**)'s standard **ED-4701** (established in 1992) (abolishment) "Environmental and Endurance Test Methods for Semiconductor devices", it reconsidered the standard.

Because the revision of **IEC** is done by the origin in **JESD22**, It revised while comparing with the contents which are prescribed by **JESD22-A114-B**.

1.2 The process of the deliberation

It deliberated this method by the Group A of the Semiconductor Devices Quality and Reliability subcommittee and three extraordinary members of a committee who invited from the ESD committee of Reliability Center for Electronic Components of Japan (RCJ) in October and December, 1999 and in February, April, June, August and October, 2000.

1.3 The item which was made a problem while deliberating

1.3.1 About the combination of the examination terminal

The test method which makes the terminal which is not a power a common terminal is prescribed in **JESD22-A114-B**.

When the discharge current flows among the optional terminals of the semiconductor, it is assumed that the a lot of currents flow through the power terminal (GND, Vss, Vcc) via the substrate or Well.

Therefore, it makes a common terminal a power terminal like the past.

Therefore, it decided to do the examination the common terminal of which is Non-supply pin which is prescribed in JESD according to need. [Refer to **Table 1**]

It makes the power terminal which leads inside the IC with the metallic wiring an identical terminal and in the case except it, it treats as another terminal.

Table 1 Pin Combinations for Integrated Circuits

Pin Combination	Connect Individually to Terminal A	Connect To Terminal B (Ground)	Floating Pins (unconnected)
4	Each Non-supply pin, One at a time	All other Non-supply Pins collectively Except Pin under test	All power pins

Remarks:

It makes a terminal except the power terminal Non-Supply terminal.

1.3.2 Classification

In **JESD22-A114-B**, a class is divided as follows, Class 0:250 volts or less, Class 1A: Equal to or more than 250 volts and 500 volts or less, Class 1B: Equal to or more than 500 volts and 1 000 volts or less, Class 1C: Equal to or more than 1 000 volts and 2 000 volts or less, Class 2: Equal to or more than 2 000 volts and 4 000 volts or less, Class 3A: Equal to or more than 4 000 volts and 8 000 volts or less, Class 3B: Equal to or more than 8 000 volts.

But 1 000 V is recommended without dividing a class from the following reason by **JEITA**.

(1) It judges that the trouble by Human Body discharge doesn't occur if being equal to or more than 1 000 V from the results from the past. For example, **IEC 61340-5-1/TR2** defines the IC of HBM 100 volts as being ESDS (Electrostatic discharge sensitive devices). On the other hand, 1 000v has a margin sufficiently.

(2) Even if it goes in the small class division, there is not a treatment regulation which corresponded to this.

1.3.3 The discharge to the no connection terminal

The No connection terminal which isn't connected with the inside by the metallic wiring doesn't examine in the discharge for the following reason. But, the terminal which is connected with the inside by the metallic wiring and is defined as being NC terminal examines in the discharge.

(1) A terminal next is sometimes destroyed when examining No connection terminal which isn't connected with the inside by the metallic wiring in the discharge. It is to occur to discharge at the terminal next by the electric charge which was stored up in the wiring capacity to the No connection terminal of the IC from the discharge resistance. It isn't appropriate in discharge examination which depended on the test machine.

(2) It is provided that it doesn't discharge by the No connection terminal in **JESD22-A114-B**.

2. MACHINE MODEL

2.1 The purpose of the revision

Machine model have been said to contain the following problems.

(1) The test results of this method do not match actual failure modes and rates on actual environment.

(2) This test method is a human body model ESD test method because the capacitance of a human body is about 200pF, and features that the testing can be done by low test voltage as the test circuit contains no discharging resistor.

(3) In some countries outside Japan, this testing method is termed "Machine model" as it contains no discharging resistor but it is off the point.

(4) The discharging current of metals contains a waveform similar to CDM.

(5) The definition of this testing method is ambiguous and not concrete.

(6) The test results are greatly affected by types of test equipment.

(7) Methods and conditions of calibration are not defined.

(8) The discharging current is determined by the inductance of wires used in the test circuit. Its waveform is a damping oscillation waveform which rarely generates in actual electrostatic discharging.

(9) There is no ground for definition of a discharge waveform.

(10) The resistance to electrostatic discharge of recent semiconductor devices have become much greater than those of semiconductor devices existing when this test method had come into wide use and most recent semiconductors can endure electrostatic discharge of 100V. The recent test method is performed by test voltages of 150V to 200V, but these test voltages are too high possibly assuming troubles which will never happen in actual environments. This tendency is also applicable to HBM.

Judging from the above, this testing method is going to be revised keeping the following notices in mind:

(1) The testing method should be defined so actually and concretely that it may be applicable to automated test equipment.

(2) HBM is preserved as a human body model electrostatic discharge test method and two calibrating conditions are defined in reference to documents, data offered by committee members, **JEDEC JESD22-A114-B**, **MIL-STD-883E** METHOD3015.7, ESD STM5.1 , and the results of questionnairing conducted on test equipment manufacturers.

(3) Although Machine model has some problems such as a mismatching with actual electrostatic discharge failures of semiconductor devices, it is preserved as a reference testing method on the premise that it will be abolished in the future. (See Section **5.1**) In case perform this test as a reference test, the waveform should be meet the prescription, so the calibration method has been clarified in this revision. The parasitic inductance is assumed 750nH. The peak current if **Table 4** is widening the width of prescription, because it is including the ringing current.

The test device needs to be produced to refer the theoretical peak current . (See **Note 2** of **Table 4**)

TEST METHOD 305 (PROVISIONAL STANDARD)
CHARGED DEVICE MODEL ELECTROSTATIC DISCHARGE (CDM/ESD)

1. SCOPE

The standard prescribes procedures of charged device model electrostatic discharge test to evaluate sensitivity of integrated circuits to electrostatic discharges that such integrated circuits are exposed to before they are installed in an electronic equipment.

Remarks

This standard is under discussion in committee, therefore this is still provisional. The content is the same as **EIAJ EDX-4702** (Obsolete).

2. DEFINITION OF TERMS

The following terms used in the standard and relevant specifications are defined as shown below.

(1) Specimen: Semiconductor device submitted to testing.

(2) Initial measurement: Measurements made on the specimen prior to the test.

(2) Final measurement: Measurement made after the test.

(3) Ambient temperature: The temperature of air around the specimen.

3. TEST EQUIPMENT

The testing equipment which is designed on the basis of testing circuits described in Section **3.1** shall meet the calibration conditions specified in **3.3**.

3.1 Test circuits

The testing equipment must meet the following specifications.

(1) As shown in Figure 1, the specimen shall be set on an insulating sheet attached to a metal p1ate, The metal p1ate must be large enough for the specimen and be grounded or connected to a stable potential. As shown in **Figure 2**, the metal p1ate can consist of sections each having a different potential.

Reference:

The insulating sheet should be 1.0±0.2 mm thick, the dielectric constant 2.0±0.5, volume resistively 1 x 10^{15} Ωm or more and the withstand voltage must be larger than the testing voltage.

(2) The metal discharge bar shall maintain ground potential before discharges are made.

Reference 1 :

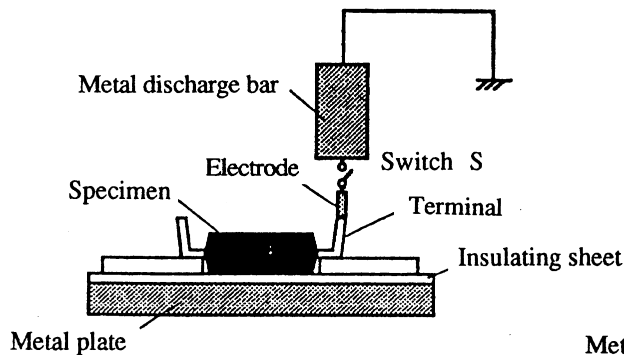
The metal discharge bar shall be connected to ground with a wire (connect the wire to the grounding connection on the housing of the testing equipment).

Reference 2:

The testing equipment shall meet the calibration values given in Section **3.3** by changing the size and configuration of the metal discharge bar.

Figure 1 Testing circuit (Basic circuit for discharge path)

(a) A discharge is caused by closing the switch



(b) A discharge is caused by bringing the metal discharge bar close to the terminal

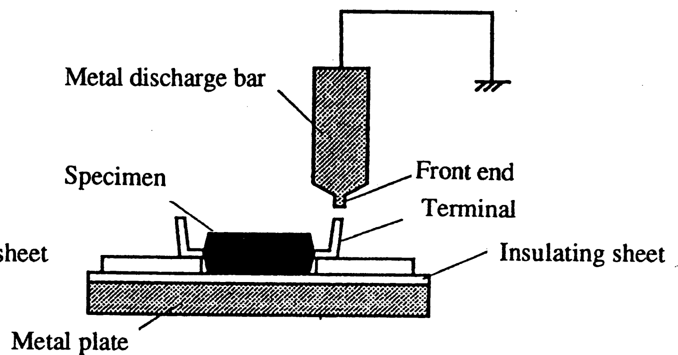
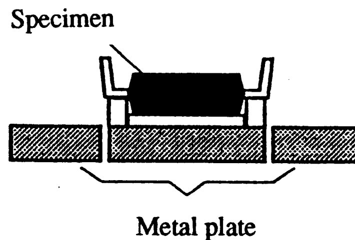


Figure 2 Metal plate consisting of several sections



(3) As shown in **Figure 3**, all the terminals of the specimen can maintain the test potential (the electric potential prescribed for the test). When a high-voltage power supply is to be connected to the terminals of a specimen via a wire, a withstand voltage resistor (R_1) that can endure the test voltage shall be connected in series between the power supply and the terminals. Resistor R_1 should have a resistance in the range of 10MΩ to 100MΩ, but it could be greater as long as it meets the conditions prescribed in Section **3.3**. When a high voltage power supply is connected to the terminals of the specimen via an electrode, a resistor (R_2) with a resistance in the range of 1MΩ to 10MΩ shall be connected in series near the electrode.

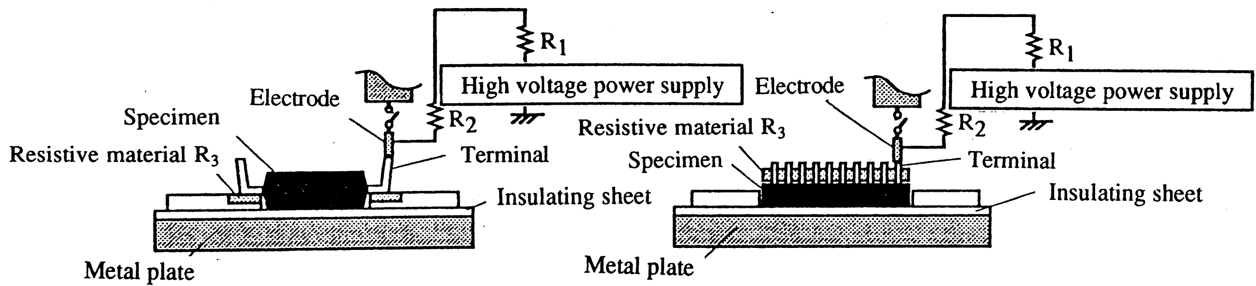
A resistive material (R_3) shall be connected to all the terminals of the specimen for the purpose that potentials of all the terminals coincide with the test voltage. The volume resistively of resistive material R_3 shall be 1×10^4 Ωm to 1×10^8 Ωm.

Reference:

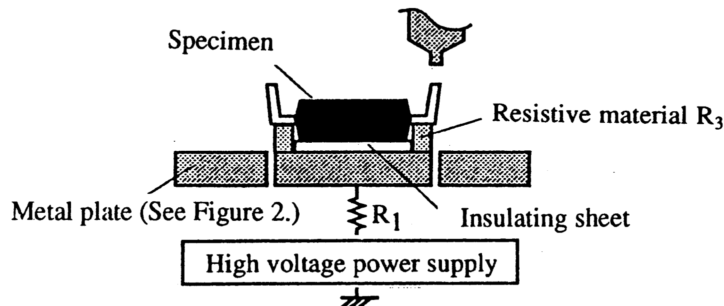
Position R_2 near the electrode to prevent the effect that the charges in the wiring may have during discharges.

Figure 3 Example of charging method for specimen

(a) Examples of charging method that specimen is charged through test terminal



(b) Example of charging method that specimen is charged by metal p1ate and resistive material



(4) The electrode in **Figure 1 (a)** and the front end of the metal discharge bar in **Figure 1 (b)** can be in contact with the terminal of the specimen.

(5) The switch used in **Figure 1 (a)** must be able to withstand the test voltage.

Reference:

A mercury relay is recommended in high-voltage switches. The contact resistance and contact capacity must be relatively low.

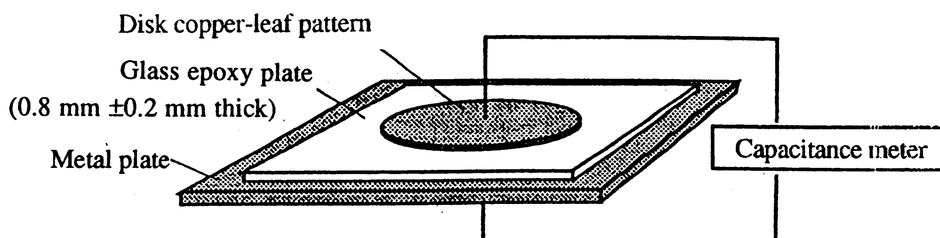
3.2 Calibration modules

A calibration module consists of a 0.8±0.2 mm thick glass epoxy plate onto which a disk copper-leaf pattern has been pasted. The dielectric constant of the glass epoxy plate should be 4.5±0.5 and the copper-leaf pattern should be gold-plated.

Place the calibration module on a metal p1ate that is larger than the module (see **Figure 4**) and use a capacitance meter permitting readings of 100 kHz to 1 MHz to measure it.

Two types of calibration modules should be made: a 4.0±0.2 pF and a 30±1 pF.

Figure 4 Procedure for measuring capacitance of a calibration module



3.3 Calibration of test equipment

Use the following procedures for calibrating testing equipment (see **Figure 5**).

(1) Clean the insulating sheet and the calibration module using isopropanol. Place the calibration module prescribed in Section **3.2** on the insulating sheet.

(2) Maintain the potential of the calibration module according to the procedures given in Section **4.2**. Unless otherwise specified, the potential should be a value of 500 or 1000V both for the plus and minus polarity to meet the test voltage range.

(3) Perform a discharge from the calibration module to the metal discharge bar according to the procedures given in Section **4.2**. Measure current I_{cal} that flows from the calibration module to the metal discharge bar. Use an oscilloscope with a bandwidth of more than 1 GHz (3.5 GHz or more is recommended).

Reference:

Since the discharge current exceeds the 1 GHz bandwidth. the current detector and the measuring circuits have to be calibrated to operate within this range. If the required characteristics cannot be obtained, the measurement value has to be corrected (see Section **6.1** and Appendix Section **3.8**).

(4) Derive the t_r, t_d, I_{p1}, I_{p2} and I_{p3} values given in **Figure 6** using the measured waveform.

(5) The t_r, t_d, I_{p2} and I_{p3} values derived from the measurement shall meet the values in **Table 1**. Peak current I_{p1} shall meet the values given in **Table 2** in Section **6.1**.

Reference:

Peak current I_{p1} tends to reach saturation level during discharges in case of the high voltage and aerial discharge (see **Figure 1 (b)**), and may therefore not meet the specified value. The testing equipment must be used within the limits of the testing voltage where peak current meets the specified values.

Figure 5 Example of calibration method of testing equipment

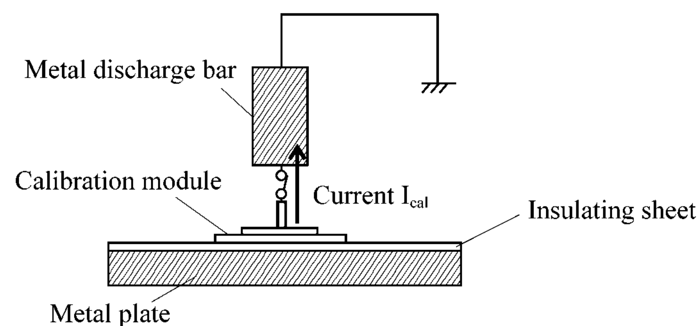


Figure 6 Current waveform

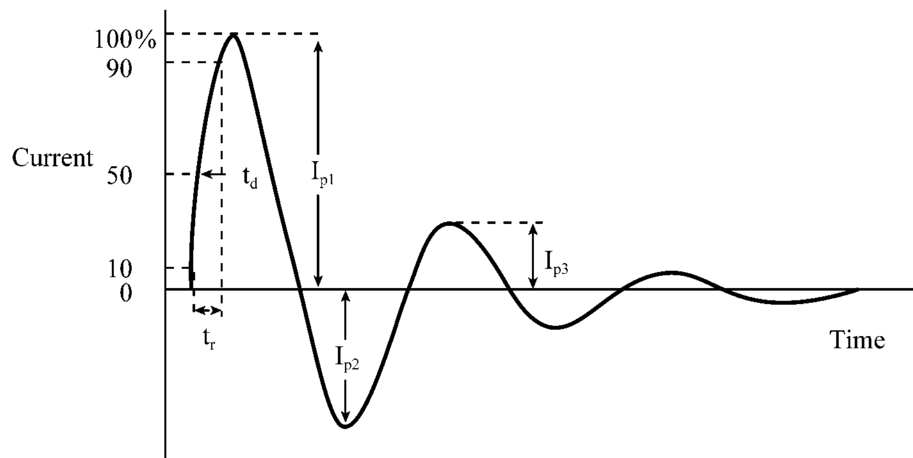


Table 1 Specified current waveform

Item (unit)		Symbol	Specified values	
			4 pF module	30 pF module
Rise time	(ps)	t_r	200 or less ([1])	250 or less ([1])
Pulse width	(ps)	t_d	400 or less	700 or less
Peak current	(A)	I_{p1}	(see Table 2)	(see Table 2)
Undershoot current	(A)	I_{p2}	Less than 50% of I_{p1}	Less than 50% of I_{p1}
Overshoot current	(A)	I_{p3}	Less than 25% of I_{p1}	Less than 25% of I_{p1}

Note([1]): This rise time value is obtained on a 3.5 GHz oscilloscope. This value is close to the measurement limit of a 1 GHz oscilloscope.

4. TEST PROCEDURE

4.1 Initial measurement

Perform the measurements according to the parameters and conditions specified in the relevant specification.

4.2 Tests

(1) Place the specimen on the insulating sheet. The ambient temperature during testing shall be 25°C±5°C.

(2) Connect all the terminals of the specimen to resistive material R_3. In **Figure 1 (a)**, connect the electrode to the terminal of the specimen that is to be tested with switch S opened.

(3) Set the power supply to the testing voltage specified in the relevant specification and make sure that the potential in all the terminals of the specimen maintains the testing voltage.

Reference:

A testing voltage of 500 V is recommended.

(4) Close switch S in **Figure 1 (a)** and in **Figure 1 (b)**, bring the front end of the metal discharge bar close to the terminal to be tested of the specimen to case discharge between the specimen and the metal discharge bar.

Reference:

Closely watch the contact between the electrode and the terminal of specimen in **Figure 1 (a)** and the contact between the front end of the metal discharge bar and the terminal of specimen in **Figure 1 (b)** during the test.

(5) Unless otherwise specified in the relevant specification, one discharge is to be performed. When multiple discharges are to be made, repeat the instructions given in steps **(3)** and **(4)**. However, there shall be an interval of 0.1 seconds or more between discharges.

Reference:

Reverse the polarity of the testing voltage and perform step **(5)** if it is specified in the relevant specification.

(6) Perform steps **(2)** to **(5)** for the next terminal and repeat this procedure to test all the terminals. **(7)** Reverse the polarity of the testing voltage and perform steps **(2)** to **(6)**. Reference: When step **(6)** is completed, perform intermediate measurements or perform step

(7) on another specimen.

4.3 Final measurement

Perform the measurements according to the parameters and conditions specified in the relevant specification.

5. INFORMATION TO BE GIVEN IN THE RELEVANT SPECIFICATIONS

(1) Voltage used for calibration [Refer to **3.3**]

(2) Parameters and conditions of initial measurement [Refer to **4.1**]

(3) Ambient temperature during test (when other than specified) [Refer to **4.2 (1)**]

(4) Test voltage [Refer to **4.2 (3)**]

(5) Number of discharges (when other than specified) [Refer to **4.2 (5)**]

(6) Interval between repeated discharges (when other than specified) [Refer to **4.2 (5)**]

(7) Procedures for reversing the testing voltage (when other than specified) [Refer to **4.2 (5) (7)**]

(8) Parameters and conditions of intermediate measurements (when other than specified) [Refer to **4.2 (7)**]

(9) Parameters and conditions of final measurement [Refer to **4.3**]

6. REFERENCE

6.1 Provisional measurement procedure for calibrating test equipment and specification

Section **3.3** specifies the current that is to be measured to calibrate the test equipment. As shown in **Figure 5**, this is the current I_{cal} which flows between the calibration module and the metal discharge bar. The problem is that current test equipment is not configured to measure the current I_{cal} and requires modifications to do so.

As a result, until the test equipment is modified, a calibration module with a disk copper pattern on each side must be used. **Figure 7** shows how to perform measurements using the provisional procedure. The calibration module is measured separately (i.e. it is not placed on the metal p1ate) and must meet the specified capacitance.

The measured waveform must meet the values given in **Table 1**.

This standard does not require a measurement of peak current I_{p1}. The reason for this is that it is derived from current I_{cal} that flows between the calibration module and the metal discharge bar and the provisional procedure cannot produce an accurate measurement of this value. **Table 2** shows the range of peak current I_{p1} for all test equipment used in Japan. This value, value of current I_{cal}, is close to the peak current I_{p1}. The peak current I_{p1} estimated using the provisional procedure is to be used in carrying out maintenance.

In the future, the wide-ranging values of current I_{cal} given in **Table 2** will be revised to establish a standard that will replace the provisional standard.

Reference:

It is often difficult to obtain a correct measurement of peak current I_{p1} due to the effect of frequency characteristics of current detectors, oscilloscopes and other measurement equipment. Thus when calibration of measurement equipment is not possible, use the procedure described in Appendix Section **3.8**.

Figure 7 Example of provisional calibration method for testing equipment

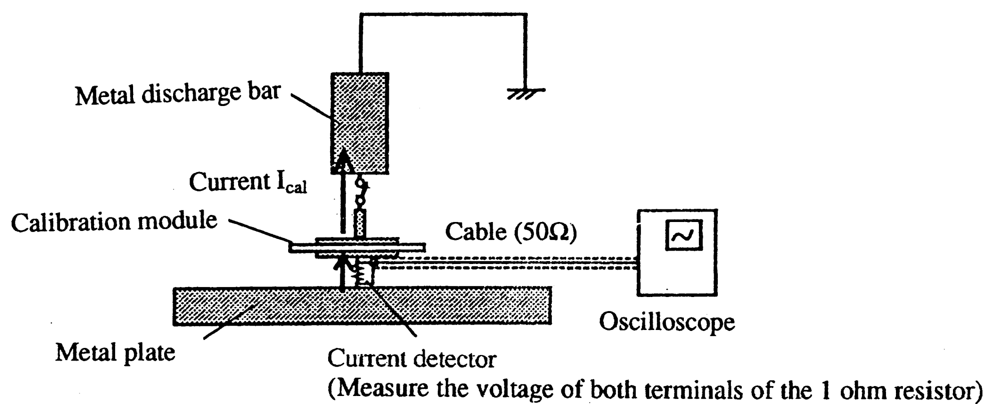


Table 2 Range of peak current I_{p1} for currently used testing equipment

Calibrating voltage ([2]) (V)	Range of I_{p1} (A)	
	4 pF module	30 pF module
500	1.0 ~ 3.0	3.0 ~ 6.0
1000	2.0 ~ 6.0	6.0 ~ 12.0

Note ([2]): The I_{p1} value is proportional to the calibration voltage value. When the calibration voltage value is exceeds 1000 volts, the I_{p1} value must be proportional to the value in the table.

6.2 Alternative tests (small capacitance method)

This section describes procedures for testing small capacitance method, an alternative procedure to the charged device model testing procedure.

6.2.1 Test equipment

The test equipment used should comprise the test circuits prescribed in step (1) below and must meet the calibration conditions set out in step (2) below.

(1) Test circuits

The test circuits must meet the following parameters.

(a) As indicated in **Figure 8**, charge capacitance C so that it is possible to allow a discharge between capacitance C and the terminal of the specimen.

(b) Capacitance C consists of a metal bars M_l and a metal sylinder M_2 and their value should be 10 pF or less. The distance between discharge switch S_1 and metal sylinder M_2 that conducts the charge to the specimen should be as short as possible. Limit resistor R_1 of the charge current should be in the range of 10 MΩ to 100 MΩ.

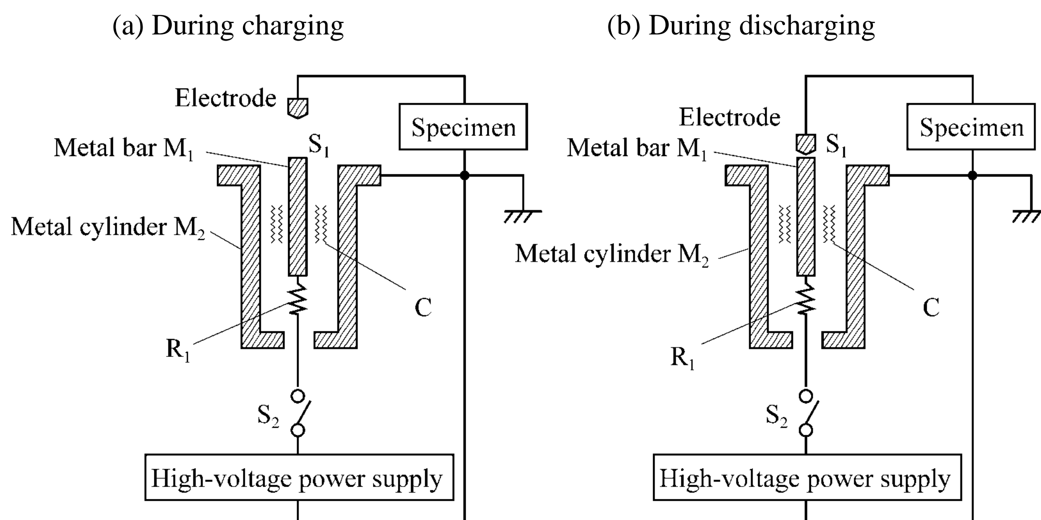
Reference:

Do not use a capacitor for capacitance C. In **Figure 8**. capacitance C is created by metal bar M_l, and metal sylinder M_2, placed on the outside. The value of the capacitance should be as small as possible. To reduce capacitance and inductance along the discharge path, switch S_1 and capacitance C should have an integrated configuration.

(c) Switch S_1 and S_2 should have a withstand voltage that is high enough for the testing voltage.

Figure 8 Example of basic testing circuit

(a) During charging (b) During discharging



(2) Calibration of test equipment

Perform the following procedure to calibrate the test equipment.

(a) Before inserting the specimen (the state of the testing equipment is shown in **Figure 9**), short-circuit the discharge terminal of the test equipment and the common terminal and connect a 1Ω resistor in the discharge path.

(b) Connect both ends of the 1Ω resistor to an oscilloscope. Use an oscilloscope with a waveband of more than 1 GHz (3.5 GHz Or more is recommended) .

Reference 1 :

In the small capacitance method a capacitance equal to the specimen is formed outside of the specimen and charges built up in this capacitance are discharged to the specimen. This test method differs from the charged device model method. As described above, the test equipment is not calibrated using a calibration module but with a 1Ω discharge current measurement resistor.

Reference 2 :

Either solder the cables to the ends of the 1Ω resistor or use special metal clips to ensure good connection.

(c) Set the voltage to 500 V or 1000 V and measure the discharge current.

(d) Derive the t_r, t_d and I_p Values from the measured waveform (see **Figure 10**).

(e) The derived t_r, t_d and I_p Values shall meet the standard values given in **Table 3**.

Reference:

It is often difficult to obtain a correct measurement of peak current I_p due to the effect of frequency characteristics of current detectors, oscilloscopes and other measurement equipment. It is therefore recommended practice to correct measured values using the method described in Description **3.8** before comparing measured values with the values listed in **Table 3**.

Figure 9 Circuit for measuring discharge waveform

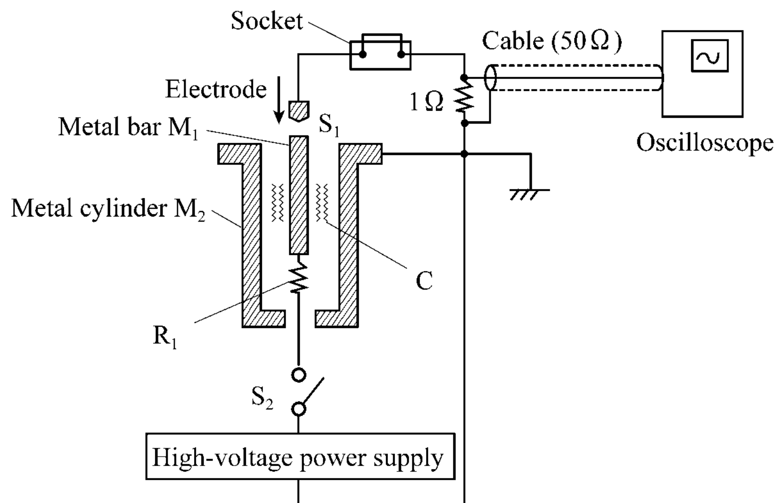


Figure 10 Discharge waveform

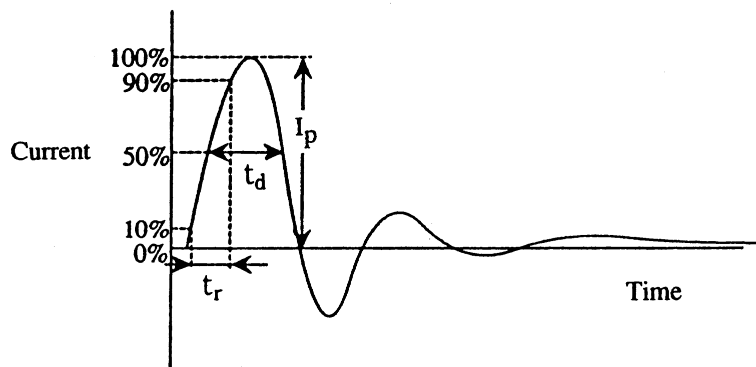


Table 3 Discharge waveform

Items (Unit)	Symbol	Specified values	
		3.5 GHz or 1.0 GHz ([4])	
		500 V	1000 V
Rise time (ps)	t_r	400 or less	400 or less
Pulse width (ps)	t_d	500 or less	500 or less
Peak current (A) ([3])	I_p	3.5±0.7	7.0±1.4

Note ([3]): The peak current is a corrected value.

Note ([4]): The upper limit of frequency band of the oscilloscope.

6.2.2 Test procedure

(1) Initial measurement

Follow the measurement parameters and conditions specified in the relevant specification.

(2) Test

(a) Insert the specimen in the socket. The ambient temperature at the time of the test shall be 25°C±5°C.

(b) Connect the terminal to be tested on the specimen to the common terminal in the test circuit. Unless otherwise specified in the relevant specifications, perform the test on one terminal that has not been defined as a common terminal. All terminals other than the terminal to be tested and the common terminal shall be left open.

Reference:

The common terminal on a specimen in an integrated circuit is the ground terminal or the power terminal.

(c) Open switch S_1 and close switch S_2. Adjust the test voltage as specified in the relevant specification and charge capacitance C. Then open switch S_2 and close switch S_1 to discharge. Unless otherwise specified in the relevant specification, perform one discharge. When multiple discharges are to be made, repeat the discharges as specified. However, there shall be an interval of 0.1 seconds or more between discharges.

Reference:

If it is specified in the relevant specification, reverse the polarity of the testing voltage and perform step (c).

(d) To test all of the terminals using the common terminal, reconnect the terminals to be tested and repeat steps (b) and (c) Reference: Perform step (3) for each terminal to be tested.

(e) Change the testing voltage and perform steps (b) to (d).

Reference:

When step (d) is completed, perform intermediate measurements or perform step (e) on another specimen.

(3) Final measurement

Perform the measurements according to the parameters and conditions specified in the relevant specification.

6.2.3 Information to be given in the relevant specification

(1) Selecting test method [Refer to **6.2**]

(2) Test voltage used for calibration (when other than specified) [Refer to **6.2.1 (2)**]

(3) Parameters and conditions of initial measurements [Refer to **6.2.2 (1)**]

(4) Combination of test terminals (when other than specified) [Refer to **6.2.2 (2)**]

(5) Processing terminals other than terminal to be tested (when other than specified) [Refer to **6.2.2 (2)**]

(6) Test voltage [Refer to **6.2.2 (2)**]

(7) Times of application (when other than specified) [Refer to **6.2.2 (2)**]

(8) Procedures for reversing the testing voltage (when other than specified) [Refer to **6.2.2 (2)**]

(9) Ambient temperature (when other than specified) [Refer to **6.2.2 (2)**]

(10) Parameters and conditions of final measurement [Refer to **6.2.2 (3)**]

REFERENCE 1. SUPPLEMENTER MATERS RELATED TO THE TEST METHODS

1. PURPOSE OF ESTABLISHMENT

The charged package model electrostatic discharge (ESD) test method is generally recognized as a test method of evaluating sensitivity of semiconductors for ESD in assembling process of electronic equipment. In 1988, when the Electronic Industries Association of Japan (EIAJ) revised the **EIAJ IC-121** Standard (test method 20: ESD test), the Section. "Charge Package Model ESD test method (Draft)" was added to the Description Section. Later in 1992, The **EIAJ IC-121** Standard was merged with the **EIAJ SD-121** to create a new standard, the **EIAJ ED-4701** Standard. In the new standard, the Charge Package Model (Draft) was offered as a reference for Test Method C-111 ESD Test Method. A large number of papers on test methods were published starting from 1988 both in Japan and overseas and as testing equipment became more easily available, standardizing this test method became an urgent need. In 1992 and 1993 the Sub Committee of Semiconductor Devices Reliability deliberations focused on revising the C-111 ESD test method of the **EIAJ ED-4701** Standard.

The charge package model which had been part of the charged device model test method was renamed as the charged device model test method and separated from the human model test method specified in C-111. The purpose of the committee was to establish the **EIAJ ED-4701-1**, C-111A Human Body Model ESD Test, an independent test method with equal rank. A problem with the charged device model test method is its reliance on sophisticated technology to simulate discharges up to several GHz. A number of difficulties especially in calibration technology are not solved. As a result, this test method is established as a provisional standard.

2. PROCESS OF DELIBERATION

The Group A of the Sub Committee of Semiconductor Devices Reliability, an organization operating under the Special Technical Committee on semiconductor Devices Quality and Reliability started deliberations to revise this test method. In conducting the deliberations, the Group A made frequent reports on the progress of the deliberations to the Semiconductor Reliability Sub-committee and the Special Technical Committee on Semiconductor Devices Quality and Reliability to get their approval. The following describes the progress of these deliberations.

June 1992 (Sub Committee of Semiconductor Devices Reliability)

During fiscal 1992, Group A determined that test methods for ESD and latch up should be discussed and organized a new group to handle the deliberations on these subjects.

It was proposed that test conditions B (1.5 kΩ, 100 pF) specification the test method C-111 of **ED-4701** and the charged device model should be the main methods used for ESD test and that test conditions A (0Ω, 200 pF) should be demoted to the level of a reference test.

September 1992 (First deliberation by Group A)

(1) The organization of Group A was discussed.

(2) Three members of the Electrostatic Discharge Control Committee of the Reliability Center for Electronic Components of Japan (RCJ) were chosen as special members of the Group A. The deliberations were set to start in October.

October and November 1992 (Second and third deliberations held by Group A)

In June 1992, the views of all members on the proposals of the Sub Committee of Semiconductor Devices Reliability was summarized and the following basic policies of the deliberations were determined.

(1) Test condition A (0W, 200 pF)

The test conditions should be retained: 1 company

The test conditions should be demoted: 6 companies

The test conditions should be abolished: 1 company

Note:

Test condition A is the Japanese Human Body Model or the Machine Model .

(2) Test condition B (1.5kW. 100 pF)

The test conditions should be retained: 8 companies

(However, some thought that the calibration methods should be revised.)

Note:

Test condition B is the Human Body Model.

(3) Charged device model

Should be established: 6 companies

No comment: 2 companies

On the basis of these results, test conditions A was reduced to a lower rank to prepare for its final abolishment. It was determined that test conditions B should be retained while the calibration methods used would be revised. The charged device model was established as a new test method. These results were reported to the Sub Committee of Semiconductor Devices Reliability who recognized their approval.

January, February, March, April, May, June, August, September 1993 (4th to 11th Group a deliberations)

The technical aspects of documents and data submitted by the members were examined during the 8 deliberations that were held. In September at the 11th deliberation, the small capacitance method was proposed as an alternative to the charged device model method. The committee received the Draft Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model Component Testing EOS/ESD-DS5.3 from the Device Testing Committee of the EOS/ESD Association and these documents were used as reference material in the deliberations.

October, November, December 1993 and January, February, March, April, May 1994 (12th to 19th Group a deliberations)

A total of 8 deliberations were held during which the contents of the test method was discussed.

June 1994 (10th Special Technical Committee on Semiconductor Devices Quality and Reliability)

The final draft was submitted which was established and accepted.

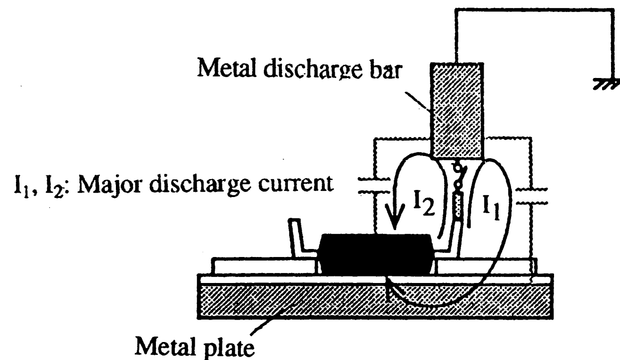
3. PROBLEMS THAT OCCURRED IN DELIBERATION

3.1 Express methods for electrostatic discharges and testing circuits

Since the discharge current of the charged device model is composed of high-frequency elementary current, it flows through the capacitance in or between conductors. The major elementary current of

the discharge current generated by the charged device model consist of elementary current 11 and 12 which flow through the capacitance between the metal discharge bar and the metal p1ate (see Appendix **Figure 1**). Test circuit drawings usually consist of symbols showing resistors and capacitors, but since the configuration and electric characteristics of metal p1ates and metal discharge bars used in the charged device model method are of vital importance, the actual circuits are drawn as shown in Appendix **Figure 1**.

Appendix Figure 1 Major discharge elementary current



3.2 Procedure for holding specimen

In order to ensure the capacitance of the specimen, the specimen has to be held on a metal p1ate. The specimen should not be inserted in a socket since the capacitance of the IC socket and the wires connected to it will be added to the capacitance of the specimen itself. An insulating sheet should be placed between the specimen and the metal p1ate to prevent discharges and leakage current when high voltages are applied.

As stated in steps (1) to (4) below, thin semiconductors are more difficult to charge than thick ones. However, when thin semiconductors are placed on a metal p1ate, their capacitance is larger than that of thick semiconductors and the charged electric charge is greater. The role of the insulating sheet is to prevent the capacitance of thin semiconductors from becoming excessively large. However, the insulating effect is not enough of a corrective so tests of thin semiconductors have to be performed with care.

Thus since thin semiconductors are damaged by low test voltages, it is a common misconception that they are more prone to damages due to static electricity. This is a fact that should be understood in testing thin semiconductors.

(1) In the environment, charged semiconductors are not usually in contact with large metal, but normally some way off. The capacitance of the semiconductor is small and is not dependent on the thickness of the package.

(2) Frictional electrification depends on the material of the package, the speed and force of friction and other factors while the amount of charges has nothing to do with the capacitance of the semiconductor. When thin semiconductors near a large metal is charged by friction, the charged voltage V of a thin semiconductor with a high capacitance C will go down as shown in equation (1). In case of static induction by that a charged material draws near a semiconductor on a large metal, the charge voltage decreases the higher the capacitance of the thin semiconductor.

$$Q=CV \quad \text{....... (1)}$$

(3) A charged semiconductor can come in contact with large metal. As the electric charge Q does not change when the semiconductor is moved, charge voltage V decreases while capacitance C of the semiconductor increases when large metal is brought close (see equation (1)). The larger the capacitance of the thin semiconductor, the lower the charge voltage becomes when the metal is moved close to it.

(4) When a thin semiconductor is placed on conductor, the charge voltage tends to drop through creeping discharge.

3.3 Electric potential and division of metal plates

Since discharge current consists of high frequency current, the test circuit must be equivalent for high frequency discharge current. To ensure this, the test potential of the specimen and the reference potential (potential of ground or the cabinet) of the metal discharge bar have to be maintained right up to the moment of the discharge.

Even if the metal p1ate is connected by wires to the reference potential, potential of the metal p1ate can not hold oneself still as the reference voltage by a single discharge in the GHz band (major elementary current I_1 in Appendix **Figure I**). As a result. if transitory potential overlap in the metal p1ate, the direct current potential do not have to be limited to the reference potential to maintain a stable voltage. As shown in **Figure 2**, even if the metal p1ate consists of several sections, the different pieces are connected capacitance and will still function like a solid metal p1ate.

The charged package model added as a test method draft in the **IC-121** and **ED-4701** standard uses split metal p1ates and the test potential is maintained in the center plate. The metal p1ate consisting of several section produces the same results as other methods using solid metal plates.

3.4 Ground wiring of metal discharge bar

To ensure that the metal charge bar stays at the reference potential (ground or cabinet potential), it has to be connected to the reference potential with a wire (ground wire). If required, connect the ground wire to a resistor in series. The resistor should have a resistance of 10 kΩ or less. The characteristics of the ground wire changes with movements of the metal discharge bar and the wire itself operates as an antenna radiating magnetic noise. The resistor cancels these unstable and unwanted high frequency noise. However, when a high withstand voltage mercury relay is not used in switch S, charges caused by corona discharges will move from the specimen to the metal charge bar making the potential of the metal charge bar unstable so resistors have to be used with care.

Since capacitance connects the metal charge bar, the metal p1ate and the specimen, the major elementary discharge current does not flow through the ground wire, but through the space between the components to the specimen (see Appendix **Figure 1**). The major elementary discharge current influence the major parameters t_r, t_d and I_{p1} shown in **Figure 5** and **Table 1** in the test method. Some of the discharge current (current with a longer wavelength and shorter amplitude than the major elementary current) flow through the ground wire. This current flows after flowing the major elementary current that transmit by the shortest route, and do not affect t_r, t_d and I_{p1}. As shown in **Figure 5** and **Table 1** , they have a slight effect on I_{p2} and I_{p3}, but their effect on test results can be ignored.

3.5 Procedure for maintaining the potential of the specimen

All the terminals of the specimen should be connected to the high-voltage power supply via resistive material R_3 to ensure that they maintain the test voltage despite the following problem.

(1) It is difficult to maintain the potential of the specimen due to the electrostatic induction shown in Appendix **Figure 2**.

(a) In the following equation, the capacitance between the specimen and the metal discharge bar is C_1, the capacitance between the specimen and the metal p1ate is C_2 and the voltage of the high-voltage power supply is V. Equation (2) shows that V_{DUT}, the potential of the specimen, is lower than V.

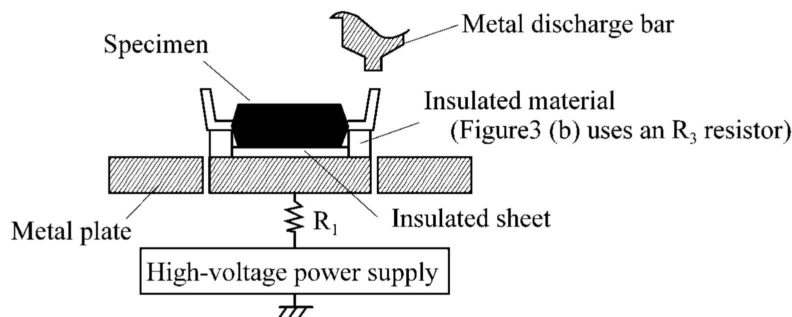
$$V_{DUT} = \frac{C_2 \cdot V}{C_1 + C_2} \qquad \text{....... (2)}$$

(b) When the specimen and the fixture board are contaminated, leakage current may cause the potential of the specimen to drop.

(c) When the specimen is made of plastic, charges from the electrified plastic enters the conductor and causes the potential to fluctuate.

(d) A corona discharge (a small discharge) normally occurs before the discharge. This causes charges to leak from the specimen and lowers its potential. Discharges in air or the use of a floating condition to maintain potential are especially prone to this phenomena and makes the test results unstable.

Appendix Figure 2 Using electrostatic induction to maintain the potential of the specimen



(2) Slight differences in potential between the terminals of the specimen change the electrical characteristics and logical state of the specimen. As these phenomena change the electrical characteristics of the discharge path of the specimen and make other paths, failure mode and the test results would be change. For this reason, all the terminals of the specimen should be connected to resistive material R_3 to maintain the same potential.

The problem pointed out in (1) above was considered in the revision of the IC-121 standard (Charged package model/**Figure 4**) in 1988. when the use of resistor (B), which corresponds to resistive material R_3, was recommended. The problem in (2) occurs when a high-voltage power supply is connected to a specimen and not all the terminals can be connected to the power supply. This causes potential differences in the specimen lowering the stability of the test result and should be corrected by applying a resistive material (R_3) shown in **Figure 3 (a)**.

3.6 Electrostatic discharging procedure

A discharge in air starts with a corona discharge which lowers the potential of the specimen. Electrostatic induction as shown in Appendix **Figure 2** has a tendency to increase this effect. Although the use of a resistive material (R_3) as shown in **Figure 3 (b)** can maintain the potential at fairly stable levels, the potential starts to become unstable at 1000 V or higher voltages. However, the conditions of discharges in air can be made to meet the required conditions if the calibrations described in **3.3** are performed.

3.7 Calibration procedure

The deliberations of the test method showed that specifying the configuration of the metal discharge bar and the dimensions of the metal p1ate (see **Figure 1**) determines the electrical characteristics of the testing equipment and eliminates the need for detailed calibration procedures. Although there are slight differences in dimensions in the testing equipment generally used in Japan, they have similar configuration which makes it possible to ensure a standard testing environment. Still, as standardizing the dimensions and configuration of the testing equipment places restrictions on the development of such equipment, the discharge current waveform was standardized, instead.

Discharges current of the charged device model contains discharges currents of several GHz. Calibrations of this method make accurate measurements of the discharge current indispensable, but there are still a number of problems that have to be solved to make this possible. The following gives the background to the proposed calibration methods and the problems that they entail.

(1) It was first suggested that the capacitance, inductance and resistance of the calibration module used should resemble those of the semiconductor device. However the need for a simple configuration and ease of manufacture led to the use of a copper-leaf disk pattern on a glass epoxy plate as used in EOS/ESD-DS5.3. There are two capacitances: 4.0 pF and 30 pF. The committee decided to follow the recommendations of EOS/ESD-DS5.3.

Since the capacitance of the calibration module is specified, there seemed to be no need to specify the thickness of the glass epoxy plate. However, to ensure the same capacitance, the size of the copper-leaf disk pattern has to be tailored to the thickness of the glass epoxy plate. It also became clear that even if the same capacitance was maintained, the dimensions and configuration of the calibration module affected these characteristics especially in the case of very fast discharges. It was therefore determined that the copper-leaf pattern should be round and that the glass epoxy plate should be 0.8 mm±0.2 mm thick.

(2) The voltage used for calibration has to include the complete range of values of the test voltage. Even if only part of the calibration voltage can be met, a test should be performed in the satisfactory range. Tests at voltages of 1000 V or more require calibration at a voltage that cover the range of the test voltage.

(3) Calibration requires that the current that flow through the terminal of specimen is measured (major elementary current I_1 and I_2 in Appendix **Figure 1**). However, at the time this standard was deliberated, existing testing equipment did not allow measurements of this current and structural modifications were required.

The difficulty of measuring major elementary current I_1 and I_2 made it difficult to determine the calibration conditions, but the parameters in the EOS/ESD-DS5.3 reference materials that could

be measured were adopted (see **Table I**). However, peak current I_{p1} value could not be adopted because of differences in the basic configuration of the testing equipment used in the EOS/ESD-DS5.3. Measurement results derived using the provisional standard method described in Section **6.1** led to the adoption of the conditions given in **Table 2**.

Differences in the frequency characteristics of current detectors, cables, oscilloscopes can affect the peak current I_{p1} value. When current detectors, cables and oscilloscopes cannot be calibrated, the results measured have to be corrected as described in Appendix Section **3.8**.

(4) Since the discharge current produced by this method is a high-frequency waveform of several GHz, the oscilloscopes, current detectors, cables and connectors used in waveform measurement have to be specially designed for operation in this bandwidth.

Currently, 4.5 GHz (3.5 GHz when equipped with a delay line) and 1 GHz oscilloscopes that can measure single pulses are available. An oscilloscope with a bandwidth of 3.5 GHz or better should be used with his method.

Cables and connectors that can be used in bandwidth up to 10 GHz are also available.

When the committee deliberated the standard, there were no current detectors that allowed accurate measurements. Two procedures can be used as a current detector, either a current probe or feeding the current through a 1Ω resistor and reading the drop in potential between the terminals of the resistor. The problem with current probes is that their bandwidth is less than 1 GHz. The slight inductance of a resistor raises impedance at high frequencies causing the amplitude (peak current I_{p1}) of the current to be larger than it should. An additional problem is that the discharge current flowing through the resistor affects the magnetic field to cause reverse power to flow through the cables connected to the resistor which lowers the amplitude. For this reason the cable from the resistors must be connected vertically to the resistor.

The correction method described in Section **3.8** has to be used to compensate for the inability to accurately measure the amplitude due to the use of a resistor.

3.8 Procedures for correcting measurement results

As stated in Section **3.7**, it is quite difficult to ensure accurate measurements of high frequency amplitudes amounting to several GHz with existing measurement systems (current detectors, cables and oscilloscopes). Nor are there any procedures for making a comprehensive calibration of the measuring equipment. The Sub Committee of Semiconductor Devices Reliability determined that the characteristics of the measurement system should be evaluated by comparing the calculated waveform and the actually measured waveform of the oscillation circuit and that these characteristics should be used to correct the measurement results.

As shown in Appendix **Figure 3**, the discharge circuit consists of capacitor C (a ceramic capacitor recommended), mercury relay S (a lead switch is recommended) and wiring (as short as possible) and a power supply that charges capacitor C via a high-impedance resistor. Then mercury relay S is closed and capacitor C is discharged. In order to generate a high-frequency discharge current, the discharge path must be several centimeters long. Equation (3) shows the relation between inductance L, resistance R (mainly the resistance in the relay contacts), frequency f of the discharge current and time t when discharge current i (t) flows through the discharge circuit.

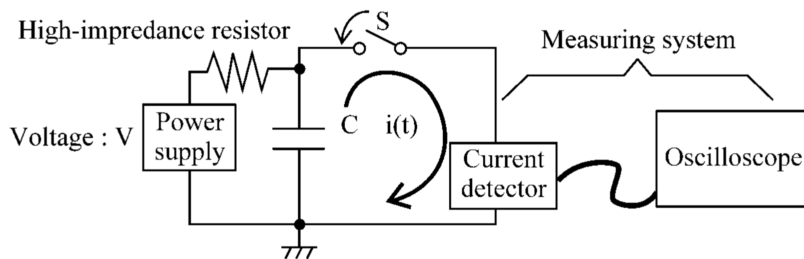
$$i(t) = G\frac{V}{\omega L}e^{-\frac{R}{2L}t}\sin\omega t \qquad \text{....... (3)}$$

$$\text{However, } \omega = 2\pi f = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}, \; G = \text{constant}$$

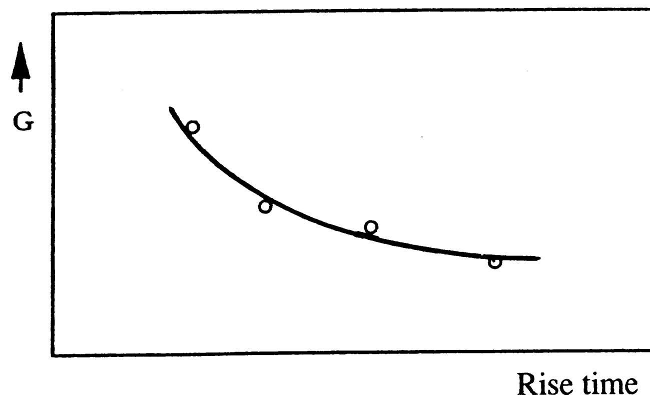
Equation (3) is matched with the waveform measured by the measuring system to derive the unknown quantities L, R and G. Since the measured waveform is slightly distorted, it is difficult to match equation (3) with the entire waveform. Thus the unknown quantities of the maximum peak current value, rise time and the attenuation factor between amplitudes from the second cycle should be derived. Then several values of capacitor C (1 to 10 pF) are used to derive the relation between rise time and G (see **Figure 4**)

When the current is measured in a measuring system using the true value of current amplitude, an amplitude that is seemingly several times G will be derived. For this reason, the measured rise time should be used to derive the G value as shown in Appendix **Figure 4** and this value is subtracted from the measurement result to give the true value of peak current I_{p1}.

Appendix Figure 3 Example of circuit used to evaluate measuring system characteristics



Appendix Figure 4 Rise time dependency characteristics of measuring system



3.9 Role of electrostatic discharge waveform

Relation between the discharge current waveform and the sensitivity of semiconductor device are not yet clear. The following is an outline of this relation.

(1) Rise time t_r

The rise time of discharge current in the charged device model is normally as low as 100 ps. Differences in the response time of the protective element in the semiconductor device with regard to the rise time can affect the test results. And since the transitory phenomena that occur

in the device are related to the rise time, rise time t_r of the testing equipment must be maintained at a value that is close to that of the actual discharge.

(2) Peak current I_{p1}

ESD failure caused by the charged device model method in a semiconductor device is dielectric breakdown of the insulating membranes and other oxide films. This is caused by the transitory voltages generated by discharges having an extremely fast rise time rather than thermal breakdown due to discharge electric energy that is often seen in human models. The type of dielectric breakdown that occurs depend on the type of protective element in the device but it is often an effect of peak current value I_{p1} of the testing equipment. When devices which are prone to dielectric breakdown are tested using test equipment with very high I_{p1} value, the high I_{p1} value even at a low testing voltage will easily cause thermal breakdown and this damage conceals the effect of dielectric breakdown. Thermal breakdown can easily be reproduced using a human model, but when I_{p1} of the testing equipment is raised very high it is difficult to reproduce dielectric breakdown which is a characteristic of the charged device model. Thus the average I_{p1} levels given in **Table 2** which cover most situations that components meet in the field and are values that can safely be used. **Table 2** shows the wide range of I_{p1} values of different test equipment available in Japan, a uniform range will be prescribed when the standard is established.

(3) Pulse width t_d

It is believed that pulse width t_d of the testing equipment affects test result in a thermal breakdown mode.

(4) Undershoot current I_{p2}, Overshoot current I_{p3}

So far it has not been possible to show that I_{p2} and I_{p3} have any effect on test results. The matching of impedance values in the measurement equipment may have an effect on test results.

3.10 Differences between EOS and ESD-DS5.3 test equipment

In 1 988 when the **EIAJ IC-121** standard was revised, the charged device model testing method was subject of deliberations. However, since this method was not in common use at the time, it was added as a testing method proposal to the **IC-121** Standard while standardization was left to a later date. The deliberations this time are based on these earlier deliberations and were started as the method is now commonly used and advances in measuring technology have made it possible to regulate the discharge current. In the progress of the deliberations, data submitted by the members indicated that setting the peak current I_{p1} value for the testing equipment as large as the recommendations made in the EOS/ESD-DS5.3 caused phenomena that differed from the failure mode which are typical of the charged device model (see Section **3.9 (2)**. For this reason, a peak current I_{p1} value that was lower than that in the EOS/ESD-DS5.3 was prescribed in the provisional standard. The non-contact method used in the EOS/ESD-DS5.3 is the same type as that prescribed in the provisional standard. However, since the I_{p1} value is high, the area of the metal discharge bar is very large and it was found out that the electrode at the center of this bar had to be shortened. The result was that the cathode of the large metal discharge bar concealed the specimen and that this made it difficult to bring the electrode close to the terminal to be tested also hampered the visual inspection of the test.

3.11 Testing procedures

The following factors were problems in determining the test procedures.

(1) In this testing procedure a high voltage power supply is brought close to the specimen. Thus in order to ensure stable potential in the specimen, it was determined that one times discharge is to be performed. Several times discharges can be performed when the relevant specification prescribes it.

(2) The discharge energy induced by the charged device model is lower than the human model, so when multiple discharges are to be made the interval between discharges should be 0.1 seconds or longer (1 second in the human model).

3.12 Tests of small capacitance method

The small capacitance method is a testing method that resembles the charged device model method. In the charged device model a device is charged and a metal bar is then brought close to a terminal on the device to cause a discharge. This test makes it possible to faithfully reproduce actual discharge conditions. The small capacitance method uses a capacitance - like the human model where such a capacity is built up in a capacitor - that is as small as that of the device and uses it to cause discharges between the terminals of a device.

The small capacitance method differs from the human body model method in that a capacitance is not used to store the capacitance. Instead, it uses a metal cylinder with a thin metal bar at its center and the capacitance is stored between the cylinder and the bar. The equipment is designed so that the route of the capacitance through the integrated charge switch to the specimen and from there to the thin metal bar on the metal cylinder is as short as possible. This makes it possible to keep impedance at a minimum during the discharge path and produces a discharge current which is as fast as that of the charged device model. The test format of the small capacitance method differs entirely from that of the charged device model. However, the discharge of a capacitance that is equal to that of the device from a metal bar to the device resembles charged device model and the electrical characteristics of both methods are reported to be similar.

It has also been reported that from the results of evaluations of a number of devices the failure mode of the small capacitance method test often matches that produced by the charged device model. The failure caused by tests such as gate oxide film breakdown and other electric field breakdowns seen in MOS semiconductors are reported to be very similar for both methods. Thus the small capacitance method can be used as an alternative to the charged device model test.

However, the small capacitance method differs from the charged device model test in the following respect. The former method forces a discharge between the terminals to be tested on the device and the reference terminal, whereas the latter discharges charges distributed in the device via the terminals to be tested. There are reports that state that the sensitivity and failure modes differ for the two methods.

Since both methods use high-frequency discharge current, it is necessary to correct the peak measurement value during calibration (see Section **3.8**).

For the above reasons, only the minimum of the waveform conditions has been standardized.

4. FUTURE OBJECTIVES

As shown in **Figure 5**, discharge current Ical that flows from the calibration module to the metal discharge bar should be measured, but such a method could not be devised in the deliberations and the provisional method shown in **Figure 7** had to be used. Consequently, this test method is established as a provisional test method which will be revised when the relevant problems have been solved and be included in the formal release of the specification.

TEST METHOD 306
LATCH-UP

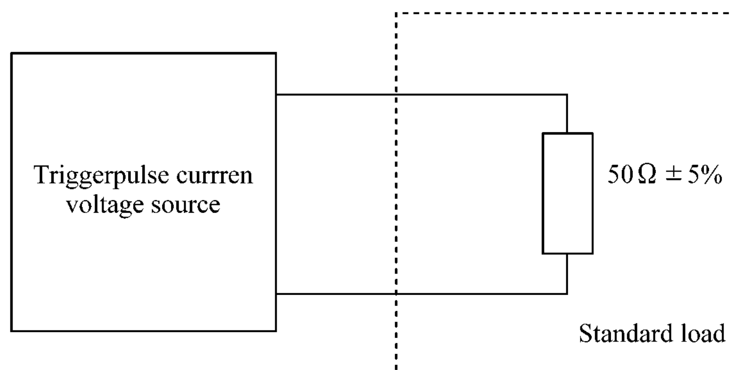
1. SCOPE

This standard defines a method of evaluating the endurance of a semiconductor device (mainly CMOS devices) to "latchup" which is a temporary short-circuiting between the power source and the ground caused by electric noises coming from I/O and power supply pins of a semiconductor device through a parasitic bipolar structure (SCR action) before a power supply is removed.

2. TEST EQUIPMENT

The test apparatus for the latchup test should consist of a power source for generating a current or voltage specified in Section **3.1** or **3.2**, a pulse generator, a current detector, and a change-over switch. The waveform of trigger pulses is measured by a circuit (see **Figure 1**) having a resistor of 50Ω±5% as a standard load. Make sure that the waveform satisfies requirements defined in Subsections **3.1.3** and **3.2.3**.

Figure 1 Trigger Pulse Waveform Measuring Circuit



3. TEST PROCEDURE

There are two testing methods: Test Method I and Test Method II. Selection of a testing method is specified in each standard.

3.1 Test method I (Pulse current injection)

3.1.1 Preprocessing

Specified in each standard if necessary.

3.1.2 Initial measurements

Should be performed according to items and conditions specified in each standard.

3.1.3 Test circuit and electric characteristics

Figure 2 and **Figure 3** shows test circuits for the Test Method I. Their electric characteristics to be satisfied are shown in **Table 1** , **Figure 4**, and **Figure 5**.

Figure 2 Test Circuit for Test Method I (Positive current)

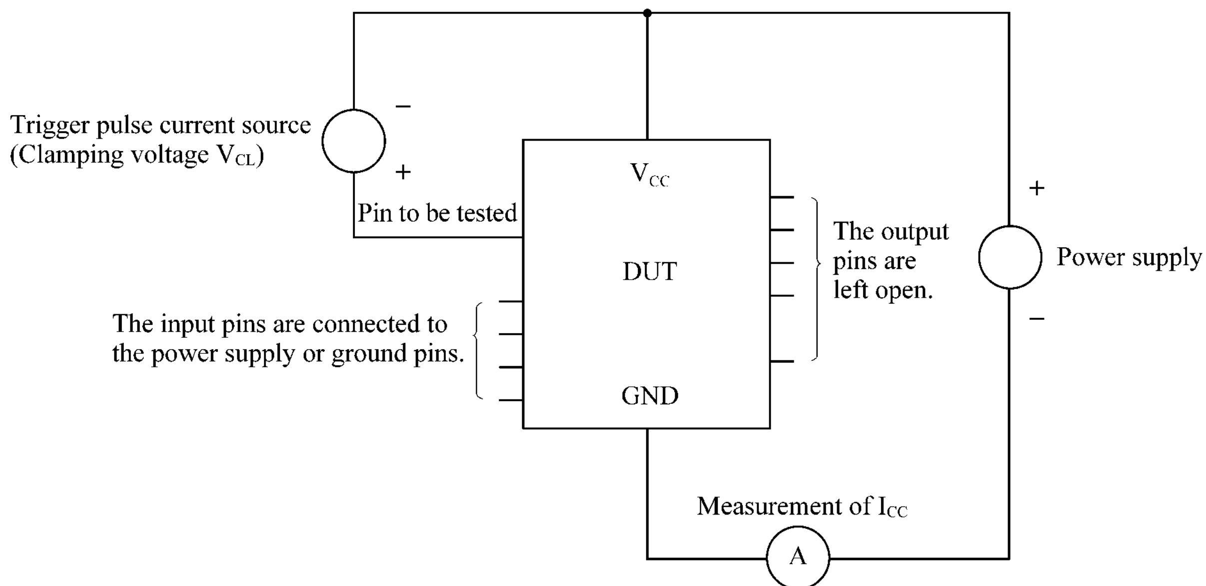


Figure 3 Test Circuit for Test Method I (negative current)

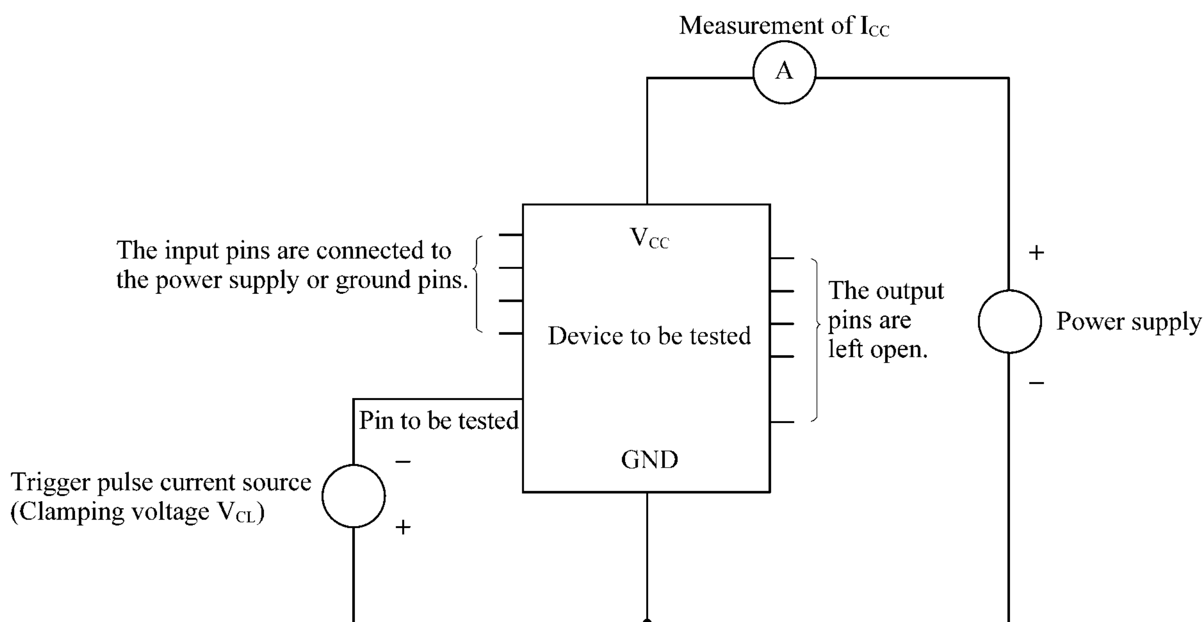


Table 1 Electric Characteristics of Trigger Pulse Current

Item	Symbol	Rated value		Unit	Remarks
		min.	max,		
Pulse width	t_p	$2 \times t_r$	10	ms	
Rise time	t_r	0.005	1	ms	(10% - 90%)
Fall time	t_f	0.005	1	ms	(90% - 10%)
Holding time	t_{OFF}	$50 \times t_p$			When repeated
Position of supply current measuring strobe	t_{STB}	10		ms	
Overshoot	I_{OS}	5% or less of I_{trig}			
Accuracy of trigger pulse current	I_{trig}	±5% or less of the set value			

Figure 4 Waveform of Trigger Pulse Current (Positive Current)

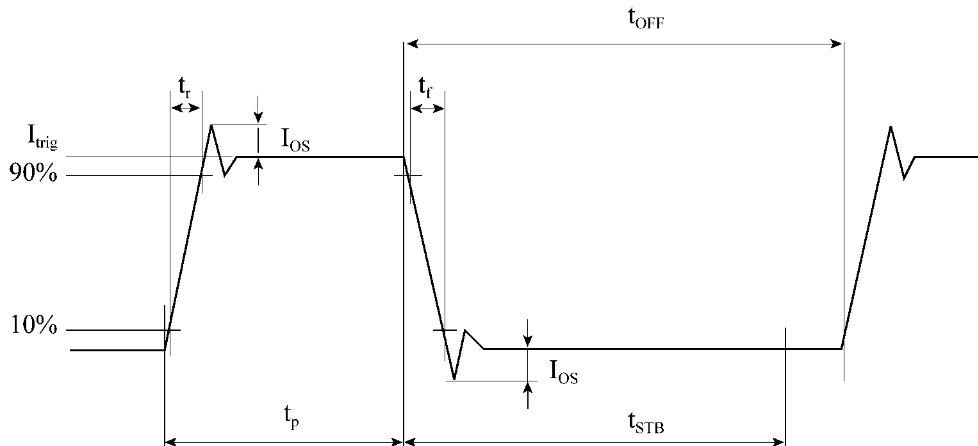
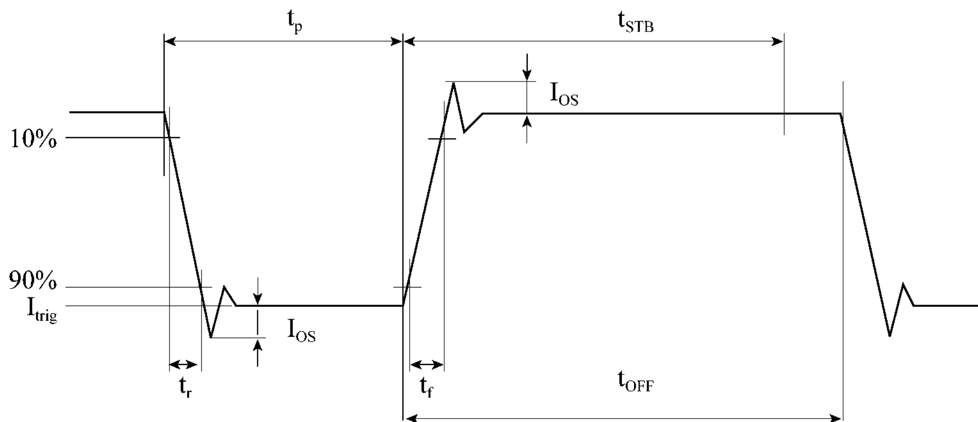


Figure 5 Waveform of Trigger Pulse Current (Negative Current)



3.1.4 Procedures to apply trigger pulses

(1) Apply a supply voltage Vcc to the semiconductor device to be tested. The supply voltage should be the maximum recommended supply voltage according to the specification in the detailed specifications.

The current limit of the power source should be more than a reference current for latchup judgment but less than the device breakdown voltage which appeared on the stress terminal. The ambient temperature during testing should be 25°C±5°C unless otherwise specified.

(2) Set the status of all input and output pins except for the test pin of the semiconductor device according to the specification of the detailed specifications . Connect the input pins to the power source or GND pin and leave the output pins opened unless otherwise specified.

(3) Supply a specified trigger pulse current (Subsection **3.1.3**) to the test pin of the DUT. The test pin can be any pin of the device except for the power supply pin (Vcc) and the reference pin (GND).

Trigger pulses should be applied only once . The polarity and current value of trigger pulses to be applied should be specified in the detailed specifications. The clamping voltage V_{CL} Of the trigger pulse power source should be an absolute value of Vcc

Remarks:

1. The recommended test trigger pulse current should be 50mA.
2. The pulse width of the trigger pulse current should be as little as possible so that the semiconductor device under test (DUT) may not be heated up.
3. When the clamping voltage V_{CL} exceeds the absolute maximum rating of the test pin, the DUT may be damaged or broken down. To prevent this, the clamping voltage V_{CL} must be specified in the detailed specifications.

(4) When the impression of the trigger pulse current ends, measure the supply current I_{cc} Of the DUT at the measuring strobe position t_{STB} of the supply current by measuring the potential difference between two ends of a resistor of 1 ohm or less or an ammeter whose internal resistance is 1 ohm or less. When the supply current I_{cc} greater than the reference current for latchup judgment specified in the detailed specifications flows, it is assumed that a latchup has occurred with the applied trigger pulse current value. However, when the voltage of the trigger pulse current source reaches the compliance voltage V_{CL} while trigger pulses are applied, the testing must be aborted immediately.

(5) When a latchup occurs, immediately turn off the supply voltage, wait until the DUT is cooled fully, then start the next test.

Remarks :

If a pin has a high input impedance and requires a voltage greater than the clamping voltage to inject a predetermined trigger pulse current, a latchup will rarely occur in the normal service status because the trigger pulse current will not be injected into the pin in the normal service status.

3.1.5 Final measurement

Perform the final measurement according to items and conditions specified in the detailed specifications.

Remarks :

Check whether the DUT is defective if necessary.

3.1.6 Items to be specified in the detailed specifications

(1) Testing method [Refer to **3.**]

(2) Preprocessing (if necessary) [Refer to **3.1.1.**]

(3) Items and conditions of initial measurement [Refer to **3.1.2.**]

(4) Supply voltage (when not specified in the standard) [Refer to **3.1.4.**]

(5) Supply current limit value [Refer to **3.1.4.**]

(6) Ambient temperature (when not specified in the standard) [Refer to **3.1.4.**]

(7) Handling of input and output pins except for test pins [Refer to **3.1.4.**]

(8) Pins to be tested (when not specified in the standard) [Refer to **3.1.4.**]

(9) Number of impressions of trigger pulses (when not specified in the standard) [Refer to **3.1.4.**]

(10) Polarities of trigger pulses [Refer to **3.1.4.**]

(11) Trigger pulse current value [Refer to **3.1.4.**]

(12) Clamping voltage (when not specified in the standard) [Refer to **3.1.4.**]

(13) Current detecting resistor (Other than a recommended value) [Refer to **3.1.4.**]

(14) Reference current value for latchup judgment [Refer to **3.1.4.**]

(15) Final measurement (if necessary) [Refer to **3.1.4.**]

3.2 Test method II (Supply overvoltage)

3.2.1 Preprocessing

Specified in each standard if necessary.

3.2.2 Initial measurement

Should be performed according to items and conditions specified in each standard.

3.2.3 Test circuit and electric characteristics

Figure 6 shows a test circuit for the Test Method II. Its electric characteristics to be satisfied are shown in **Table 2** and **Figure 7**.

Figure 6 Test Circuit for Test Method II

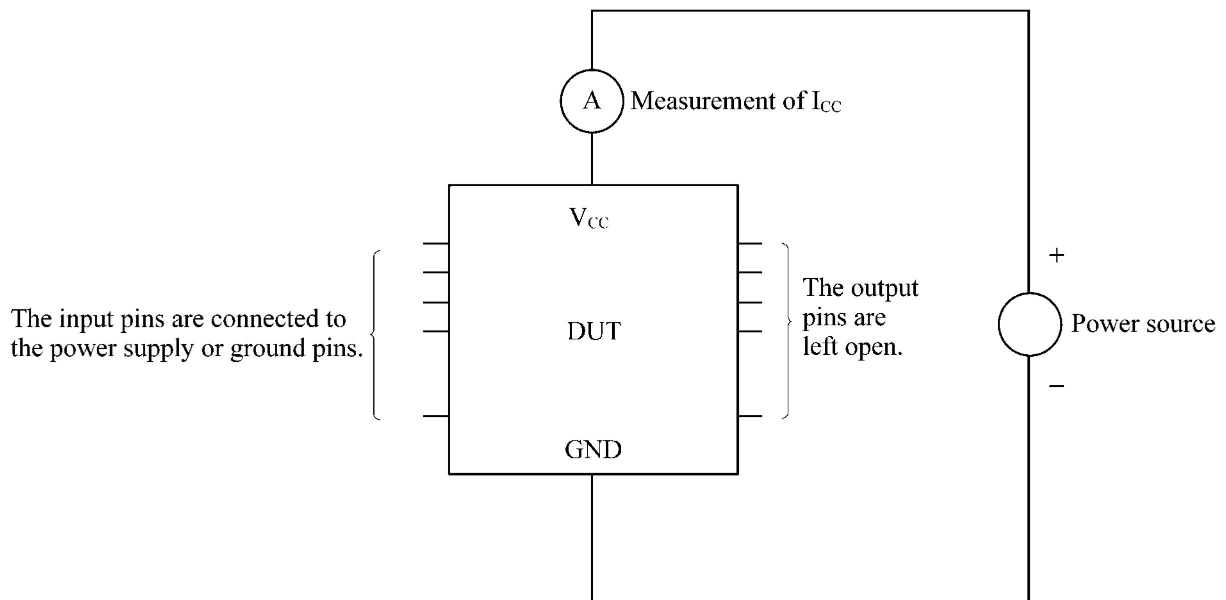
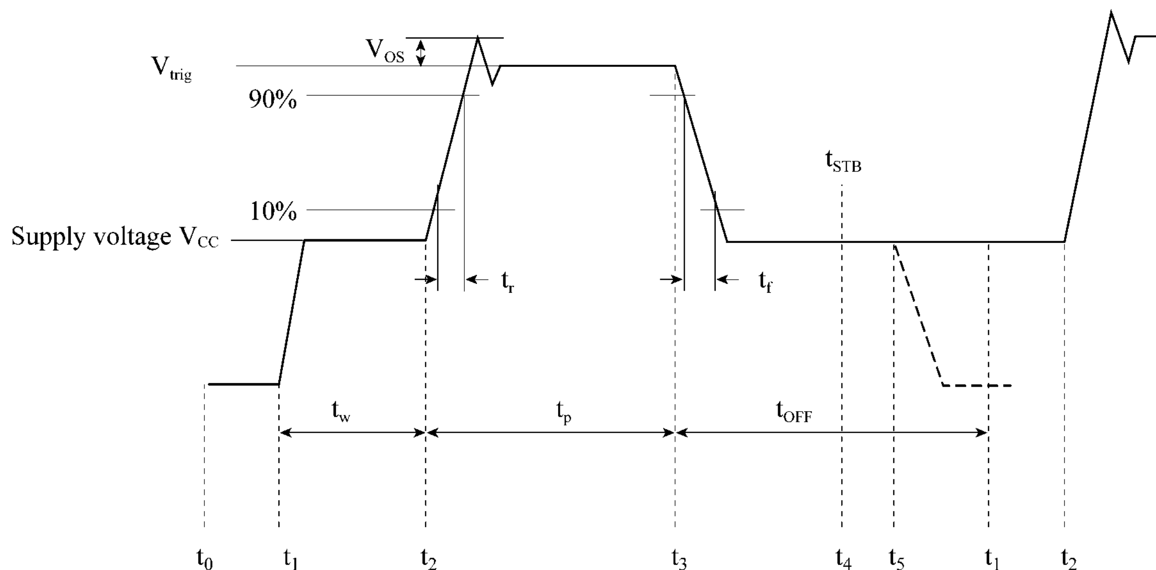


Table 2 Electric Characteristics of Trigger Pulse Current

Item	Symbol	Rated value		Unit	Remarks
		min.	max,		
Pulse width	t_p	$2 \times t_r$	5	s	
Rise time	t_r	0.005	5	ms	(10% - 90%)
Fall time	t_f	0.005	5	ms	(90% - 10%)
Waiting time	t_w	*1			
Holding time	t_{OFF}	t_p		s	
Position of supply current measuring strobe	t_{STB}	0.003	5	s	
Overshoot	V_{OS}	5% or less of V_{trig}			
Accuracy of trigger pulse current	V_{trig}	±5% or less of the set value			

Note *1 : Time waiting for the specified logical status should be specified in the detailed specifications.

Figure 7 Trigger Pulse Voltage Waveform



3.2.4 Procedures to apply trigger pulses

(1) Apply a supply voltage V_{cc} to the semiconductor device to be tested. The supply voltage should be the maximum recommended supply voltage according to the specification in the individual standard. The current limit of the power source should be more than a reference current for latchup judgment but less than the breakdown voltage of the device. (t_1 in **Figure 7**)
The ambient temperature during testing should be 25°C±5°C unless otherwise specified.

(2) Set the status of all input and output pins except for the test pin of the semiconductor device according to the specification of the detailed specifications . Connect the input pins to the power supply or GND pin and leave the output pins opened unless otherwise specified. (Between t_0 and t_2 in **Figure 7**)

(3) Increase the supply voltage up to the trigger pulse voltage Vtreg in relation to the ground (GND). The number of impressions of trigger pulses should be once unless otherwise specified. The supply voltage should not exceed the absolute maximum rating of the DUT. (Between t_2 and t_3 in **Figure 7**)

(4) After applying a specified trigger pulse current (Subsection **3.2.3**) to the test pin of the semiconductor device to be tested, lower the supply voltage down to the maximum recommended voltage, then measure the supply current I_{cc} of the DUT at the measuring strobe position t_{STB} of the supply current by measuring the potential difference between two ends of a resistor of 1Ω or less or an ammeter whose inherent resistance is 1Ωor less. (t_4 in **Figure 7**)

(5) When the supply current I_{cc} greater than the reference current for latchup judgment specified in the detailed specifications flows, it is assumed that a latchup has occurred with the applied trigger pulse current value. The power supply must be stopped immediately. When the supply current I_{cc} is under the reference current for latchup judgment, the next latchup test can be continued. In this GHz, wait until the DUT is fully cooled, then start the latchup test from the test item t_1 (t_5 in **Figure 7**)

Remarks :

In case the DUT has two or more power supply pins, apply the specified voltage to all of the power supply pins, then apply trigger pulses to each power supply pin.

3.2.5 Final measurement

Perform the final measurement according to items and conditions specified in the detailed specifications.

Remarks:

Check whether the DUT is defective if necessary.

3.2.6 Items to be specified in the relevant specifications

(1) Testing method [Refer to **3.**]
(2) Preprocessing (if necessary) [Refer to **3.2.1.**]
(3) Items and conditions of initial measurement [Refer to **3.2.2.**]
(4) Waiting time [Refer to **3.2.3.**]
(5) Supply voltage (when not specified in the standard) [Refer to **3.2.4.**]
(6) Supply current limit value [Refer to **3.2.4.**]
(7) Ambient temperature (when not specified in the standard) [Refer to **3.2.4.**]
(8) Handling of input and output pins [Refer to **3.2.4.**]
(9) Number of impressions of trigger pulses (when not specified in the standard) [Refer to **3.2.4.**]
(10) Absolute maximum ratings [Refer to **3.2.4.**]
(11) Trigger pulse voltage value (when not specified in the standard) [Refer to **3.2.4.**]
(12) Current detecting resistor (Other than a recommended value) [Refer to **3.2.4.**]
(13) Reference current value for latchup judgment [Refer to **3.2.4.**]
(14) Final measurement (if necessary) [Refer to **3.2.5.**]

4. NOTICES

(1) The floating capacitance of wiring between the semi-conductor device under test (DUT) and the test apparatus should be small enough to have no effect on the impressed pulse voltage and the current waveform.

(2) The reference current value for judgment of a latchup of the DUT greatly depends upon the characteristics of the DUT. Accordingly, it should be specified for each DUT type.

(3) The current value which causes a latchup varies according to the temperature of the DUT. Therefore, the temperature of the DUT must be kept as constant as possible. If a latchup occurs in the course of testing, cool down the DUT fully, then restart testing. If the DUT is cooled insufficiently, the latchup endurance of the DUT may be lower than the expected.

(4) As the latchup test forcibly applies an electric stress to the DUT, it sometimes happens that the DUT is damaged by the electric stress (EOS). In this case, it seems that a latchup occurred, but substantially it is due to the destruction of the DUT. Identify the phenomenon carefully.

(5) In some cases, when a latchup occurs, a large current flows between the power supply and the ground (GND), breaks wiring in the DUT, and consequentially open the circuit between the power supply and the ground (GND). In such a case, no more supply current flows and a latchup will never occur in the succeeding test of the DUT.

(6) The supply current limit value should be such that it will not break the DUT when a latchup occurs. If the preset supply current value is equal to or less than the latchup retaining current value, a latchup will never occur even when trigger pulses are applied. Therefore, set the supply current limit value, fully considering the characteristics of the DUT .

(7) In case a DUT may become unstable and oscillate during a latchup test of an input pin of the DUT (as the input pin opens temporarily), the input pin to be tested can be connected to the V_{cc} or GND pin via a resistor. The resistance of the resistor should not have any effect on the trigger pulse current value to be applied.

REFERENCE 1. SUPPLEMENTER MATTERS RELATED TO THE TEST METHODS

1. PURPOSE OF ESTABLISHMENT

Recently, semiconductor devices have been turned into low-power complementary metal oxide semiconductors (CMOS). A "latchup" is a phenomenon specific to a semiconductor device having a parasitic thyristor structure such as a CMOS and its testing method has been expected so much. In countries outside Japan, the testing method has already been defined by the EIA/JEDEC (JEDEC Standard N0.17, August, 1988) and by the IEC (IEC SC47A(CO)266, November, 1991). So, in Japan, the EIAJ has been expected to establish a latchup testing method.

Under the above circumstances, the Special Technical Committee on Semiconductor Devices Quality and Reliability subcommittee adopted and deliberated establishment of this latchup testing method as a main theme in 1992 and 1993 activity years.

2. PROCESS OF DELIBERATION

According to the above view. the establishment of this test method was deliberated by Group A of the Semiconductor Devices Quality and Reliability subcommittee under the Special Technical Committee on Semiconductor Devices Quality and Reliability. The content of deliberations by Group A were occasionally reported to the committee and the subcommittee for approval. Below are listed how deliberations pertaining to the establishment of this testing method has been made.

June, 1992 (Semiconductor Devices Quality and Reliability subcommittee)

The 1992's job themes for Group A were determined. They are the establishment of an electrostatic discharge te sting method and a latch-up testing method. Group members for the them were determined.

September, 1992 (1st Group A deliberation)

(1) Deliberation was made on the organization of Group A.

(2) It was determined to invite three members as special guest members of Group A from Reliability Center for Electronic Components of Japan (RCJ) and to start deliberation from October.

October & November, 1992 (2nd and 3rd Group A deliberations)

After collecting members' opinions on the items proposed in the Semiconductor Devices Quality and Reliability subcommittee, the basic policy of deliberation was determined as shown below .

(1) Pulse Current Injecting Method
- Agreed to establish .... 8 members

(2) Capacitor Voltage Applying Method
- Agreed to establish .... 1 member
- Agreed to abolish .... 4 members
- Agreed to preserve as a reference standard............................... 1 members
- Others .... 2 members

As the result. the subcommittee decided to establish a pulse current injecting method as a standard and not to adopt the capacitor voltage applying method. The above decision was reported to the Semiconductor Devices Quality and Reliability subcommittee and approved there.

January & February, 1993 (4th and 5th Group A deliberations)

Group A compared parameters of the pulse current injecting method by those defined in the EIA/JEDEC and the IEC(CO) documents and discussed problems.

March & April, 1993 (6th and 7th Group A deliberations)

Group A discussed a power testing method upon a request made by a member and decided to adopt a supply overvoltage method defined in the JEDEC standard and to establish it as a standard.

May, June, August September, October, November, and December, 1993 and January, February, March, April and May, 1994 (8th to 19th Group A deliberations)

In these twelve meetings, Group A deliberated a draft of this testing method according to the results of investigations of test apparatus possessed by each member and investigation of documents.

June, 1994 (10th Special Technical Committee on Semiconductor Devices Quality and Reliability)

The final determination of this testing method was reported to the committee and establishment and publication of the testing method were approved there.

3. PROBLEMS DELIBERATED

3.1 Differences from the testing method defined in the JEDEC

Standard and in the IEC(CO) Documents (1) Common items

(1) Common items

Item	**EIAJ ED-4701-1**	**JEDEC Standard No.17**	IEC SC47A (CO) 266
Testing method	(a) Pulse current injecting method (b) supply overvoltage method	(a) Pulse current injecting method (b) supply overvoltage method	(a) Pulse current injecting method (b) supply overvoltage method
Test temperature	25°C±5°C	Less than a current value which destroys the semiconductor device	Not defined ↓
Waveform measuring circuit	50Ω±5%	Not defined	
Latchup judgment standard	Set for each semiconductor device	min. I_{ccmax} + 5mA	
Supply current limit	Less than a current value which destroys the semiconductor device	I_{trig} + 100mA (min.200mA)	Less than a current value which destroys the semiconductor device
Input pins (except a test pin)	V_{cc} or GND	±V_{supply} or Pattern generator	V_{cc} or GND or pattern generator
Output pins (except a test pin)	open	open	Open

(2) Pulse current injecting method

Item	EIAJ ED-4701-1	JEDEC Standard No.17	IEC SC47A (CO) 266
Trigger pulse width	$2 \times t_r$ ~ 10ms	$2 \times t_r$ ~ 5s	Not defined
Rise time	5 µs ~ 1ms	5 µs ~ 5ms	↓
Fall time	5 µs ~ 1ms	5 µs ~ 5ms	↓
Overshoot	5% or less	5% or less	↓
Measuring timing period	10ms or more	5 µs ~ 5ms	↓
Cooling time	$50 \times t_p$ or more	t_w or more	↓
Clamping voltage of trigger pulse current source	$\lvert V_{cc} \rvert$	$\lvert V_{test} \rvert$	↓
Supply voltage at impression of trigger pulse	Maximum recommended supply voltage	Range specified in the specification	↓

(3) Supply overvoltage method

Item	EIAJ ED-4701-1	JEDEC Standard No.17	IEC SC47A (CO) 266
Maximum trigger pulse voltage	Absolute maximum rating	Not defined	Not defined

3.2 Selection of a testing method

Selection of a latchup testing method was deliberated according to the following standards (and drafts):

(1) Latchup testing method

(Draft) (Internal documents of EIAJ Committee STCS-DQR AB-6201)

Pulse current injecting method or Capacitor voltage impressing method

(2) JEDEC Standard N0.17 (August, 1988)

Pulse current injecting method or Supply overvoltage method

(3) IEC SC47A(CO)266 (November, 1991)

Pulse current injecting method or Supply overvoltage method

Among above three testing methods, the pulse current injecting method has been adopted because the contents of the EIAJ testing method (draft) are contained in the JEDEC standard and the IEC(CO) documents (except for part of specified values) and because a latchup which is induced by a current can be regenerated any time by current injection.

Standardization of the capacitor voltage impressing method was cancelled because the basis of 200pF and 0Ω is not clear and because a current is forcibly fed through the DUT at a high voltage (which is abnormal) although some members were in favor of the capacitor voltage impressing method because it had been adopted by some users and manufacturers .

The supply overvoltage method was adopted because it has been standardized by the JEDEC and further it is now deliberated by the IEC and because a method for testing supply pins of semiconductor devices is need although very few test data and references of this testing method are available in Japan.

3.3 Test temperature

It is known that the latehup strength of a semiconductor device decreases as the temperature increases. To facilitate comparison and relative evaluation of latchup strengths of semiconductor devices at

room temperatures, the ambient temperature during testing is made 25°C±5°C. If the test temperature is particularly required (according to the operating environments of semiconductor devices), it should be specified in the detailed specifications.

3.4 Standard load for waveform measurement

The relationship between waveforms to be monitored under the standard load condition and waveforms of trigger pulses to be applied to a DUT (semiconductor device under test) is not clear and must be deliberated in the future.

3.5 Latchup judgment standard

A method of using a preset supply current value as a latchup judgment standard was offered. However, the preset supply current value varies widely (e.g. from 1μA to 100 mA) according to the type of semiconductor devices. Accordingly it is meaningless to use a single fixed supply current value. Therefore, it is determined to specify an adequate supply current value to each semiconductor device type.

3.6 Supply current limit value

This should be specified to protect a semiconductor device under test (DUT) against damages by a latchup. Similarly to the latchup judgment standard. an adequate supply current limit must be set for each semiconductor device type. It should be as high as possible. considering the latchup retaining current characteristics.

3.7 Logical setting of non-test pins

It is very time-and labor-consuming to test a semiconductor device in all logical states. Accordingly, in the latchup test, the input and output pins are connected to the V_{cc} or GND pins to assure stability of testing and reproducibility of test results. Therefore, pin conditions must be added to the test results.

3.8 Pulse width of trigger pulse current

As the result of investigating a tendency that the latchup strength decreases as the heat generation by a trigger pulse current increases, it is found that the test result will be affected by the heat generation when the pulse width exceeds 10ms. As for some kinds of semiconductor devices, their latchup strengths (endurances) are a little affected when the upper pulse width limit is 10ms.

Some members said that pulse widths should be specified strictly. However, considering the functional restrictions of testing apparatuses, an attainable pulse width range $2 \times t_r$ to 10ms is adopted.

The pulse width for the testing should be as short as possible considering the turn-on/off time of the parasitic thyristor when a latchup generates.

3.9 Trigger pulse rise and fall

Times and Measuring Timing Period These time values are set so that the latchup test can be carried out steadily with less noises.

3.10 Cooling time

A cooling time should be set adequately to fully cool a hot semiconductor device under test (DUT) to make the characteristics of the DUT stable.

3.11 Clamping voltage of pulse current injecting method

The pulse current injecting method has a possibility to damage the DUT by an overvoltage stress (EOS) caused by trigger pulses. To prevent such a trouble, the upper limit of the trigger pulse

voltage must be determined. There were many arguments on its value. In some cases (e.g. a surge test of an electronic apparatus), a voltage exceeding some ten volts is applied to a semiconductor device. In such a case, the electronic apparatus must take a measure to reduce the voltage below the specified value of the semiconductor device. This testing method has adopted the maximum recommended supply voltage $| V_{cc} |$ as a clamping voltage, considering a potential difference which may possibly generate in the normal operating status of the semiconductor device.

For this reason, the following two cases can be assumed in which potentials of pins except for power supply pins become higher than the supply voltage in the normal operating status of a general semiconductor device :

(a) In case a voltage is supplied to a specific input pin prior to any of power supply pins on a circuit board which uses two or more power supplies due to asynchronism of rise timings of power supplies.

(b) In case a semiconductor device in an apparatus or a printed circuit board whose power must be started up is connected to an active apparatus and a voltage is supplied to I/O pins prior to power supplies.

In the above cases, a potential difference between the I/O pin and a power supply pin is equal to the maximum supply voltage (which was said by some members). The maximum pulse voltage value specified in the pulse current injecting method of the JEDEC is up to the supply voltage $| V_{test} |$ (at the impression of trigger pulses). This value is also used as a reference.

3.12 Supply voltage

Assuming the worst case in the operating voltage range, a maximum recommended supply voltage is used in the latchup test. Although the supply voltage V_{test} at impression of trigger pulses and the supply voltage V_{cc} during measurement of I_{cc} are defined separately in the JEDEC standard, the current standard treats them as an identical supply voltage for convenience.

3.13 Test voltage in the supply overvoltage method

As the performance of a semiconductor device is not assured for a voltage exceeding the absolute maximum rating, it is determined that the upper limit of the test voltage is the absolute maximum rating or less.

3.14 Trigger pulse waveform in the supply overvoltage method

The maximum trigger pulse width (up to 5ms). specified in the JEDEC standard is directly used in the current standard assuming that this trigger pulse injecting method generates less heat than the pulse current injecting method.

4. PROBLEMS TO BE SOLVED

(1) As to international standards, JEDEC Standard No.17 was revised to JEDEC Standard No.78 (March, 1997) and IEC is studying the standardization based on IEC/PAS 62181 (July, 2000). In JEITA, however, no discussion has been made since June, 1994, and therefore, the testing method needs to be reviewed shortly, and revised if necessary, considering the compatibility with the international standards.

(2) This latchup test simulates part of latchup phenomena of semiconductor devices and the phenomenon does not always match with actual phenomenon. More scientific study and research are required for improvement of the testing method (including the establishment of a new testing method).

TEST METHOD 307
THERMAL SHOCK [1]

1. SCOPE

This standard provides for the method to evaluate the endurance of the semiconductor devices when they are submitted to rapid changes in the temperature.

Remarks;

1. Initially, this test was designed by assuming the cleaning of semiconductor devices by means of heated solvents. Recently, however, the thermal shock test is being used in some cases as an alternative test substituting the temperature cycle test, but care must be taken when applying it because it may bring about failure modes that are impossible in the field. (Refer to **REFERENCES**).
2. The glass transition temperature point of resin has gradually become lower as packages become thinner and more compact, and a failure modes that dose not occur in the field may occur due to overshooting the glass transition temperature under a high-temperature test condition, in particular.
   It is, therefore, necessary to take such a failure into due consideration in case of the application.

2. TEST EQUIPMENT

Two chambers, capable to keep the fluid at the high temperature and low temperature conditions of Table 1, should be used. These two chambers must be installed adjacent to each other, so as to allow the transfer of the specimen within the transfer time specified in section **3.2.2** Liquid to be used in this test should be in conformity with the stipulations shown in Table 1.

3. PROCEDURE

When the specimen is plastic-moulded SMD, carry out the moisture soaking and soldering heat stress treatment specified in the TEST METHOD **104** (Moisture soaking and soldering heat stress test series) prior to this test.

3.1 Initial measurement

Carry out the initial measurements in conformity with the items and conditions specified in the relevant specifications.

3.2 Tests

3.2.1 Test Conditions

The temperatures in the two chambers and the fluids to be used therein should be selected out the conditions A, B, C, D and E of **Table 1**, or from within the range of the storage conditions (T_{stgmin} to T_{stgmax}) specified in the relevant specifications. The Conditions A should be applied unless otherwise specified.

Table 1 THERMAL SHOCK TEST CONDITIONS

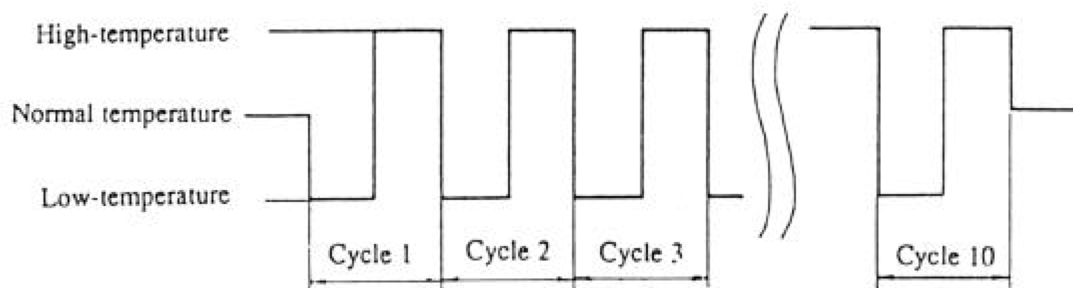
Code of the test conditions		A	B	C	D	E
High temperature side		100°C $^{+0}_{-5}$ °C	125°C±5°C	150°C±5°C	200°C±5°C	T_{stgmax}±5°C
Low temperature side		0°C $^{+5}_{-0}$ °C	-55°C±5°C	-65°C±5°C	-65°C±5°C	T_{stgmin}±5°C
Fluid used	High temperature side	Pure water (running water)	Appropriate medium	Appropriate medium	Appropriate medium	Appropriate medium
	Low temperature side	Pure water (running water)	Appropriate medium	Appropriate medium	Appropriate medium	Appropriate medium

3.2.2 Test methods

(1) Method I

The specimen should be dipped in the specified fluid of the low-temperature side for 5 or more minutes. After that, it should be dipped in the high-temperature side fluid for 5 or more minutes. The specimen should be transfer from the low-temperature side to the high-temperature side, or vice versa, within 10 seconds. Ten cycles should be repeated as shown in **Figure 1**, unless otherwise specified.

Figure 1 THERMAL SHOCK TEST PATTERN



(2) Method II

The dwell time which the specimen is to be dipped in the specified fluid of the low-temperature side and high-temperature side should be from 15 seconds to 5 minutes, and the transfer between them should be done within 3 seconds. All other relevants are the same as those of Method I.

Remarks:

Selection of the test method: The standard test methods shown in the following are recommended for each applicable case.

(1) When the mass of the specimen exceeds 1.5g or more: Test Method I

(2) When the mass of the specimen is less than 1.5g: Test Method II

Note ([1])
This test corresponds to RAPID CHANGE OF TEMPERATURE: TWO-FLUID-BATH METHOD of the IEC standards.

3.3 Post treatment

Whenever required, wash the specimen with pure water (running water) or another appropriate fluid after finishing the last cycle, and then leave it standing under normal conditions from 2 hours to 24 hours.

3.4 End-point measurement

Carry out the end-point measurements in conformity with the items and conditions specified in the relevant specifications.

4. INFORMATION TO BE GIVEN IN THE RELEVANT SPECIFICATIONS

(1) Items and conditions of the initial measurements [Refer to **3.1**]

(2) Code of the test conditions (When using test conditions other than those ones of Conditions A of **Table 1**) or the test temperatures (When using temperatures other than those ones of **Table 1**) [Refer to **3.2.1**]

(3) Fluid to be used (When using fluids other than those of Conditions A of **Table 1**) [Refer to **3.2.1**]

(4) Test method [Refer to **3.2.2**]

(5) Number of repetition cycles (When executing the test with number of cycles other than 10) [Refer to **3.2.2(1)**]

(6) Post treatment (When executing the tests with post treatment conditions other than the specified ones) [Refer to **3.3**]

(7) Items and conditions of the end-point measurements [Refer to **3.4**]

REFERENCE 1
SUPPLEMENTARY INFORMATION ON THE TEST METHOD

1. TECHNICAL BACKGROUND

The thermal shock test is characterized by an extremely rapid shift from low/high temperature conditions to high/low temperature conditions, compared with the slow transition of the temperature cycle. The name "THERMAL SHOCK" of this test has been adopted in view of the extremely rapid temperature change. In general, the specimen is made of various materials with different thermal expansion coefficients, and stress occurs during the thermal cycle test due to the differential expansion and contraction extents of the various materials at the high and low temperatures, and failures related to deformation and rupture occur when the number of cycles is increased. On the other hand, peculiar failures induced by rapid temperature changes occur in the thermal shock test, in addition to failures similar to those ones of the temperature cycle test.

These peculiar failures consist of deformations and ruptures in the specimen resulting from stresses due to differential expansion and contraction extents at the inner and outer sides, caused by large instantaneous differential temperatures between the outer side of the specimen (directly in contact with the heat medium) and the inner side (not in contact with the heat medium). Since these failures may occur even when the specimen is made of a single material (same as a crack that occurs in a frozen glass cup when it is placed in hot water), they are distinguished from failures caused by thermal cycle.

As mentioned above, it may safely be said that the thermal shock test is a method consisting of composite conditions, in which there is repetition of transient states accompanying rapid temperature changes, in addition to the cycle repetition of high-temperature and low-temperature conditions.

2. ON THE SCOPE OF APPLICATION

The following cases related to actual conditions of practical use of semiconductor devices are presumed to be examples of environmental conditions corresponding to those ones of the thermal shock test, in which the semiconductor device is exposed to rapid temperature changes of the order of scores of degrees centigrade.

- Cleaning of the semiconductor device and printed circuit board using hot solvent
- Current applying test in hot inert fluid
- Thermal stress during solder mounting (The SOLDERING HEAT ENDURANCE TEST is specified for this stress), etc.

Since these cleaning and current applying tests may be carried out several times, the conditions of this thermal shock test are specified within a sufficient margin of safety related to temperature and number of times of repetition.

3. ON THE CORRELATION WITH THE THERMAL CYCLE TEST

(1) Precautions related to the application

Temperature changes due to changes in the meteorological conditions and ON/OFF of the power are slow. The temperature cycle test is recommendable to apply with these temperature changes.

Recently, the thermal shock test is being executed in some cases as an alternative test method of

the thermal cycle test with the object of shortening the test time. When the thermal shock test is executed, there is risk of inducing failures that are impossible in the actual environment, concurrently with rapid temperature changes.

When executing the thermal shock test as an alternative test method, it must be borne in mind that there is risk of occurrence of failures that are impossible in the field, and that the thermal cycle test is the is the basic alternative.

(2) On the accelerabillity

During the discussion of this test method, some members of the committee mentioned that the temperature shock test has accelerabillity several times larger compared with the temperature cycle test. The difference is presumably attributable to the following fact. In the temperature cycle test using the hot gaseous medium, the temperature in the test chamber is unstable, and furthermore the specimen can not reach the specified high temperature and low temperature conditions because of its large heat capacity, and as a result the test in gaseous medium becomes more gentle compared with the thermal shock test in liquid medium. Other committee members mentioned that the same results as the thermal shock test could be obtained when the test conditions are preset by the temperature measured of the specimen itself.

4. DISCUSSION CONTENTS ABOUT THE REVISION AND CARRIED OVER PROBLEMS.

In discussing the revision based on the compatibility with IEC, questionnaires were sent to the committee of each company for the review about the necessity of the revision of thermal shock test and test conditions, and the following results were obtained.

(1) Necessity of the revision of thermal shock test.

More than 75% of the committee (13 out of 17 companies) were of the opinion that the revision is not necessary in particular.

(2) Test condition.

(a) The test temperature conditions were divided roughly in to the six conditions shown below.

-65°C ←→ +150°C, -55°C ←→ +150°C, -55°C ←→ +125°C, 0°C ←→ 100°C,
Tstg.min ←→ Tstg.max, Conformance to MIL standards.

(b) No.of actual test cycles was dispersed over a range of 10 ~ 1000 cycles among the committee of these companies.

Since the execution purposes of this test were not defined yet, the number of test cycles was noticeably dispersed among these companies as a result, because of the mixture of the number of test cycles for the product development processes, customers' demands, and other factors.

(3) There was a following opinions from member of the committee.

(a) Since the work for transferring semiconductor devices from a liquid bath to a liquid bath under the actual working environments requires only washing in the course of assembly, several test cycles(about 5 cycles) may be enough.

No test may be required for resin molded devices.

(Necessity of its discontinuance was reviewed.)

(b) Definition of the basis of the holding time specified by the unitary mass of samples.

(c) The glass transition temperature of package resin is referred to as the remarks in the scope. The glass transition temperature of thin packages, etc. becomes low recently, and its representation should be rechecked.

5. CONCLUSION

According to the results in paragraph 1, almost all members of the committee were of the opinion that the revision is not necessary, in particular, about the thermal shock testing methods.
Since data and materials were insufficient for discussing and reviewing the revision due to the noticeable dispersion about the number of test cycles, indefinite basis of the number of cycles, etc., the substantial revision of thermal shock test was difficult, and the revision was limited to the expression of the glass transition temperature of package resin only at this time.
The required number of test cycles etc. were carried over as the problems to be reviewed in the future.