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Standard of Japan Electronics and Information Technology Industries Association

EIAJ ED - 4702A

Mechanical stress test methods for semiconductor surface mounting devices

Established in October, 1992
Revised in December, 2003

Prepared by
Technical Standardization Committee on Semiconductor Devices

Published by
Japan Electronics and Information Technology Industries Association

11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan
Printed in Japan

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EIAJ ED-4702A

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Mechanical stress test methods for semiconductor surface mounting devices

1. Scope

This standard specifies the evaluation method of the mount board of CSP/BGA packages, regarding the mechanical stresses received, and also regarding the durability to thermal stress, during or after the mount process of discrete semiconductor devices and of integrated circuits (the both devices/circuits are referred to semiconductor devices in this standard) used mainly for industrial and consumer use equipment.

Note 1. The test method specified in this standard is an integrated one by including mounting methods, mounting conditions, printed circuit boards, soldering materials, and so on in the scope of the test. It dose not specify the evaluation method of an individual semiconductor device.

2. Mounting conditions, printed wiring boards, soldering materials, and so on affect significantly the result of the test specified in this standard. Therefore, the test specified in this standard shall not be regarded as the one to be used to guarantee the mounting reliability of semiconductor devices.

3. The test method is not applicable nor necessary if there are no stresses (mechanical and other stress) receiving, which are subject in each test in this standard.

2. Definition of Terms

The terms and difinition below, as well as those described in **EIAJ ED-4701**, are applicable to the standard, and also in the individual standards to be developed as required.

(1) Specimen

The mounted SMD's provided for the tests.

The SMD's provided for the tests.

(2) SMD

Surface Mounting Device which is a semiconductor device designed to be mounted on the surface of a printed circuit board.

(3) Surface Mounting

Mounting or jointing device on the surfaces of printed circuit boards.

(4) The package defined in this standard

The way to load and join parts only on to a printed circuit board.

The word "Chip Scale Package" (CSP) means the package itself whose size is equivalent to or a little bit larger than that of the chip. It dose not mean the outline of the package. However, it is used in the standard to simply and clearly describe the type of the package outline subject to the standard. The word "CSP/BGA packages" in the standard means the packages listed below.

(a) The packages called ball grid arrays (BGA) of ball pin type and also those called land grid arrays (LGA) of N-lead type, classified in Form D in **EIAJ ED-7300** "Basic items for specifications of outline of semiconductor packages".

(b) The packages called quad flat non-leaded packages (QFN) of N-lead type, classified in Form A in **EIAJ EIAJ ED-7300** "Basic items for specifications of outline of semiconductor packages"

(c) The Packages called small outline non-leaded packages (SON) of N-lead type, classified in Form B in **EIAJ ED-7300** "Basic items for specifications of outline of semiconductor packages"

(5) The other terms are based on **EIAJ ED-4701** "Environmental and endurance test methods for semiconductor devices".

3. Normative References

EIAJ ED-4701	"Environmental and endurance test methods for semiconductor devices"
EIAJ ED-7407	"Environmental and endurance test methods for CSP, BGA package on mounting condition"
JPCA-BU01	"Build-up wiring board"
JIS Z 3282	"Solder"
JIS Z 3284	"Solder paste"
JIS Z 5012	"Test method for printed wiring board"
JIS Z 5016	"Test method for flexible printed wiring board"
EIAJ ED-7300	"Basic items for specifications of outline of semiconductor packages"
EIAJ EDR-7315	"Design guideline of integrated circuit for Ball Grid Array (BGA)
EIAJ EDR-7316	"Design guideline of integrated circuit for Fine-Pitch Ball Grid Array and Fine-Pitch Land Grid Array (FBGA/FLGA)
EIAJ ED-7311-5	"Standard of integrated circuits package (SRAM/Flash FBGA)"

The test methods applicable to an individual semiconductor device are specified in **EIAJ ED-4701** "Environmental and endurance test methods for semiconductor devices". The standard set this time is to be used for evaluation of the items of assumed faults, which can exist only with the components being mounted on the board.

4. Classification

(1) Test preparation

Appendix 1: Test Board Design Guideline

Appendix 2: Standard Mounting Process for SMD

This standard specified the mount boards, the mount materials, and the mount methods to be used to evaluate the mount reliability.(This test method is neither applicable nor necessary if there is no doubt of the result of the test for mount reliability evaluation.)

(2) Mechanical environmental tests

Test Method 001: Temperature cycle after mounting

Test Method 002: Strength tests for soldering joint

Method 1: Peel strength test for soldering joint

Method 2: Pull strength test for soldering joint

Method 3: Push strength test for soldering joint

Test Method 003: Bending test for surface mount devices on the board

Test Method 004: Reiterative bending test for surface mount Device

Test Method 005: Drop test after mounting

These tests specify the test methods for durability against the stresses that CSP/BGA mount boards received during or after the mount process.

5. General Consideration

(1) The test method specified in this standard is mainly applicable to the test of the soldered part of CSP/BGA packages being mounted on the board. The soldering strength in this case depends very much on the mount methods, the mount conditions, the used materials, the printed wiring boards, and so on. Therefore, if the desired soldering strength has not been achieved, check and analyze the possible causes to find out whether CSP/BGA package has problems or not. If there is no problem with the CSP/BGA package, it is necessary to carry out again the test after checking the mount methods, the mount conditions, the used materials, the printed wiring boards, and so on.

(2) The test result using this standard is the way of endurance test for mechanical and thermal stress under mounted condition. Therefore, correlation with the conditions in the actual usage of the package shall be fully taken into consideration.

Appendix 1 Test board design guideline

Annex 1 (Reference) describes a supplemental explanation to the test boards design guideline, but it shall not be considered as part of the specification in the standard. It describes the design of the printed circuit board to be used to evaluate the mount conditions of CSP/BGA packages.

1. DESIGN STANDARD

The items listed below are subject to consideration for the design standard of the mount reliability test board.

(1) Classification of board specification

Board thickness, the number of layers, and copper foil thickness

(2) Material of the board

(3) Land shape and land size

1.1 Classification of Board Specification

Both the board thickness and the number of layers of the mount reliability test board that is applicable to CSP/BGA packages are to be determined by selecting the appropriate type in **Table 1**, according to the usage of the semiconductor device subject to the test.

Table 1 Types of mount reliability test board

Type		Type A	Type B	Type C	Type D
Example of application		Cellular phones, Video Camera recorders, etc.	Notebook type PCs	Floor/rack type equipment	Workstations, etc.
Board thickness		0.6-0.8 mmt	1.0-1.2 mmt	1.6 mmt	2.4 mmt
Number of layers		4 layers or more	4 layers or more	4 layers or more	6 layers or more
Terminal pitch (unit:mm)	1.27		◎	◎	◎
	1.00		◎	◎	◎
	0.80	◎	◎		
	0.75	◎	◎		
	0.65	◎	○		
	0.50	◎	○		
	0.40 or less	○			
Standard copper wiring thickness (outer layer/inner layer)(1)	18 μm/12 μm	◎	○		
	35 μm/18 μm		◎	◎	◎

Note(1) nominal dimensions

Note 1. The board design largely depends on the terminal pitch of the mounted component.

Therefore, the table shows the example of applications, and the terminal pitch, which corresponds to the application. The double circles indicate the major present applications while the single circles indicate the assumed future applications.

The copper wiring thickness, also largely depends on the terminal pitch of the mounted component.

It also largely depends on the method of board process. Therefore, there are two kinds of the copper wiring thickness of type B in the table.

2. In general, thicker the board is, shorter the life of the soldering joint in the temperature cycling test becomes. In view of mechanical strength, the stress of the soldering joint tends to be decreased with the board thickness increased. Therefore, it is recommended to select the appropriate board type per application, considering the requirements for test quality.

1.2 Material of the Board

The standard material is FR-4 (NEMA Standard NO.LI 1-1998).

1.3 Board Layer Configuration

Table 2 shows the standard board layer configuration.

Table 2 Standard mount reliability test board layer configuration

Types A, B, and C		Type D	
1st layer	Signal path layer	1st layer	Signal path layer
2nd layer	Plane layer or mesh layer	2nd layer	Plane layer or mesh layer
		3rd layer	Plane layer or mesh layer
3rd layer	Plane layer or mesh layer	4th layer	Plane layer or mesh layer
		5th layer	Plane layer or mesh layer
4th layer	Signal path layer	6th layer	Signal path layer

Note: If a signal path cannot be made in the 1st, 4th and/or 6th layers use the internal plane layer or increase the number of layers.

1.4 Land Shape

Figure 1 shows the standard land shape.

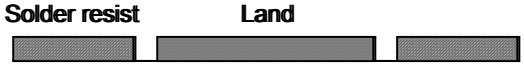


Figure 1 Standard land shape of the mount reliability test board

The standard surface treatment of the land shall be copper plating covered with heat-resistance preflux.

1.5 Land Size

Being applicable to **EIAJ EDR-7315** and **EIAJ EDR-7316** "Design guideline for semiconductor packages", the table below shows the design guideline for the land size of the packages of area array type (BGA, FBGA, LGA, and FLGA).

Table 3 Design guideline for the land size of the packages of area array pin type (BGA, FBGA, LGA, and FLGA)

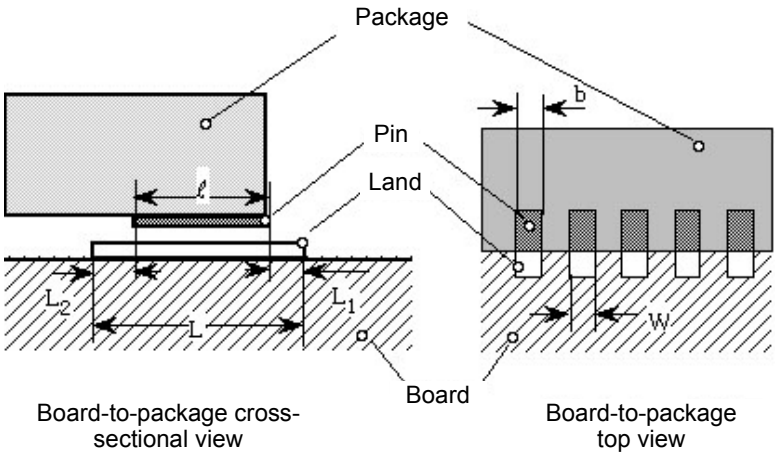
Unit: mm

Terminal pitch	Land size(1)			Notes
	Min.	Nom.	Max.	
1.5	0.60	0.75	0.90	50% of straight line terminal pitch specified in **EIAJ EDR-7315**
1.27	0.60	0.75	0.90	
1.0	0.50	0.60	0.70	
0.8	0.45	0.50	0.55	Applicable to terminal diameter b (c) P-FLGA specified in **EIAJ EDR-7316**
0.75(2)	0.40	0.45	0.50	
0.65	0.35	0.40	0.45	
0.5	0.25	0.30	0.35	
0.4	0.20	0.25	0.30	

Note 1. Land sizes define top diameter.

2. 50 % of straight line terminal pitch specified in **ED-7311-5** applies to 0.75 mm of terminal pitch.

The design standard specifies the land shape of the packages of peripheral pin type (SON and QFN), as shown in **Figure 2.**



Unit: mm

		SON	QFN
l	Lead length of package	Refer to the design standard.	Refer to the design standard.
b	Lead width of package		
L	Land length	· · + L_1 + L_2	
L_1		0.25 ± 0.05	0.30 ± 0.05
L_2		0.00	0.20 ± 0.05
W	Land width	b ± 0.05	b ± 0.05

Figure 2 Design standard for the land shape of the packages of peripheral pin type (SON and QFN)

2. INFORMATION TO BE GIVEN IN THE DETAIL SPECIFICATION

(1) Board type [Refer to **1.1**]

(2) Board size

(3) Board thickness (when not specified) [Refer to **1.1**]

(4) Number of board layers (when not specified) [Refer to **1.1**]

(5) Board layer configuration (when not specified) [Refer to **1.3**]

(6) Copper wiring thickness (when not specified) [Refer to **1.1**]

(7) Board material (when not specified) [Refer to **1.2**]

(8) Land shape (when not specified) [Refer to **1.4**]

(9) Surface treatment of land (when not specified) [Refer to **1.4**]

(10) Land size (when not specified) [Refer to **1.5**]

REFERENCE. SUPPLEMENTARY INFORMATION ON THE TEST METHOD

1. PURPOSE OF ESTABLISHMENT

In discussing this matter, questionnaires were sent to the committee of each company for the test board design. As a result, since being conformable to **EIAJ ET-7407** from these results of the investigation was checked, the Test Board Design Guide was established based on **EIAJ ET-7407.**

Examples of test board design items

<table>
<tr><td rowspan="2">Item</td><td colspan="4" rowspan="2">EIAJ ET-7407</td><td colspan="2">Deliberation contents(1)</td></tr>
<tr><td>questionnaire survey</td><td>resolution</td></tr>
<tr><td>Board type</td><td>Type A</td><td>Type B</td><td>Type C</td><td>Type D</td><td rowspan="2">-</td><td rowspan="2">Conformance to EIAJ ET-7407</td></tr>
<tr><td>Example of application</td><td>Cellular phones,etc</td><td>Notebook type PCs</td><td>Floor/rack type equipment</td><td>Workstations ,etc</td></tr>
<tr><td>Board material</td><td colspan="4" rowspan="2">FR-4</td><td>FR-4(typeA-D：8 companies）</td><td rowspan="6">Conformance to EIAJ ET-7407</td></tr>
<tr><td rowspan="5">Board thickness</td><td rowspan="5">0.6-0.8mm</td><td rowspan="5">1.0-1.2mm</td><td rowspan="5">1.6mm</td><td rowspan="5">2.4mm</td><td>ALIVH(typeA：2 companies）</td></tr>
<tr><td>0.8mm(typeA：4 companies)</td></tr>
<tr><td>1.0mm(typeB：1 company)</td></tr>
<tr><td>1.27mm(type？：1 company)</td></tr>
<tr><td>1.6mm(typeC：1 company)</td></tr>
<tr><td>2.5mm(typeD：1 company)</td></tr>
<tr><td rowspan="4">Number of board layers</td><td colspan="3" rowspan="4">4 layers or more</td><td rowspan="4">6 layers or more</td><td>2 layers：4 companies</td><td rowspan="6">Conformance to EIAJ ET-7407</td></tr>
<tr><td>4 layers：7 companies</td></tr>
<tr><td>6 layers：2 companies</td></tr>
<tr><td>8 layers：1 company</td></tr>
<tr><td>Board layer configuration (outer layer)</td><td colspan="4">Signal path layer</td><td>Signal path layer：7 companies</td></tr>
<tr><td>Board layer configuration (inner layer)</td><td colspan="4">Plane layer or mesh layer</td><td>Plane layer：5 companies
mesh layer：2 companies</td></tr>
<tr><td>Copper wiring thickness (outer layer/inner layer)</td><td colspan="2">18μm/12μm</td><td colspan="2" rowspan="2">35μm/18μm</td><td>35μm/18μm：3 companies
35μm/35μm：1 company</td></tr>
<tr><td>Land shape</td><td colspan="4">Solder resist Land Solder resist</td><td>6 companies
2 companies</td><td>Conformance to EIAJ ET-7407</td></tr>
<tr><td>Surface treatment of land</td><td colspan="4">Copper plating covered with heat-resistance preflux</td><td>heat-resistance preflux ：2 companies
Au plating：1 company</td><td>Conformance to EIAJ ET-7407</td></tr>
<tr><td>Land size</td><td colspan="4">Conformance to EIAJ EDR-7315 or EIAJ EDR-7316</td><td>-</td><td>Conformance to EIAJ ET-7407</td></tr>
</table>

Note([1]) The committee considered the opinion survey results of each company on **EIAJ ET-7407**.

2. Mounting method of the device

We gathered information by questionnaire on the mounting method of the device. As a result it is confirmed that 2 companies use the mounting method of both sides mounting, 8 companies use the mounting method of one side mounting. But both sides mounting are the customer request, so we decided on the mounting method of one side with all company's agreements.

3. Printed circuit board

This specification shows the conditions of general printed circuit board. Since an examination result may be affected when it differs from this specification, what is specified in individual specification is recommended.

Appendix 2 Standard mounting process for smd

1. SCOPE

This standard describes a test method for the standard mounting process.

2. TEST BOARD

The mount reliability test board must be as specified in **Appendix 1.**

3. EQUIPMENT FOR MOUNTING

A reflow soldering equipment, such as infrared reflow furnace or hot air reflow furnace, a flow soldering, or solder bath is used for mounting.

4. PROCEDERE

4.1 Pre-treatment

The sample SMD shall be subjected to pre-treatment if it is specified in the detail specification.

4.2 Mounting method

The sample SMD shall be mounted on the printed circuit board as specified in the detail specification. If a mounting method is not specified, the sample SMD shall be mounted using methods I and II. In this case, the soldering temperature for mounting sample shall be limited. The temperature of package shall be checked by measuring method described in **Figure 1** and **Figure 2**.

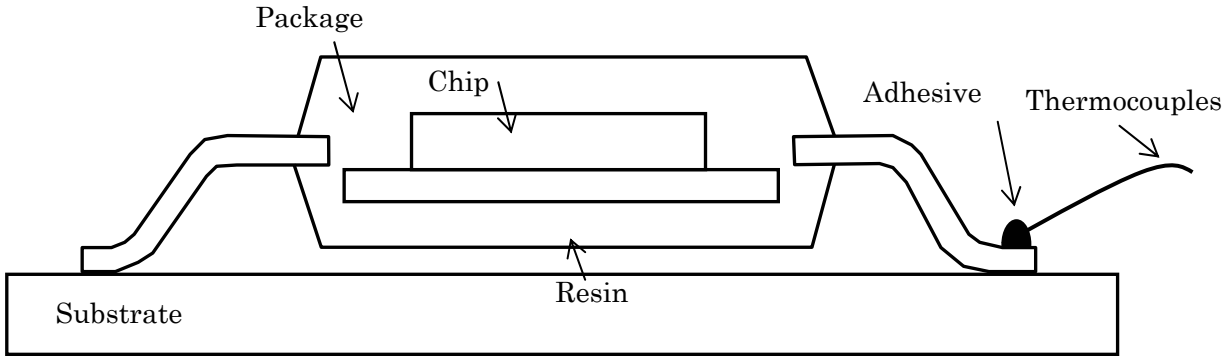


Figure 1 Temperature measurement of the specimen using thermocouples

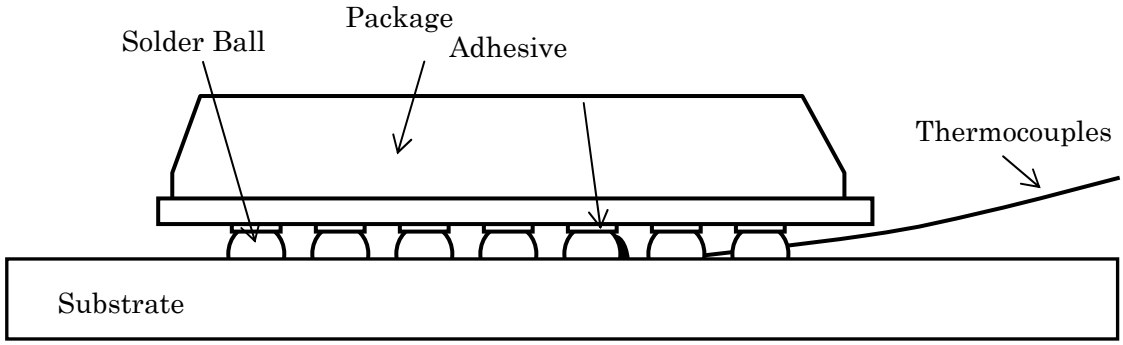


Figure 2 Temperature measurement of the specimen using thermocouples

Method I (Infrared reflow furnace, air reflow furnace)

When mounting a sample SMD with a reflow soldering equipment such as an infrared reflow furnace, follow the procedure specified below.

(a) Preparation 1: Print solder paste to the mounting area on the printed circuit board by thickness of 150 μm ± 50 μm. If a solder bridge is formed after soldering, change cream solder thickness, without being restricted to the above thickness.

(b) Preparation 2: mount a sample SMD on a printed circuit board.

(c) Mount the sample SMD on the printed circuit board with the reflow profile in either condition 1 or condition 2 per **Table 1**.

(d) Removing flux: Remove the flux from sample by cleaning.

Table 1 Heating conditions in Reflow soldering

	Peak temperature	Pre-heated temperature
Condition 1	215~235 °C	140~160 °C
Condition 2	235~260 °C	160~190 °C

Caution

(1) A temperature of reflow furnace is specified by a temperature on a solder joint. It is necessary to take notice in a way that a temperature on a top of package does not exceed guaranteed temperature for mounting.

(2) After mounting, it is necessary to take notice in a way that there aren't any problems with a wetability of solder joint, if there are any problem, review the reflow condition.

(3) In case that a solder joint after mounting is evaluated, if a temperature of reflow furnace is lower than usual, or, if a solder paste is less than usual, it may be gotten a worst result than usual.

Method II (a flow soldering, solder dipping)

When mounting a sample SMD with a reflow soldering equipment such as a flow soldering unit, solder bath, follow the procedure specified below.

(a) Preparation: Bond sample SMD with adhesive to a printed circuit board.

(b) Flux dipping: Apply flux to the leads of the sample SMD.

(c) Cleaning the solder surface: when mounting the sample SMD by solder dipping, clean the solder bath surface with a stainless spatula or another similar tool.

(d) Heating: Select either heating condition from **Table 2**. Take care so that the surface temperature of the sample SMD does not exceed the specified temperature during mounting.

(e) Removing flux: Remove the flux from sample by cleaning.

Table 2 Heating conditions in flow soldering or solder dipping

Soldering temperature	Soldering time
240 °C± 5 °C	5 s ± 1 s
260 °C± 5 °C	5 s ± 1 s

5. MATERIAL

Materials used to mount a sample SMD on printed circuit board is specified in the detail specification. If not specified, the following description shall be applied.

(1) Solder: Solder shall be the one specified in H63A, H60A and H60S in **JIS C 3282** (solder) or appendix B of **IEC** publ. **68-2-20** or an equivalent. Or along with the popularization of lead free, solder shall be lead free solder (such as Tin-Silver-Copper solder).

(2) Flux: Flux shall be 2-propanol (isopropyl alcohol in **JIS K 8839**, **JIS K 1152**, or appendix C of **IEC** publ. **68-2-20**) solution of rosin (in **JIS K 5902** or appendix C of IEC publ**. 68-2-20**) or an equivalent. The concentration of the rosin shall be 10 % to 35 % by weight. Unless otherwise specified, the concentration shall be 25 %.

(3) Cream solder: The solder grain size shall be 200 meshes or less. The material shall be as specified in **(1)** above, or shall provide a higher quality. Flux shall be as specified in **(2)** above, or shall be less active rosin (RMA specified in Federal standard **QQ-S-571** or an equivalent).

(4) Cleaning liquid: Cleaning liquid shall be 2-propanol (isopropyl alcohol) specified in **JIS K 8839** or ethanol (ethyl alcohol) specified **JIS K 8101**.

TEST METHOD 001
Temperature cycle after mounting

1. SCOPE

This standard provides for the accelerated test methods to evaluate the life expectancy of the semiconductor devices and of the soldering joint on the board, by taking into consideration the assumed temperature increase when the SMD packages mounted on the board is working.

2. TEST EQUIPMENT

2.1 Temperature Cycling Test Oven

The temperature cycling test oven shall be air type, which meets the test conditions of the temperature cycle profile specified under section **3.5.3**.

3. PROCEDURE

3.1 Specimen

The specimen shall be used actual device or test package, which is formed daisy chain connection on SMD lead-frame and CSP/BGA substrate.

3.2 Pre-treatment

When required, the pre-treatment shall be carried out according to the conditions specified in the detail specifications.

3.3 Sample Creation

Before carrying out the evaluation test, the specimen specified under section **3.1**. shall be mounted according to the standard mount conditions specified in “Resistance to Reflow Soldering for Test Board”, on the standard mount quality test board specified in “Test Board Design Guideline”.

3.4 Initial measurement

Carry out the initial measurements in conformity with the items and conditions specified in the detail specifications.

3.5 Test

3.5.1 Test methods

Place the specimen in the oven where the good airflow is obtained, and where the sufficient airflow is also obtained around the specimen.

3.5.2 Measurement method

Measure by sampling at the room temperature. The measurement condition shall be carried out for the items and under the conditions, those specified in the detail specifications. It is recommended that, as much as possible, the electrical resistance of the specimen at maximum and minimum storage temperature to be measured continuously during the test.

3.5.3 Test conditions

Figure1 defines the test of one cycle. According to **Table 1**, the specimen shall be tested starting at low temperature. The test equipment shall be set so that the temperature of the specimen is set to the values specified in **Table 1**.

Table 1 Temperature cycling test conditions

Step	Test condition A	Test condition B	Test condition C	Test condition D	Test condition E
Minimum storage temperature ($Tstg_{min}$)	-30 °C (+0/-10 °C)	-25 °C (+0/-10 °C)	-40 °C (+0/-10 °C)	-65 °C (+0/-10 °C)	Top_{min} °C (+0/-10 °C)
Maximum storage temperature ($Tstg_{max}$)	+80 °C (+10/-0 °C)	+125 °C (+15/-0 °C)	+125 °C (+15/-0 °C)	+125 °C (+15/-0 °C)	Top_{max} °C (+10/-0 °C)
Hold time	At least 7 minutes				

Notes : Top_{min} ; Minimum operating temperature

Top_{max} ; Maximum operating temperature

The hold time starts when the temperature of the specimen reaches the specified value.

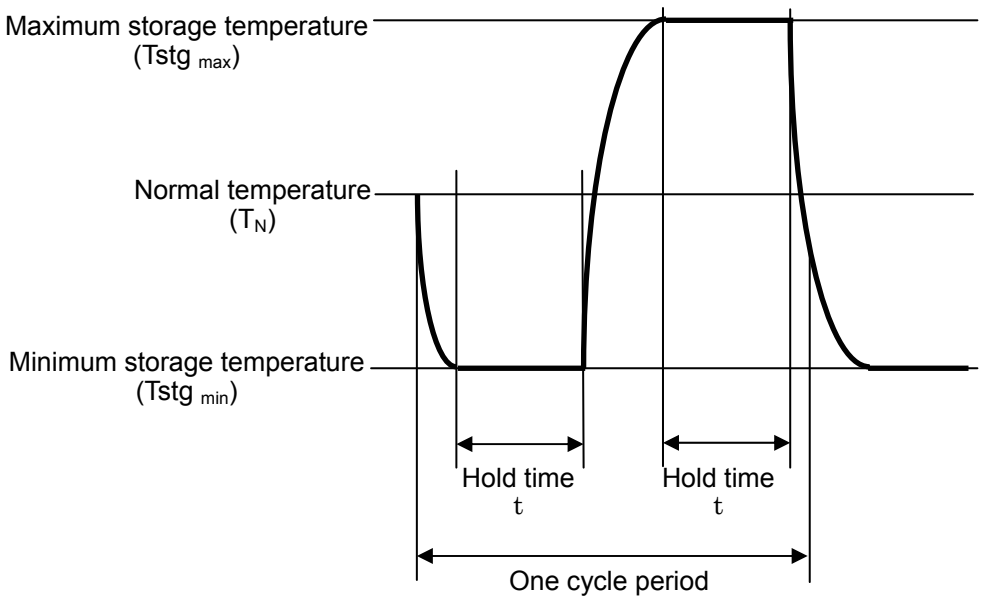


Figure 1 Configuration of one cycle period

3.6 Post treatment

After finishing the test, if necessary, the specimen should be left under the standard conditions for the time specified in the detail specifications.

3.7 End-point measurements

Carry out the end-point measurements in conformity with the items and conditions specified in the detail specifications.

In this test, the printed circuit board, solder ability, and the SMD may cause complex effects. If a failure occurs, check whether it is caused by the SMD itself and take appropriate action.

4. INFORMATION TO BE GIVEN IN THE DETAIL SPECIFICATION

(1) Preliminary treatment(when required) [Refer to section **3.2**]

(2) Specification of mount quality test board(when not specified) [Refer to section **3.3**]

(3) Mount conditions(when not specified) [Refer to section **3.3**]

(4) Items and conditions of initial measurement [Refer to section **3.4**]

(5) Test conditions [Refer to section **3.5.3**]

(6) Time to leave the specimen at normal temperature [Refer to section **3.5.3**]

And at low and high temperature (when any conditions Other than those specified are applied)

(7) Whether or not to continuously monitor [Refer to section **3.5.2**]

The electrical resistance

(8) Number of repetition cycles [Refer to section **3.5.3**]

(9) Post treatment(when required) [Refer to section **3.6**]

(10) Item and conditions of the end-point measurement [Refer to section **3.7**]

(11) Criterion [Refer to section **3.7**]

COMMENTS TEMPERATURE CYCLING FOR SOLDERING JOINT

This comments gives a supplemental explanation to the temperature cycling test for soldering joint, but it shall not be considered as part of the specification in the standard. It explains the temperature cycling test for soldering joint for the life of the semiconductor devices and the joint on the board affected by the temperature rise expected when the semiconductor devices as SMD packages being mounted on the board are working.

A part of these comments is quoted from **EIAJ ET-7407** ”Environmental and endurance test methods for CSP/BGA package on mounting condition”. As a result of the discussion, the part was quoted from the agreement of **EIAJ ET-7407 Annex 2** (reference) ”Temperature Cycling Test for Soldering Joint (Explanation)” to the content of this explanation.

1. ABOUT ACCELERATION OF THE TEMPERATURE CYCLING TEST

The temperature cycling test specified in **Test method 001** is mainly applied when obtaining the temperature cycle life at the soldering joint between the component and the board. The Manson-Coffin's law (1) is often used to obtain the heat fatigue life of the soldering joint.

$$N \propto (\Delta \varepsilon)^{-n} \qquad (1)$$

Where:N is breaking life, $\Delta \varepsilon$ is heat fatigue strain amplitude, and n is a constant (stress parameter) determined by the material.

From the equation (1), it is known that the soldering life is proportional to n-th power of the heat fatigue strain amplitude. For the temperature cycling acceleration test specified in the standard, the evaluation is made under more severe conditions than actual operating conditions regarding the maximum and minimum temperatures and the number of ON/OFF cycles. It is necessary to measure the effect of these factors on the heat fatigue life. Properly speaking, equation (1) shall be used. However, using the modified Manson-Coffin's law already proposed, the heat fatigue life at the soldering joint can be conveniently expressed as shown in equation (2).

$$N = C \times f^{m} \times (\Delta \varepsilon)^{-n} \times \exp\left(\frac{H}{kT_{\max}}\right) \qquad (2)$$

Where:C is a constant, f is On/Off frequency, m is a frequency parameter which is normally 1/3, k is a boatman’s constant, H is activation energy, and T_{max} is the maximum test temperature.

In the modified equation, the heat fatigue strain amplitude $\Delta \varepsilon$ can be approximated and be expressed as follows:

$$\Delta \varepsilon = \alpha \times \lambda \times \Delta T \times \left[\frac{V}{\pi r^{2} h^{1+\beta}}\right]^{1/\beta} \qquad (3)$$

Where:α is the linear expansion coefficient, λ is DNP (the distance to neutral point), ΔT is the temperature variation in the temperature cycle, V is the solder volume at the soldering joint, r is the radius of the bump, and ? is the shear strain and shear stress which is expressed τ =k × εβ.

According to equations (1), (2), and (3), acceleration factor AF of the two different conditions is given as follows:

$$AF = \left[\frac{f_f}{f_t}\right]^m \times \left[\frac{\Delta T_f}{\Delta T_t}\right]^{-n} \times \exp\left[\frac{H}{K} \times \left(\frac{1}{T_{\max - f}} - \frac{1}{T_{\max - t}}\right)\right] \quad (4)$$

Where:f_f, and f_t are the number of On/Off cycles in the field and under test conditions, respectively, ΔT_f, and ΔT_t are temperature variation in the field test and under test conditions, respectively, $T_{max\text{-}f}$ and $T_{max\text{-}t}$ are the maximum temperatures in the field test and under test conditions, respectively, H is the activation energy of the solder which is 0.123 eV, K is a Boltzmanns constant, m is 1/3, and n is **1.9.**

Propriety of acceleration characteristic of equation (4) in the market was discussed.

During development stage of the standard, propriety of acceleration equation was also discussed. Under the temperature cycling test conditions shown in **Table 1**, a majority said that there was correlation with the assumed conditions in the market; therefore, the acceleration equation was employed.

2. TEST CONDITIONS

There were several proposals made during discussion for selection of the test conditions. The list below shows why the test conditions described in Test method 001 were so specified.

The temperature cycling test conditions are:

- to be set so that the maximum storage temperature does not significantly exceed T_g of FR-4 board because an organic board is often used as the mount reliability test board for SMD packages.
- to be set so that the assumed conditions on the market and the failure modes can be simulated.
- to be set so that the acceleration characteristic which is proportional to that on the market can be simulated.
- to be set so that they are correlated to and considerably similar to existing standards of the same scope.
- to be set so that the time required for the test can be made shorter.

As test condition A, the maximum storage temperature of 80 °C and the minimum storage temperature of - 30 °C were specified. These temperatures adopted by car manufacturers were additionally noted as one of the test conditions.

As test condition B, the maximum storage temperature of 125 °C and the minimum storage temperature of - 30 °C were specified. A temperature of 125 °C is close to T_g of the board and is conventionally used as the maximum storage temperature. A temperature of - 25 °C was specified because it was reported as an example that the linear acceleration characteristic became faulty with the minimum temperature set around - 30 to – 40 °C.

As test condition C, the maximum storage temperature of 125 °C and the minimum storage temperature of - 40 °C were specified. These temperatures were specified in **JIS C 0025**, and were widely adopted by the equipment manufacturers, as it was shown, as the outcome of the sent-out questionnaire regarding standardization of connection reliability evaluation, in "Environmentally harmonized mount technology survey and research report" published in 1998 by Japan Electronic Industry Development Association (**JEIDA**).

As test condition E, the maximum storage temperature of 125 °C and the minimum storage temperature of - 65 °C were specified to take ΔT greatly, and to shorten the examination time. A temperature of 125 °C is close to T_g of the board and is conventionally used as the maximum storage temperature. A temperature of - 65 °C is used by evaluating the product as the lmaximum storage temperature.

However, it is necessary to note enough acceleration and failure mode because it was reported as an example that the linear acceleration characteristic became faulty with the minimum temperature set around - 30 to - 40 °C.

As test condition E, the maximum operating temperature Top_{max} and the minimum operating temperature Top_{min} were specified by considering the actual environment on the market.

In particular, it is preferable to use test condition B if there is no doubt of the acceleration characteristic of the simulated condition with respect to the actual condition on the market. A variety of proposals were also made on the hold time. The majority of the committee members said that it was learnt by experience that there is no doubt of the test result when stored at the maximum or minimum temperature for 7 minutes.

Then, the hold time was specified as 7 minutes at least.

The time required for the test was not specified because it was impossible to specify the hold time with number of operating conditions and of to-be-guaranteed conditions, existing on the market. The acceleration characteristic on the market can be calculated using equation (4). As a reference, **Table1** shows the result of the calculation of the acceleration characteristic of both the test conditions and the typical conditions on the market.

Comment Table 1 Relation between the test condition and the time for the test of the acceleration characteristic

Acceleration test condition					Accele-ration factor	The number of test cycles	
Test condition	Max. storage temperature $Tstg_{max}$	Min. storage temperature $Tstg_{max}$	ΔT	On/Off frequency		Equivalent to 5 years on the market	Equivalent to 10 years on the market
Condition A	80 °C	- 30 °C	110 °C	72cyc/day	1.5	1,217cycle	2,433cycle
Condition B	125 °C	- 25 °C	150 °C		4.2	435cycle	869cycle
Condition C	125 °C	- 40 °C	165 °C		5.0	365cycle	730cycle
Condition D	125 °C	- 65 °C	190 °C		6.6	277cycle	553cycle
Condition on the market	70 °C	25 °C	45 °C	1cyc/day	1.0	1,825cycle (5 years on the market)	3,650cycle (10 years on the market)

Note: Calculation was made assuming the hold time at maximum and minimum storage temperatures set to 7 minutes, and the exchange time from maximum storage temperature to minimum storage temperature and vice versa set to 1.5 minutes.

For analysis of the test data, it is desirable to carry out the statistical process in Weibull distribution. Regarding the accelerated characteristic of the life of the soldering joint, it is proposed that calculation shall be made as a simulation by calculating the heat fatigue strain at the soldering joint, not by using equation (4) adopted by the standard. However, it is necessary for the simulation to be carried out with huge calculation using the finite element solution method. At present, this is not practical. So, the standard has adopted equation (4) for the accelerated characteristic.

3. TEST CONDITION PROPOSAL DURING DISCUSSION

There were several proposals made during discussion for selection of the test conditions. **Table 2** shows the test conditions proposed.

Comment Table 2 Temperature cycling test conditions proposed during discussion

	Test condition				questionnaire survey
	Minimum storage temperature	Maximum storage temperature	ΔT	Hold time	
1	- 55 °C	+ 125 °C	180 °C	20 min	1 company
2	- 40 °C		165 °C	7~30 min	3 companies
3	- 25 °C		150 °C	7~10 min	4 companies
4	0 °C		125 °C	10 min	1 company
5	- 10 °C	+ 110 °C	120 °C	–	1 company
6	- 35 °C	+ 105 °C	140 °C	–	1 company
7	- 40 °C	+ 85 °C	125 °C	30 min	2 companies

4. MEASUREMENT METHOD

As for the measurement method, the sampling method and the continuous electric resistance monitoring system were discussed. In the case of the sampling method, actual device is mainly measured. In the case of continuous electric resistance monitoring system, daisy chain sample is mainly measured. Since the use of continuous electric resistance monitoring system is required for the improvement of test environment, it is not practical at present. Therefore, measuring by the sampling method was agreed during discussion.

However, a failure occurred at high temperatures as “Open” indicated by infinite electrical resistance but it recovered as normal at normal temperatures. For the sampling method, measuring the heated specimen is effective.

5. ABOUT THE FACTOR, WHICH AFFECTS THE LIFE OF THE SOLDERED PART

Of the board, the thickness and the layer configuration, as well as the mount congestion on the board, largely affect the temperature cycle life of the soldering joint with the component being mounted on the board. It is well known that the life of soldering becomes about a half when in particular the packages of area pin type are mounted on the same area of both sides of the board. [3], [4]. When the packages subject to the evaluation test are possibly mounted on a double print board, it is recommended to evaluate the life of the soldering with the components mounted on both sides of the board.

6. SPECIMEN

As for the specimen, substrate daisy chain, chip daisy chain and actual device were discussed. As a result of the discussion, actual device or substrate daisy chain was selected for considering the specimen cost.

7. JUDGMENT METHOD

A variety of proposals on judgment method were made during discussion.

Table 3 shows the judgment method proposed.

Comment Table 3　Judgment method proposed

Judgment condition	Criteria	Measurement condition	Questionnaire survey
1	10% change or more from initial value	Continuous monitoring	2 companies
2	10% change or more from initial value	Sampling at the room temperature	4 companies
3	10% change or more from initial value	Continuous monitoring or sampling at the room temperature	1 company
4	50% change or more from initial value	Continuous monitoring or sampling at the room temperature	1 company
5	100% change or more from initial value	Sampling at the room temperature. The measurement at high temperature is added when the electric resistance changes.	1 company

As a result of the discussion, each company specifies judgements under many kinds of conditions in detail specification.

8. EXPLANATION OF TERM

Substrate daisy chain : test package which is formed daisy chain connection on SMD lead-frame and CSP/BGA substrate.

Chip daisy chain : test chip which is patterned daisy chain connection in package mounted on SMD lead-frame and CSP/BGA substrate.

TEST METHOD 002
Strength tests for soldering joint

METHOD 1 Peel strength test for soldering joint

1. SCOPE

This standard provides for endurance test methods to evaluate the endurance of peel strength between SMD and printed wiring board against mechanical stress is applied from vertical direction in some external mechanical stress.

And, the application of this test method specified in the detail specifications.

Note: This test method considers the following situation in field use.

(1) In case that the attached seal on device surface was peeled off.

(2) In case of the structure, like a surface mount type connector, basically premised on receiving external mechanical tress.

(3) In case that a tall SMD such heat sink attached SMD was applied external mechanical stress under handling of SMD mounted board.

2. TEST EQUIPMENT

The equipment and tools in this test shall meet the test conditions specified under section **3.5**.

3. PROCEDURE

3.1 Specimen

The specimen shall be used actual device or test package which is formed daisy chain connection on SMD lead-frame and substrate of BGA, LGA, SON, and so on.

3.2 Pre-treatment

When required, the pre-treatment shall be carried out according to the conditions specified in the detail specifications.

3.3 Sample creation

Before carrying out this endurance test, the specimen specified under section **3.1**. shall be mounted according to the standard mount conditions specified in **Appendix 2**, on the standard mount quality test board specified in **Appendix 1**.

3.4 Initial measurement

Carry out the initial measurements in conformity with the items and conditions specified in the detail specifications.

3.5 Test

Peel load of this test shall be applied by the following method. The specimen shall be fixed, and specimen SMD or the attached pull tool on specimen SMD surface shall be caught, in **Figure 1**. However, in case of heat sink attached SMD, heat sink shall be caught. When required, 5N of peel load shall be applied during 10 +/- 1 second. The axis of peel load shall be within 5 degree against vertical direction.

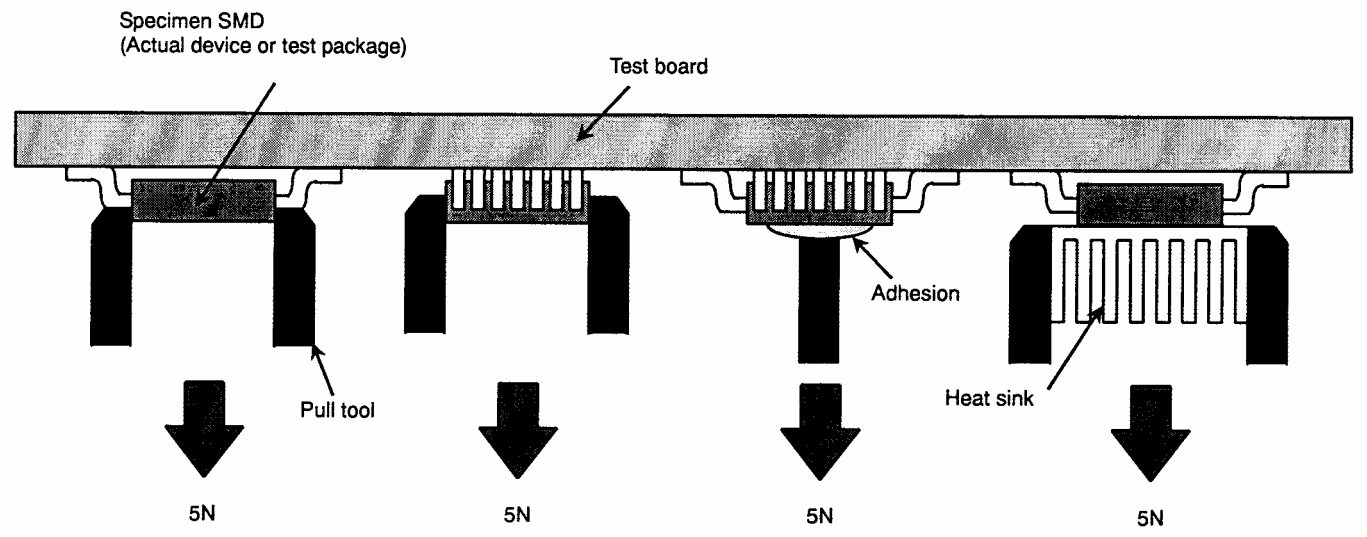


Figure 1 Method of peel load

3.6 Post treatment

After finishing the test, if necessary, the post treatment of the specimen should be carried out according to the conditions specified in the detail specifications.

3.7 End-point measurements

Carry out the end-point measurements in conformity with the items and conditions specified in the detail specifications.

Because this test might be affected by complex cause of substrate material, solderability, SMD, and so on, the failure shall be conformed whether SMD has root cause or not, when failure occurred.

4. INFORMATION TO BE GIVEN IN THE DETAIL SPECIFICATION

(1) Pre-treatment condition (when required) [Refer to section **3.2**]

(2) Specification of mount quality test board (when not specified) [Refer to section **3.3**]

(3) Mount conditions (when not specified) [Refer to section **3.3**]

(4) Items and conditions of initial measurement (when required) [Refer to section **3.4**]

(5) Test conditions (when not specified) [Refer to section **3.5**]

(6) Post treatment condition (when required) [Refer to section **3.6**]

(7) Item and conditions of the end-point measurement [Refer to section **3.7**]

(8) Failure criteria [Refer to section **3.7**]

(9) The other needful items

5. Reference

Because this test shall be performed under actual use condition essentially, this standard provided the endurance test method is instead of actual use condition as similar as possible.

As the other method for lead less parts, there is the test method applies load from back side through the hole of test board. However, because the test method is not reality and needs the test board meets to package dimension in SMD case, this standard did not provide. Also, this standard did not provide the test method that cut leads of one side of SMD and deform the cut leads to vertical direction against printed wiring board, because this test is not reality.

METHOD 2 Pull strength test for soldering joint

1. SCOPE

This standard provides for endurance test methods to evaluate the endurance of pull strength for soldering joint between SMD and printed wiring board at SMD mounted board

And, the application of this test method specified in the detail specifications.

2. TEST EQUIPMENT

The equipment and tools in this test shall meet the test conditions specified under section **3.4.**

3. PROCEDURE

3.1 Specimen

The specimen shall be used actual device or test package which is formed daisy chain connection on SMD lead-frame and substrate of BGA, LGA, SON, and so on.

3.2 Pre-treatment

When required, the pre-treatment shall be carried out according to the conditions specified in the detail specifications.

3.3 Sample creation

Before carrying out this endurance test, the specimen specified under section **3.1**, shall be mounted according to the standard mount conditions specified in **Appendix 2**, on the standard mount quality test board specified in **Appendix 1**.

3.4 Test method

3.4.1 Specimen fixture

The specimen shall be fixed at slope to 45 degree, in **Figure 1**.

3.4.2 Specimen preparation

The lead of specimen shall be hooked the wire for pull, in **Figure 1**. However, if the wire cannot be hooked when the lead of specimen is very small, the strength of soldering joint shall be evaluated by push strength test for soldering joint.

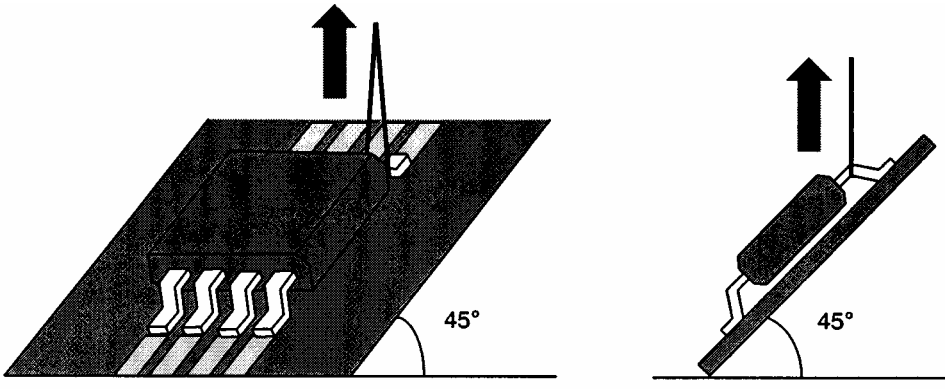


Figure 1 Specimen fixture and test method

3.4.3 Measurement

The wire shall be pulled up at speed of 5 through 30 mm/min, in **Figure 1**. When soldering joint break, the strength shall be measured.

Note: In **Figure 2**, the leads are pulled up by turns and this operation raised up the package. This phenomenon might affect to broken strength data. Therefore, the availability of the data shall be confirmed.

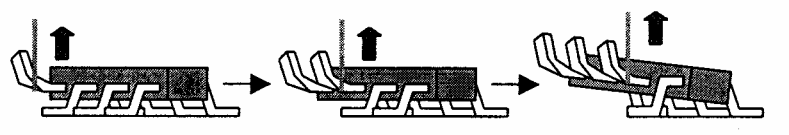


Figure 2 Attention for pull test method

3.5 Post treatment

After finishing the test, if necessary, the post treatment of the specimen should be carried out according to the conditions specified in the detail specifications.

3.6 End-point measurements

Carry out the end-point measurements in conformity with the items and conditions specified in the detail specifications.

When not required, the criteria of pull strength for a lead shall be more than 5N (pull load)/ lead counts of the package. Because this test might be affected by complex cause of substrate material, solderability, SMD, and so on, the failure shall be conformed whether SMD has root cause or not, when failure occurred.

4. INFORMATION TO BE GIVEN IN THE DETAIL SPECIFICATION

(1) Pre-treatment condition (when required) [Refer to section **3.2**]

(2) Specification of mount quality test board (when not specified) [Refer to section **3.3**]

(3) Mount conditions (when not specified) [Refer to section **3.3**]

(4) Test conditions (when not specified) [Refer to section **3.4**]

(5) Post treatment condition (when required) [Refer to section **3.5**]

(6) Item and conditions of the end-point measurement [Refer to section **3.6**]

(7) Failure criteria [Refer to section **3.6**]

(8) The other needful items

METHOD 3　Push strength test for soldering joint

1. SCOPE

This standard provides for endurance test methods to evaluate the endurance of push strength (fixedness) between SMD and printed wiring board at SMD mounted board against mechanical stress is applied from side direction in some external mechanical stress.

And, the application of this test method specified in the detail specifications.

Note: This test method considers the following situation in field use.

(1) In case of the structure, like a surface mount type connector, basically premised on receiving external mechanical tress.

(2) In case that a tall SMD such heat sinks attached SMD was applied external mechanical stress under handling of SMD mounted board.

2. TEST EQUIPMENT

The equipment and tools in this test shall meet the test conditions specified under section **3.5**.

3. PROCEDURE

3.1 Specimen

The specimen shall be used actual device or test package which is formed daisy chain connection on SMD lead-frame and substrate of BGA, LGA, SON, and so on.

3.2 Pre-treatment

When required, the pre-treatment shall be carried out according to the conditions specified in the detail specifications.

3.3 Sample creation

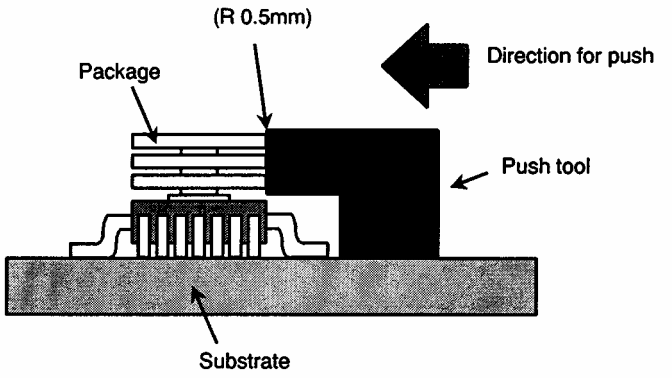
Before carrying out this endurance test, the specimen specified under section **3.1**. shall be mounted according to the standard mount conditions specified in **Appendix 2**, on the standard mount quality test board specified in **Appendix 1**.

3.4 Initial measurement

Carry out the initial measurements in conformity with the items and conditions specified in the detail specifications.

3.5 Test

The specimen shall be fixed, and the push load shall be applied to the highest portion of specimen SMD from horizon direction against printed wiring board of specimen by push tool, in **Figure 1** and **2**. When not required, push load shall be 5 N and hold time shall be 10 +/- 1 second. In the case of dual lead package such SOP and so on, the push load shall be applied to middle of no lead side of the package, in **Figure 2**. And in the case of quad lead package such QFP and so on, the push load shall be applied to the middle of 2 side at different direction.



Fugure 1 Push direction (side view)

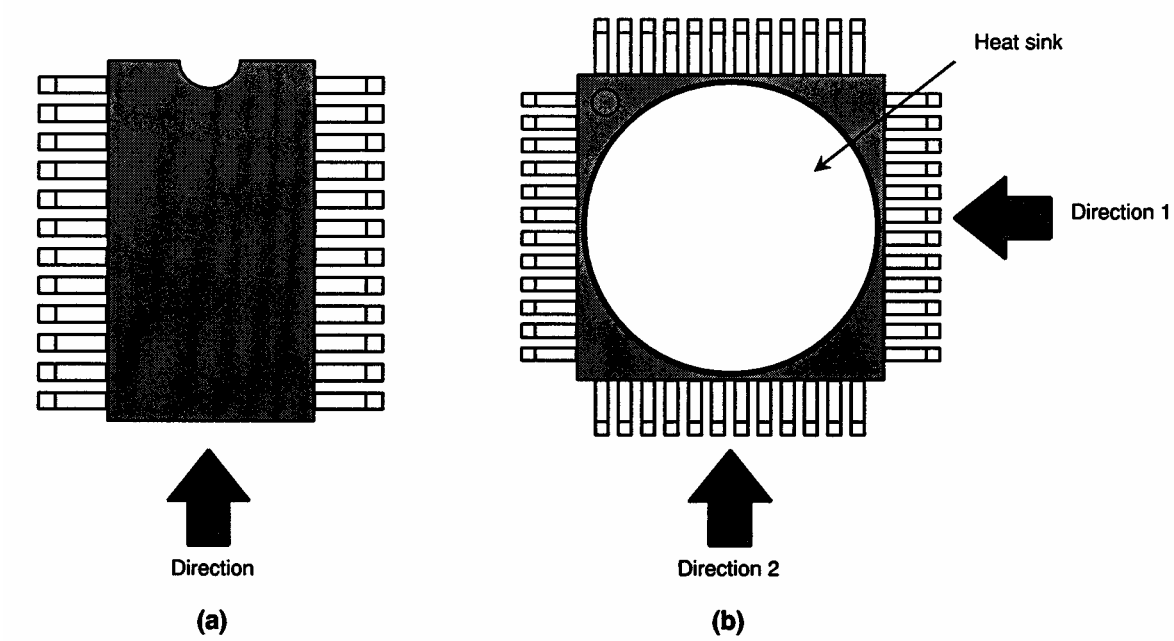


Figure 2 Push direction (top view)

3.6 Post treatment

After finishing the test, if necessary, the post treatment of the specimen should be carried out according to the conditions specified in the detail specifications.

3.7 End-point measurements

Carry out the end-point measurements in conformity with the items and conditions specified in the detail specifications.

Because this test might be affected by complex cause of substrate material, solderability, SMD, and so on, the failure shall be conformed whether SMD has root cause or not, when failure occurred.

4. INFORMATION TO BE GIVEN IN THE DETAIL SPECIFICATION

(1) Pre-treatment condition (when required) [Refer to section **3.2**]

(2) Specification of mount quality test board (when not specified) [Refer to section **3.3**]

(3) Mount conditions (when not specified) [Refer to section **3.3**]

(4) Items and conditions of initial measurement (when required) [Refer to section **3.4**]

(5) Test conditions (when not specified) [Refer to section **3.5**]

(6) Test tool (when not specified) [Refer to section **3.5**]

(7) Post treatment condition (when required) [Refer to section **3.6**]

(8) Item and conditions of the end-point measurement [Refer to section **3.7**]

(9) Failure criteria [Refer to section **3.7**]

(10) The other needful items

TEST METHOD 003
Bending test for surface mount devices on the board

1. SCOPE

The test shall specify a procedure for evaluating the resistance of the surface mount device (SMD) and soldered joints to the stress caused by a bent printed circuit board (PCB) mounted SMDs. This test is mainly applied to BGA, LGA, SON type package and so on.

2. TEST EQUIPEMNET, TOOLS AND JIGS

The equipment and tools used in this test shall conform to **3.6**.

3. TEST PROCEDURE

3.1 Test samples

Test sample is a device or a daisy chained package. A daisy chained package are composed of a wired leadframe or a package applied to BGA, LGA, SON, and so on soldering on a printed circuit board.

3.2 Pre-treatment

Perform pre-treatment for the sample SMD as specified in the detail specifications, if necessary.

3.3 Preparation of a sample

Solder an SMD on a printed circuit board as specified in **APPENDIX 001** and **APPENDIX 002.**

3.4 Initial measurement

Check the electrical and/or mechanical characteristics specified in the detail specification.

3.5 Placement

Place the printed circuit board mounted sample SMD on a support as shown in **Figure 1.** The support must be on a flat and rigid test table so that is not affected by an applied pressure.

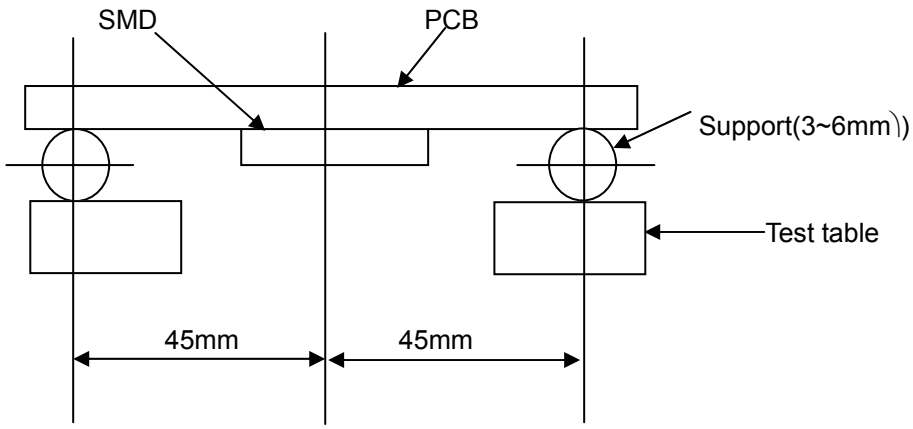


Figure 1 Placement

3.6 Test condition

Use the tool shown in **Figure 2**, apply the load to the printed circuit board mounted the sample SMD by method shown **Figure3**. The material of the support must have no deformation under pressure. The mount of deflection is 1.0 mm ± 0.5 mm, 2.0 mm ± 0.5 mm, 3.0 mm ± 0.5 mm or 4.0 mm ± 0.5 mm. These values are not specified. Press the tool with deflection speed of 1 mm/sec., until the specified deflection is reached. Replace at an initial position with the same speed. Unless otherwise specified, perform this test only once. The deflection to press is only X deflection.

(1) Deflection speed: 1.0 mm/sec

(2) Amount of deflection: 1.0 mm±0.5 mm, 2.0 mm±0.5 mm, 3.0 mm±0.5 mm, 4.0 mm±0.5 mm(Reference)

(3) Material and shape of the support cylinder: 3~6 mm〉

(4) Span:90 mm ± 3 mm

(5) Direction for test:bottom of PCB

(6) Front edge shape and metal of tool for bending:R 230 (hardened steel or hard metal)

Remarks: When a printed circuit board mounted a too large SMD is bent, the surface of the printed circuit board presses the backside of the SMD. In this case, an excessive force is applied to the SMD, as a result, disconnecting of soldered portions, deforming or cutting of lead happens. This status never occurs in actual use. Take care when setting an amount of deflection.

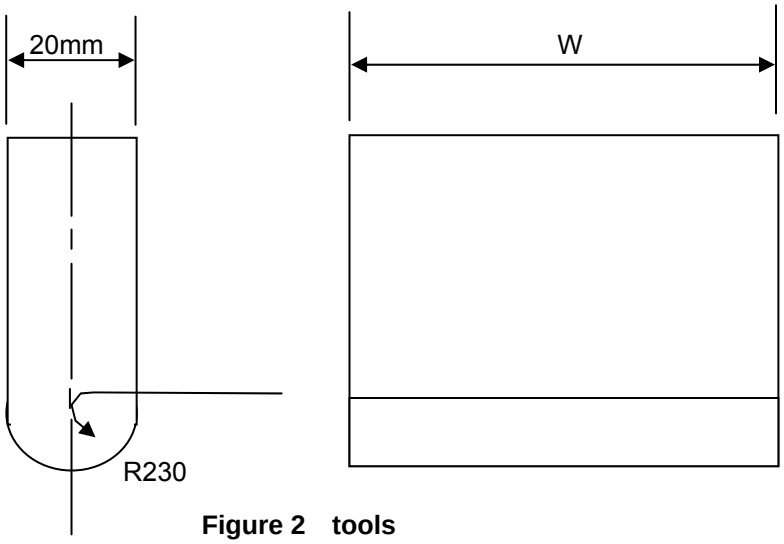


Figure 2 tools

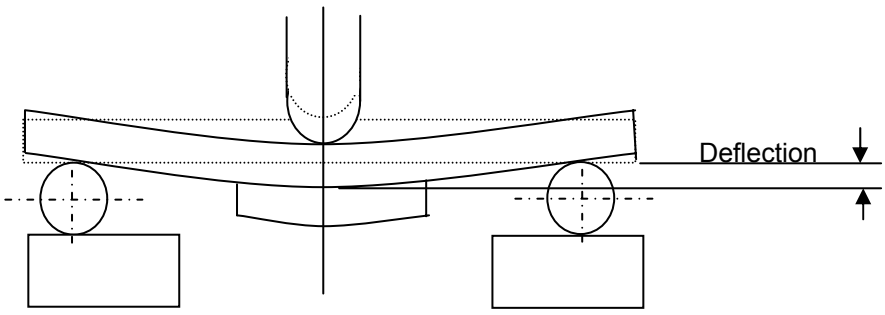


Figure 3 Pressuring

3.7 Post-treatment

Perform post-treatment for samples SMD as specified in the detail specification, if necessary.

3.8 Final measurement

Check the electrical and/or mechanical characteristics specified in the detail specification. Electrical characteristics should be checked holing the specified deflection for 5 sec±1 sec. If a failure occurs, check whether it is caused by the SMD itself and deal with appropriate action.

4. INFORMATION TO BE GIVEN IN THE DETAIL SPECIFICATIONS

(1) Pre-treatment [refer to **3.2**]

(2) Printed circuit board for mounting SMD [refer to **3.3**]

(3) Soldering condition [refer to **3.3**]

(4) Items and conditions in initial measurements [refer to **3.4**]

(5) Test conditions [refer to **3.6**]

(6) Amount of deflection [refer to **3.6**]

(7) Monitoring [refer to **3.6**]

(8) Post-treatment [refer to **3.6**]

(9) Items and conditions in final measurements [refer to **3.7**]

(10) Criteria [refer to **3.8**]

(11) Other required items

EIAJ ED-4702A

DESCRIPTION BENDING TEST FOR SURFACE MOUNT DEVICES ON THE BOARD

1. HISTORY OF DELIBERATION

Recently there are many downsized package for cellular phone and mobile devices as technology trends and market trends. A bending stress may occur to a solder joint on the printed circuit when key on the keyboard is pressed. This standard is specified of a bend stress of solder joint on a printed circuit board as a part of standard of a reliability test method.

2. ANSWERS IN RESPONSE TO QUESTIONNAIRES

During discussion, there are many opinions about the test method, the test condition and the criteria. Answers in response to questionnaires addressed by the CSP/FC PG.

[Test condition of a bending test for the surface mounted devices on the printed circuit board during discussion]

(1) Company standard	: established(3), unestablished(6)
(2) Experiences	: Yes(6), No(3)
(3) Board design	: the same board for temperature cycling(2)
(4) Bending speed	: 8 mm/min(1), 1 mm/min(1), 5 mm/min(2)
(5) Amount of deflections	: lead to breakdown(4), 1 mm ~ 3 mm(limit)(1)
(6) The shape of the support	: cylinder(5)
(7) Span	: 90 mm(3), 50 mm(1), 45 mm(1)
(8) A bending direction	: solder side(5), component side(1)
(9) Measurement	: continuous monitoring(4), interval(1)
(10) Numbers of points to press	: two points at component side(3), one point at solder side (1), two points at solder side (2)
(11) Criteria	: 10 % and above(4), 100 % and above(1)

3. MESUREMENT

The methods of measurement are discussed about the measurement at interval of some cycles and the continuous monitoring. In the first mentioned case, actual devices are measured. In another case, daisy chained packages as a test equipment element is measured. Because it is necessary to improve infrastructure for continuous monitoring, it is not general. The members of this PG agreed that the measurement at interval of some bending cycles is used. It is recommended electric characteristics should be checked holing the specified deflection. A step stress of amount of deflections with 1.0 mm, 2.0 mm, 3.0 mm, and 4.0 mm were adopted. But their values are not specified, because an actual stress is unknown in the process of actual fabrication. And to check out limit deflection, it is discussed that to measure electrical characteristics while changing amount of deflections.

4. SUPPLEMENT

The span of support tools is able to be changed with the size of PCB. Even the same specified amount of deflection is applied, the stress on joint in the case of span 50 mm is not the same stress in the case of span 90 mm,because of the radius of curvature of PCB is not the same. Each amount of deflection applied to the same stress of joint is selected in the case of each span. The radius of curvature of PCB can be shown as follows:

$$R = (L^2+4H^2)/8H \qquad (1)$$

Where L (mm) is span of support H (mm) is amount of deflection.

Table 1

A comparison of an amount of deflection in the case of span 90mm and in the case of span 50mm

	Span 90 mm	Span 50 mm
Deflection	1 mm	0.3 mm
	2 mm	0.6 mm
	3 mm	0.9 mm
	4 mm	1.2 mm

TEST METHOD 004
Reiterative bending test for surface mount devices on the board

1. SCOPE

The test shall specify a procedure for evaluating the resistance of the surface mounts device (SMD) and soldered joints to the bent stress again and again caused by a key touch. This test is mainly applied to BGA, LGA, SON type package and so on for cellular phone and PDA.

2. TEST EQUIPEMNET, TOOLS AND JIGS

The equipment and tools used in this test shall conform to **3.6**.

3. TEST PROCEDURE

3.1 Test samples

Test sample is a device or a daisy chained package. A daisy chained package are composed of a wired leadframe or a package applied to BGA, LGA, SON, and so on soldering on a printed circuit board.

3.2 Pre-treatment

Perform pre-treatment for the sample SMD as specified in the detail specifications, if necessary.

3.3 Preparation of a sample

Solder an SMD on a printed circuit board as specified in **APPENDIX 001** and **APPENDIX 002.**

3.4 Initial measurement

Check the electrical and/or mechanical characteristics specified in the detail specification.

3.5 Placement

Place the printed circuit board mounted sample SMD on a support as shown in **Figure 1**. The support must be on a flat and rigid test table so that is not affected by an applied pressure.

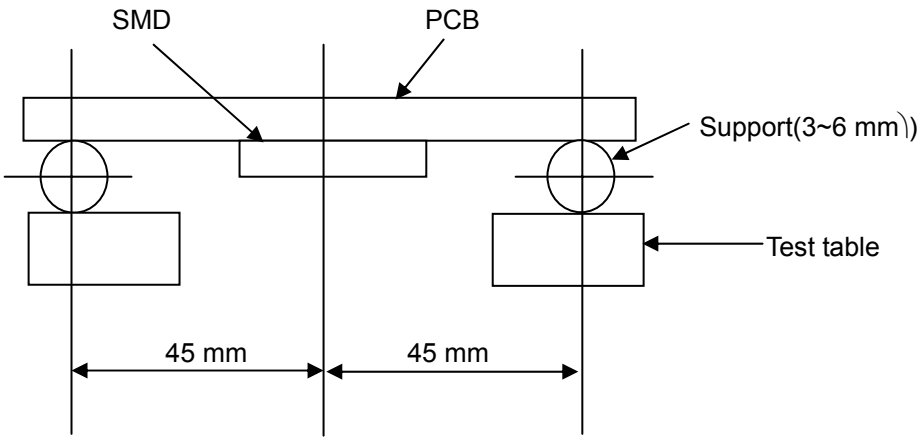


Figure 1 Placement

3.6 Test condition

Use the tool shown in **Figure 2**, apply the load to the printed circuit board mounted the sample SMD by method shown **Figure 3**. The material of the support must have no deformation under pressure. The mount of deflection is chosen from either 1mm or 2 mm with its tolerance of ± 0.5 mm. These values are not specified. Press the tool with deflection speed of 1 mm/sec., until the specified deflection is reached. Replace at an initial position with the same speed. Repeat the cycles specified in the detail specifications. The deflection to press is only X delection.

(1) Deflection speed : 1.0 mm/sec

(2) Amount of deflection : 1.0 mm±0.5 mm,2.0 mm±0.5 mm,(Reference)

(3) Material and shape of the support : 3~6 mmφ(hardened steel or hard metal)

(4) Span : 90 mm±3 mm

(5) Direction for test : bottom of PCB

(6) Front edge shape and metal of tool for bending : R 230(hardened steel or hard metal)

Remarks

(1) Adequately select a number of cycles as usage

(2) When a printed circuit board mounted a too large SMD is bent, the surface of the printed circuit board presses the backside of the SMD. In this case, an excessive force is applied to the SMD, as a result, disconnecting of soldered portions, deforming or cutting of lead happens. This status never occurs in actual use. Take care when setting an amount of deflection.

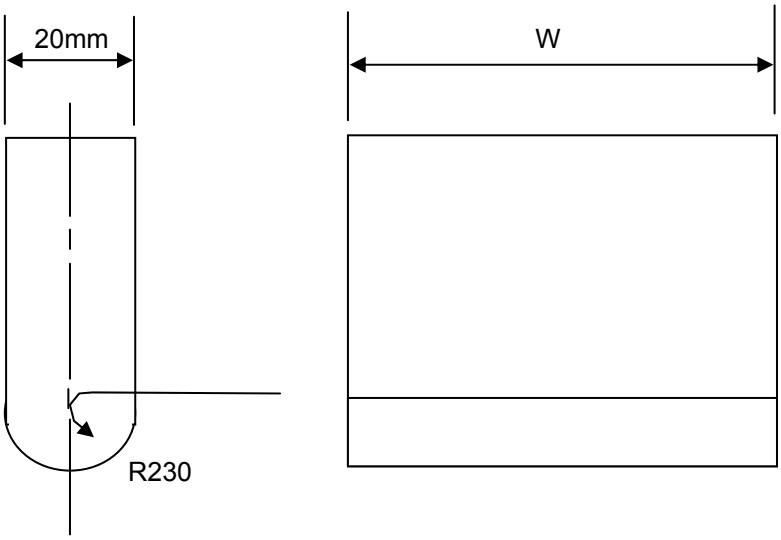


Figure 2 tool

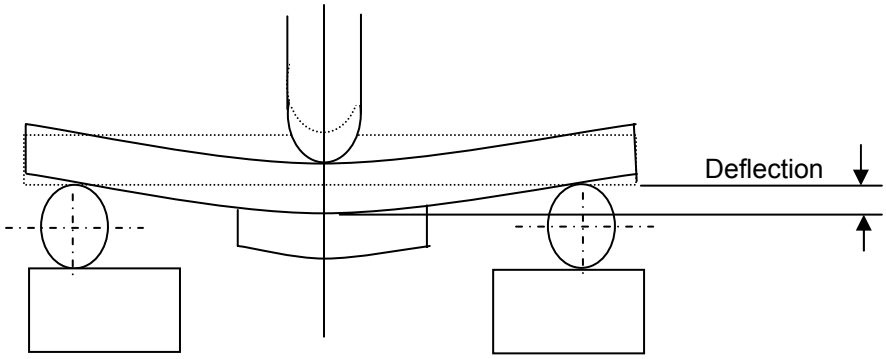


Figure 3 Pressuring

3.7 Post-treatment

Perform post-treatment for samples SMD as specified in the detail specification, if necessary.

3.8 Final measurement

Check the electrical and/or mechanical characteristics specified in the detail specification. Electrical characteristics should be checked while testing. If a failure occurs, check whether it is caused by the SMD itself and deal with appropriate action.

4. INFORMATION TO BE GIVEN IN THE DETAIL SPECIFICATIONS

(1) Pre-treatment [Refer to **3.2**]

(2) Printed circuit board for mounting SMD [Refer to **3.3**]

(3) Soldering condition [Refer to **3.3**]

(4) Items and conditions in initial measurements [Refer to **3.4**]

(5) Test conditions [Refer to **3.6**]

(6) Amount of deflection [Refer to **3.6**]

(7) Monitoring [Refer to **3.6**]

(8) A number of cycle [Refer to **3.6**]

(9) Post-treatment [Refer to **3.6**]

(10) Items and conditions in final measurements [Refer to **3.7**]

(11) Criteria [Refer to **3.8**]

(12) Other required items

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DESCRIPTION REITERATIVE BENDING TEST FOR SURFACE MOUNT DEVICES ON THE BOARD

1. HISTORY OF DELIBERATION

Recently there are many downsized package for cellular phone and mobile devices as technology trends and market trends. A bending stress may occur to a solder joint on the printed circuit when key on the keyboard is pressed. This standard is specified of a bend stress of solder joint on a printed circuit board as a part of standard of a reliability test method.

2. ANSWERS IN RESPONSE TO QUESTIONNAIRES

During discussion, there are many opinions about the test method, the test condition and the criteria.

Answers in response to questionnaires addressed by the CSP/FC PG.

[Test condition of a bending test for the surface mounted devices on the printed circuit board during discussion]

(1) Company standard	: established(3), unestablished(6)
(2) Experiences	: Yes(7), No(2)
(3) Board design	: the same board for temperature cycling(2)
(4) Bending speed	: 1 sec/cycles(240 mm/min)(1), 80 mm/min(2), 50 mm/min (1), 40 mm/min (1)
(5) Amount of deflections	: 2 mm(1), 1 mm(2), 0.5~2.0 mm(1), 1.5 mm/3.0 mm/4.5 mm(1)
(6) The shape of the support	: cylinder(5)
(7) Span	: 90 mm(3), 50 mm(1), 45 mm(1)
(8) A bending direction	: solder side(4), both side(2)
(9) Measurement	: continuous monitoring(3), interval(2)
(10) Numbers of points to press	: two points at component side(3), one point at solder side (1), two points at solder side (2)
(11) Criteria	: 10 % and above(4), 100 % and above(1)

3. MESUREMENT

The methods of measurement are discussed about the measurement at interval of some cycles and the continuously monitoring. In the first mentioned case, actual devices are measured. In another case, daisy chained packages as a test equipment element is measured. Because it is necessary to improve infrastructure for continuous monitoring, it is not general. The members of this PG agreed that the measurement is at interval of some bending cycles. It is recommended electrical characteristics should be checked holing the specified deflection. An amount of deflections with 1.0 mm, 2.0 mm were adopted. But their values are not specified, because an actual stress is unknown in the process of actual fabrication.

4. SUPPLEMENT

The span of support tools is able to be changed with the size of PCB. Even the same specified amount of deflection is applied, the stress on joint in the case of span 50 mm is not the same stress in the case of span 90 mm, because of the radius of curvature of PCB is not the same. Each amount of deflection applied to the same stress of joint is selected in the case of each span. The radius of curvature of PCB can be shown as follows:

$$R = (L^2+4H^2)/8H \qquad (1)$$

Where L (mm) is span of support H (mm) is amount of deflection.

Table 1

Acomparison of an amount of deflection in the case of span 90mm and in the case of span 50 mm

	Span 90 mm	Span 50 mm
Deflection	1 mm	0.3 mm
	2 mm	0.6 mm
	3 mm	0.9 mm
	4 mm	1.2 mm

TEST METHOD 005
Drop test after mounting

1. Scope

This standard is applied to the CSP, BGA and leadless package used for notebook PC and the portable devices such as a cellular phone etc.

This standard provides a board level evaluation method of dropping impact against solder joint by means of duplicating the dropping impact stress in the field use condition.

2. Test Equipment

The equipment and tools used in this test shall conform to section **3.5**.

3. Test Procedure

3.1 Specimen

The specimen should be prepared with production device or daisy-chain package.

3.2 Pre-treatment

Pre-treatment shall be carried out according to the items and conditions specified in the individual specification, if necessary.

3.3 Board assembly procedure

Before going into the test, the specimen specified under section **3.1** shall be mounted on the standard test board specified in “Test Board Design Guide” with the standard assembly conditions specified in “ Soldering heat test for the test board”.

3.4 Initial Measurement

The initial measurement shall be carried out according to the items and conditions specified in the individual specification.

3.5 Test Conditions

The test shall be carried out with the terms and conditions specified in the individual standard.

(1) Drop method:free-fall

(2) Material of floor plate: concrete floor or steel plate

(3) Support tool:

The items below should be followed by the terms and conditions specified in the individual standard.

1. How to fix the specimen on the support tool.
2. The position where a specimen is fixed
3. Weight of support tool

When the specimen collides with floor plate, the possible step should be taken to keep original position of the specimen against the floor surface.

Unless otherwise specified in the detail specifications, the following any methods are recommended for the purpose of keeping the specimen position.

Figure 1 shows an example of **method 1**.

Method 1: The specimen shall be dropped with suspended by thread.

Method 2: The specimen shall be dropped with caught by a tool like arm. It becomes free from fixing tools immediately before collision with floor plate.

Method 3: The specimen shall be dropped with placed on a table. It becomes free from the table immediately before collision with floor plate.

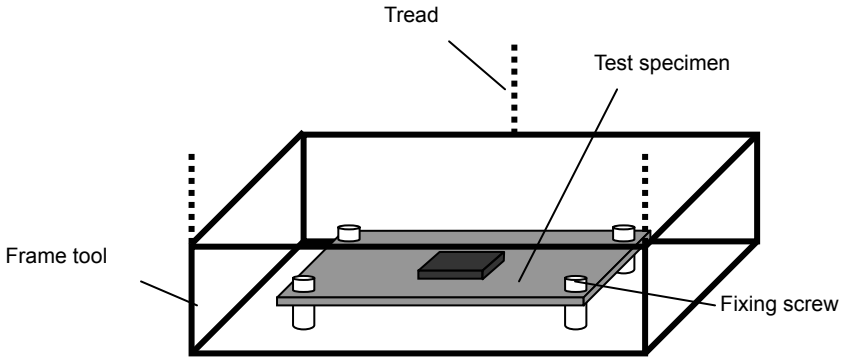


Figure 1 An example of the test board fixture in the method 1.

(4) Drop height: Applicable drop heights are shown in **Table 1**.

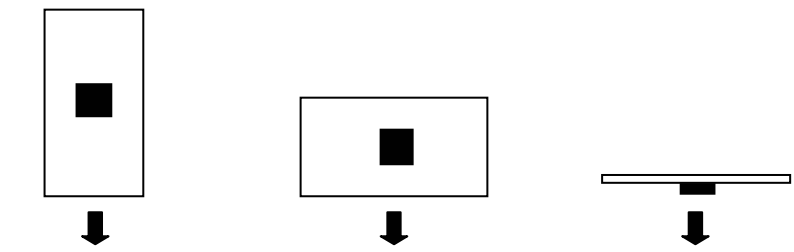
Drop height is defined as the distance between floor surface and the lowest part of the test specimen.

Table 1 Drop height

Drop height (cm)	30 cm	100 cm	150 cm
Example of applications	Mobile devices, Notebook PC	Mobile devices	Mobile devices

(5) Direction

Three directions shall be applied as shown in **Figure 2**.



Vertical drop (Short side collides) | Vertical drop (Long side collides) | Horizontal drop (Device is on down side)

Figure 2 Three directions for drop test

(6) Drop number: 2 times as a standard.

Drop number count: one drop in each of three directions makes one count In case of a repeated drop test is required, applicable conditions are shown in **Table 2.**

Table 2 Drop number

Drop height	Drop number
30 cm	200 times
100, 150 cm	10, 20 times

3.6 Test Method

The test shall be carried out according to the test conditions specified in section **3.5** with the assembled sample following section **3.3** set up on the support tool in the section **3.5 (4).**

3.7 Interim Measurement

Interim measurement shall be carried out according to the terms and conditions specified in the individual specification, it is recommended to measure the sample in between each number of times, as much as possible.

3.8 Final Measurement

The final measurement shall be carried out according to the terms and conditions specified in the individual specification. In this test, the printed circuit board, solderability, and the SMD may cause complex effects. If a failure occurs, check whether it is caused by the SMD itself and take appropriate action.

3.9 Conditions to be specified in the individual specification.

(1) Pre-treatment conditions (if necessary) [Refer to section **3.2**]

(2) Quality specification of test board (when not specified) [Refer to section **3.3**]

(3) Mount conditions (when not specified) [Refer to section **3.3**]

(4) Items and conditions of initial measurement [Refer to section **3.4**]

(5) Test conditions [Refer to section **3.5**]

(6) The number of repetitive drop [Refer to section **3.5**]

(7) Items and conditions of middle measurement [Refer to section **3.7**]

(8) Items and conditions of final measurement [Refer to section **3.8**]

(9) Criterion [Refer to section **3.8**]

(10) Other required items

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COMMENT

1. Background

When accidentally dropping mobile devices to the ground, it's solder joint in between electronic component and motherboard experiences a dropping impact. Therefore this kind of devices, it is very important t to evaluate the dropping impact influences by drop test. From the circumstance above, wedecided to establish the drop test standard. This standard provides a board level evaluation method of dropping impact against solder joint by means of duplicating the dropping impact stress in the field use condition.

2. Current status of related companies

During the discussion, many opinions were given about test methods, conditions, and criteria.

Opinion survey results on the test are outlined below.

In addition, the drop test has mainly performed with the conditions from cellular phone makers and other mobile device makers.

And its results strongly depend on the assembly conditions between the enclosure and the motherboard.

Therefore, just an example of test method is introduced in the standard.

Regarding the drop height, this standard specified as follows with the consideration of field use condition.

Cellular phone: 100 cm/150 cm, Notebook PC: 30 cm

Additionally for dropping direction, 3 directions are defined to simplify the test as much as possible.

[Drop test conditions under discussion]

(1) Existence of enforcement

Enforce: (5) not enforce: (3)

(2) Drop test conditions

① Drop height: 100 cm(1), 150 cm(1), 100 cm and 150 cm(1), 150 cm and 180 cm(1)

② Angle: 3 angles/ X, Y, Z (1), 6 angles/X1, X2, Y1, Y2, Z1, Z2 (2), 6 angles, 12 tours and 4 points (1)

③ Drop method: Natural fall (3)

④ Material of floor plate: Steel on the concrete (1), concrete (2)

⑤ Support tool: Aluminum (1)

⑥ Weight : 100 g(1), 84 g(1), 150 g/100 cm and 80 g/150 cm(1)

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Comments

1. Purpose of this standard

This standard was being established at **IEC**. Mechanical stress test methods for mounted SMDs are already specifies in standards **EIAJ RCX-0102** to **RCX-0105** established by Electronic Industries Association of Japan(**EIAJ**).This standard covers the resistances to items in these standards as the minimum requirement when semiconductor SMDs is mounted.

2. Evolution of establishment

The environmental and endurance test methods for the semiconductor devices have already been specified as **EIAJ ED-4702** and **EIAJ ED-7407**. However, a variety of semiconductor package types and their mount types are proposed according to the changes in technologies and market these days. Also the environmental and endurance test methods for semiconductor devices are becoming an important position at its development stage. Under these circumstances, the standardization of the reliability evaluation methods for the soldering joint on the board and the semiconductor devices being mounted on that board, under actual operating environments after the semiconductor packages have been mounted on the board, is required. Accordingly, the test methods standard for the semiconductor devices themselves (**EIAJ ED-4701**) cannot cover all the items. Taking into consideration such changes of the industry, it is decided to newly establish the environmental and endurance test methods for the semiconductor devices being mounted on the board. The same as before, **EIAJ ED-4701** is used as the environmental and endurance test methods for the semiconductor devices themselves, while this standard is established so that the semiconductor devices are tested and evaluated for the failures which can be assumed to occur only when the semiconductor devices are mounted on the board.

3. About the devices for evaluation and the test method

There are two types of specimen that are used for the evaluation specified in the standard.

(1) Actual devices

(2) Test element group (TEG)

It is ideal to use the actual devices. However, to simply carry out measurement and analysis of electrical characteristic, it is better and common to use the dedicated TEG at an early development and evaluation stage in order to efficiently carry out the test. When the reliability of the CSP/BGA packages being mounted is evaluated at the temperature cycling test specified in Annex 1 (Normative) of the standard, many cases were reported that the soldering joint were broken at high temperature but it was recovered at normal temperatures. In this case, the failure modes occurred not only with the soldering joint but also with bonding part (breaking) of the ICs. It is desirable to consider possible failures for the design of the TEG.

Standardization of the TEG for evaluation was also a subject of discussion. But, it is set aside as the subject to be discussed in the future. However, the TEG is used for partial evaluation only, and it is not appropriate that it is used to find out either the synergy of or the effect on the actual devices or the failures caused by mismatching. Therefore, final evaluation should be carried out using the actual devices.

To evaluate the characteristics of the actual devices, apply the boundary-scan test method, as well as applying the function tester. However, note that the boundary-scan test method is applicable only to the semiconductor devices corresponding to that test method.

4. About mechanical stress measurement method for SMD mounted on board

CSP-BGA packages installed on a circuit board will be subjected to mechanical stress in any event stated below. It is important to evaluate its reliability in these events.

(1) Temporary bending (A circuit board holding the SMD is bent temporarily when a unit in which the circuit board is installed is produced or used.)

(2) Repeated bending (The circuit board is bend repeatedly when keys on the unit are pressed.)

(3) Shock (Package receives shocks when the unit is dropped onto a hard object.)

(4) Vibration

(5) Stress due to self- heat generation by semiconductor devices

In this deliberation, we wxamined the test methods of the stresses mentioned above. However, there are few actual test examples about the stress due to vibration or self-heat generation by semiconductor devices. So the setting of factors and the establishment of optimal evaluation method for them are continuously studied in the future.

Table 1 Mechanical stress applied to SMD mounted on circuit boards

Event	Required quality example	Possible defect development mechanism	Factor example	Evaluation method example
Temporary bending	Bending Displacement of X mm does not break the package	When the board is bent, it generates excessive stress to the joint between the board and package, leading to rupture.	Stress to the joint (strain) Deformation (strain) speed	Board bending limit test
Repeated bending	Hitting keys X times does not break the package.	When the board is bent repeatedly, it generates stress to the joint, leading to fatigue rupture.	Stress to the joint (distortion) Deformation (distortion) speed Number of times that the board is bent	Repeated board bending test
Shock	Dropping the unit from height of X m Y times does not break the package.	When the unit is dropped onto a hard block, the board is bent instantaneously and generates stress to the joint, leading to rupture.	Stress to the joint (distortion) Deformation (distortion) speed Number of times that the board is bent	Board impact test
Permanent bending	Keeping the board bent by X mm for Y hours does not break the packages.	When stress to the board is permanently bent, it generates stress to joint, leading to creep rupture.	Stress to the joint (distortion) Time during the board is kept bending	Creep test
Vibration	Subjecting the board to vibration of Y G at X Hz for Z hours does not break the package.	When the board is instantaneously bent due to vibration, it generates stress to the joint, leading to fatigue rupture.	Stress to the joint (distortion) Deformation (distortion) speed Time	Board vibration test
Stress due to self-heat generation by semiconductor devices	X times of switching on/off semiconductor devices does not break the package	When stress happens to a joint due to self-heat generation by semiconductor devices, it leads to breakage.	Supplied electric power (Temperature) Time of ON/OFF	Temperature cycle test and power cycle test
Stress due to temperature change of external environment	X times of changing temperature of external environment does not break the package	When stress happens to a joint due to temperature change of external environment, it leads to breakage.	Temperature of external environment and a gap of temperatures	Temperature cycle test

5. About strength test of device itself and shock resistance test

As a result of deliberation by the reliability subcommittee, it was decided that the standard itself is deleted because no company has executed the actual tests and necessity of the standard is low.

6. Deliberating member

Deliberating of this standard has been made by “CSP/FC board level reliability PG” of the Technical Standardization Committee on Semiconductor Device/Semiconductor Devices Reliability Group.

The members of deliberation of this standard are below.

<Technical Standardization Committee on Semiconductor Devices>

Chairman	Kazuo Endo	NEC Electronics Corp.

<Group on Semiconductor Devices Reliability>

Chairman	Kazutoshi Miyamoto	Renesas Technology Corp.

<Sub-Committee on Semiconductor Devices Reliability>

Chairman	Tetsuaki Wada	Matsushita Electric Industry Corp.

<CSP/FC Test Method PG>

Leader	Hiroshi Matsushima	Matsushita Electric Industry Corp.
Sub-Leader	Toshiki Yamaguchi	Fujitsu Ltd.
	Koujiro Shibuya	NEC Electronics Corp.
	Makoto Morikawa	NEC Electronics Corp.
Members	Toshiyuki Osada	KAWASAKI MICROELECTRONICS, INC.
	Yasuhiro Watanabe	Sanyo Electric Co., Ltd.
	Masato Murata	New Japan Radio Co., Ltd.
	Tsuneji Shiraishi	Sony Semiconductor Kyushu Corp.
	Toshimitsu Suzuki	Toshiba Corp.
	Kazuhiro Umemoto	IBM Japan, Ltd.
	Masahiro Hirose	Renesas Technology Corp.
	Takahiro Itoh	Rohm Inc.