Standard of Japan Electronics and Information Technology Industries Association

3.3V±0.3V (Normal Range), and 2.7V to 3.6V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuit

1. Interface Standard

1.1 Purpose

To provide this standard of specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1.2 Scope

This standard defines power supply voltage ranges, DC interface parameters for a family of nonterminated digital circuits operating from a power supply of 3.3V and driving/driven by parts of the same family, or mixed families which comply with the input/output interface specifications.

The specifications in this standard represent a minimum set or "base line" set of interfaces for LVTTL-compatible and LVCMOS-compatible circuits.

2. Standard specifications

All voltages listed are referenced to ground except where noted.

2.1 Absolute maximum continuous ratings

Table 1 Absolute maximum continuous ratings Note 1

Parameter	Symbol	Test condition	Rating	Unit
Power supply voltage	V_{DD}		-0.5 ～4.6	V
DC input voltage	V_{IN}	excluding I/O pins	-0.5～V_{DD}+0.5(≦4.6 max)	V
DC output voltage	V_{OUT}	including I/O pins	-0.5～V_{DD}+0.5(≦4.6 max)	V
DC input current	I_{IN}	V_{IN}＜0V or V_{IN}＞V_{DD}	±20	mA
DC output current	I_{OUT}	V_{OUT}＜0V or V_{OUT}＞V_{DD}	±20	mA
Storage temperature range	T_{STG}		Note 2	℃

Note 1: Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum conditions is not implied, if it is beyond recommended operating conditions.

Note 2: Specified by manufacturer for various purposes, respectively.

2.2 Recommended operating conditions

Table 2 Recommended operating conditions

Parameter	Symbol	Normal range (3.3V nominal)	Wide range (3V nominal)	Unit
Power supply voltage	V_{DD}	3.0 ～3.6	2.7～3.6	V
Operating temperature range	Ta	Note 3	Note 3	℃

Note 3: Specified by manufacturer for various purposes, respectively.

2.3 DC specifications

All specifications in the following tables apply across the operating temperature range.

Table 3 LVTTL & LVCMOS input specifications

Wide range (3V nominal):V_{DD} (min) =2.7V, V_{DD} (max) = 3.6V

Normal range (3.3V nominal):V_{DD} (min) =3.0V, V_{DD} (max) = 3.6V

Parameter	Symbol	Test condition Note 4	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geqq V_{OH}$ (min) or $V_{OUT} \leqq V_{OL}$ (max)	2.0	V_{DD}+0.3	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	V_{IN} = 0V or V_{IN} = V_{DD} Note 5		±5	μA

Note 4: For conditions shown as `min` or `max`, use the appropriate value shown in Table 4 and Table 5.

Note 5: Excluding common input/output terminals.

Table 4 LVTTL output specifications

Normal range (3.3V nominal): V_{DD} (min) = 3.0V, V_{DD} (max) = 3.6V

Parameter	Symbol	Test condition	Min	Max	Unit
High-level input voltage	V_{OH}	V_{DD} = min, I_{OH} = -2mA	2.4		V
Low-level input voltage	V_{OL}	V_{DD} = min, I_{OL} = 2mA		0.4	V

Table 5 LVCMOS output specifications

Wide range (3V nominal):V_{DD} (min) = 2.7V, V_{DD} (max) = 3.6V

Normal range (3.3V nominal):V_{DD} (min) = 3.0V, V_{DD} (max) = 3.6V

Parameter	Symbol	Test condition	Min	Max	Unit
High-level input voltage	V_{OH}	V_{DD} = min, I_{OH} = -100 μA	V_{DD}-0.2		V
Low-level input voltage	V_{OL}	V_{DD} = min, I_{OL} = 100 μA		0.2	V

2.4 Optional DC electrical characteristics for Schmitt trigger operation

All specifications in the following tables apply across the operating temperature range.

2.4.1 Optional Schmitt trigger operation – 3.3V Normal range

Table 6 3.3V Normal range Note 6 and 7

Symbol	Parameter	Test Condition	MIN	MAX	Unit
V_{DD}	Supply Voltage	---	3.0	3.6	V
Vt+ (Vp)	Positive Going Threshold Voltage	$V_{OUT} \geqq V_{OH}$ (min)	0.9	2.1	V
Vt− (Vn)	Negative Going Threshold Voltage	$V_{OUT} \leqq V_{OL}$ (max)	0.7	1.9	V
VH (⊿Vt)	Hysteresis Voltage	Vt+ − Vt−	0.2	1.4	V
V_{OH}	Output High Voltage	I_{OH}= −100 μA I_{OH}= −2mA	V_{DD}−0.2 2.4	— —	V
V_{OL}	Output Low Voltage	I_{OL}= 100 μA I_{OL}= 2mA	—	0.2 0.4	V

Note 6: VDD of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.
Note 7: For Vt+ (Vp) and Vt- (Vn), VDD refers to the receiving device. For VOH and VOL, VDD refers to the sending device.

2.4.2 Optional Schmitt trigger operation – 3.3V Wide range

Table 7 3.3V Wide range Note 8and 9

Symbol	Parameter	Test Condition	MIN	MAX	Unit
V_{DD}	Supply Voltage	---	2.7	3.6	V
Vt+ (Vp)	Positive Going Threshold Voltage	$V_{OUT} \geqq V_{OH}$ (min)	0.9	2.1	V
Vt− (Vn)	Negative Going Threshold Voltage	$V_{OUT} \leqq V_{OL}$ (max)	0.7	1.9	V
VH (⊿Vt)	Hysteresis Voltage	Vt+ − Vt−	0.2	1.4	V
V_{OH}	Output High Voltage	I_{OH}= −100 μA	V_{DD}−0.2	—	V
V_{OL}	Output Low Voltage	I_{OL}= 100 μA	—	0.2	V

Note 8: VDD of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.
Note 9: For Vt+ (Vp) and Vt- (Vn), VDD refers to the receiving device. For VOH and VOL, VDD refers to the sending device.

3 Test conditions

3.1 Positive Going Threshold Voltage : Vt+ (Vp)

Input signal is raised from a grand level in the measurement circuit shown in Fig. 1 , and the input voltage value of which output logic changed is determined as Vt+ (Vp).

3.2 Negative Going Threshold Voltage : Vt- (Vn)

Input signal is dropped from a power supply voltage level in the measurement circuit shown in Fig. 1 , and the input voltage value of which output logic changed is determined as Vt- (Vn).

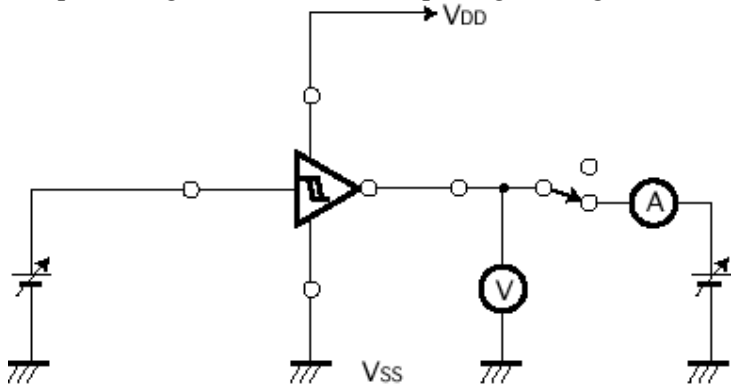

Fig. 1 DC characteristic measurement circuit of Schmitt-trigger input

Explanatory note

1. Purpose of establishment

This standard is enacted to accomplish a high speed and a low voltage operation for digital integrated circuits.

This standard defines power supply voltage ranges, DC interface parameters for a family of nonterminated digital circuits operating from a power supply of 3.3V and driving/driven by parts of the same family, or mixed families which comply with the input/output interface specifications.

2. Review of discussion history

JEDEC JC-16 (Low Voltage & High Speed Interface Sub-committee), called JEDEC after here, which belongs to EIA (Electronic Industries Association of U.S.A), enacted substantially the standard of power supply voltage for digital circuits in the world.

IC Low Voltage Operation Sub-committee which belongs to EIAJ(Electronic Industries Association of Japan) has been cooperation with JEDEC and communicated mutually, since it was founded in 1992.

A power supply voltage of digital circuits had been kept 5V,actually for a long time from 1980's. But, in 1990's, a requirement of low power supply voltage has become increasing to attain a low power consumption and a high noise immunity of electric equipments, in a main application of portable equipments (note PC, etc) which need a long battery operation and high performance equipments (WS, etc) which require a high speed.

In 1990's, also an age of deep sub-micron process technology (below 0.5 μ m process technology) has begun. Needs of low power supply voltage have become the most important issue to obtain a keeping of reliability and continuities of the trends of high density, high speed, together.

According to above back ground, discussion for standard of low power supply voltage, firstly 3.3V,have begun in JEDEC, from early of 1990's. 3.3V standard (JESD8-A) was enacted in June,1994, 2.5V standard (JESD8-5) was in October, 1995 and 1.8V standard (JESD8-7) was in February, 1997, respectively.

Especially, 3.3V JEDEC standard(JESD8-A) was required to maintain 5V TTL and 5V CMOS compatibility, because both 5V and 3.3V power supply voltages were used in a transition period from 5V to 3.3V when it was a first case of lower power supply voltage. To obtain a 5V compatibility, this standard defined a specifications of LVTTL and LVCMOS.

IC Low Voltage Operation Sub-committee began the discussion for standard of low power supply voltage since April, 1996 in EIAJ, according to JEDEC's activities of power supply discussion, in anticipation of a real popularization of 3.3V power supply voltage from the half of 1990's and coming of next lower supply voltage than 3.3V.

EIAJ standard of 3.3V power supply voltage was established in May, 1998. This standard corresponds to that of JEDEC about specifications, because it has been already known and used widely in the world. But, this standard is amended from that of JEDEC about notation and sentence for accomplishing the unify of them among three JEDEC standards (3.3V, 2.5V, 1.8V).

After standardizing the dc standard, discussion on Schmitt trigger input standard was started by JEITA / LVSC in February 2003. JEITA/LVSC submitted its proposed Schmitt trigger input standard to JEDEC in March 2004, for the first time. JEDEC's discussion on Schmitt trigger input standard was begun by this proposal. The task-group was organized by JEITA / LVSC and JEDEC at the JEDEC meeting in June 2004. It has decided that the proposal of Schmitt trigger standard to be added into existing dc standard. Finally, the proposal of Schmitt trigger input standard was approved at the JEDEC meeting in December 2004. Based on the result of JEDEC meeting, JEITA's revised standard of 3.3V power supply voltage was revised as ED-5001A in May 2005.

3. Members of discussion

This standard has been discussed by the IC Low Voltage Operation Sub-committee which belongs to Group on Integrated Circuits of Technical Standardization Committee on Semiconductor Devices.
The members are shown as following.

＜Technical Standardization Committee on Semiconductor Devices＞

Chairman	Hisao Kasuga	NEC Corp.

＜Group on Integrated Circuits＞

Chairman	Hisao Kasuga	NEC Corp.

＜IC Low Voltage Operation Sub-Committee＞

Chairman	Haruyoshi Takaoka	Fujitsu Ltd.
Vice-chairman	Kohji Hosokawa	IBM Japan, Ltd.
Member	Masahiro Kurimoto	Oki Electric Industry Co.,Ltd.
	Hidemitsu Baba	SANYO Electric Co.,Ltd.
	Koji Inoue	Sharp Corp.
	Akira Nakada	Seiko Epson Corp.
	Mitsuo Soneta	Sony Corp.
	Masanori Kinugasa	Toshiba Corp.
	Takashi Akioka	Renesas Corp.
	Takefumi Yoshikawa	Matsushita Electric Industrial Co.,Ltd.
	Akitoshi Watanabe	Rohm Co.,Ltd.
Guest	Kazuo Yamaguchi	TOSHIBA LSI System Support Corp.
	Osamu Uno	Fujitsu VLSI Ltd.