

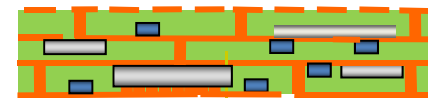
Standardization Group on 3D Assembly technology with device embedding assembly technology

Dumpty chairman: Hisao Kasuga (IS-INOTEK)
17 Members (7 companies + 5 associations)

◆ Scope

Development of international standards
at IEC TC91WG6 and other deliverables
in the area of 3D Assembly technology

with device embedding assembly technology , which covers device
embedded substrates and modules using such substrates, and
other deliverables related to modules



(Example of Device embedded module)

◆ Standard system & Documents

Standard system

IEC62878: Device embedding assembly technology

IEC62878-Part 1: Generic specification

IEC62878-Part 2: Guide line

IEC62878-Part 3: Sectional Requirements (TBD)

Documents of IEC(IS, TS, TR, WIP: Work in Progress)

IEC 62878-1(Part 1)	Generic specification [IS] <New pub.>
IEC 62878-1-1	Generic specification - Test methods [IS] by JP
IEC62878-2(Part 2)	Guide line
IEC/TS 62878-2-1	General description of technology [TS] by JP
IEC/TR 62878-2-2	Electrical testing [TR]
IEC/TS 62878-2-3	Design Guide [TS] by JP

Documents of IEC(IS, TS, TR, WIP: Work in Progress)

IEC/TS 62878-2-4	Test element groups(TEG) [TS] by JP
IEC 62878-2-5	Implementation of a 3D data format for device embedded substrate (<u>FUJIKO format</u>) [IS] <New pub.>* by JP
IEC 62878-2-600 series	Requirements of stacked electronic module - Guideline for stacked electronic module
IEC 62878-2-601	Generic Spec [TBD]
IEC 62878-2-602*	Evaluation method of inter-module electrical connectivity [WIP]* by JP
IEC 62878-2-603*	Evaluation method of intra-module electrical connectivity [WIP]* by JP

Documents of IEC(IS, TS, TR, WIP: Work in Progress)

IEC/TR 62878-2-7	Accelerated stress testing of passive embedded circuit boards [TR]
IEC/TR 62878-2-8*	Warpage Control of Active Device Embedded Substrate [WIP]
IEC/TR 62878-2-9*	Concept of JISSO level in the electronic industries [WIP]* by JP

IEC62878-3(Part 3) Sectional Requirements (TBD)