JEITA

Standard of Japan Electronics and Information Technology Industries Association

EIAJ ED-4704-1

Failure mechanism driven reliability test methods for LSIs (Amendment 1)

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CONTENTS

Standard of Electronic Industries Association of Japan

Failure mechanism driven reliability test methods for LSIs

1. SCOPE

This standard provides failure mechanism driven reliability test methods of LSI by TEG (Test Element Group). B102 provides stressmigaration test method, E101 provides General matter of failure mechanism driven reliability test method.

2. TEST METHODS

Refer to the Appendix I for the test methods.

3. REMARKS

The intesity of stress or the failure criteria of failure mechanism driven reliability test are not defined absolutely. Test results such as lifetime obtained from individual test condition is reduced to the result of standard test condition because the stress and the lifetime are defined by quantitative acceleration model. Also the failure criteria of each elemental device such as MOSFET is dependent on the circuit design. Therefore the stress conditions or the failure criteria are recommended values for typical case.

EXPLANATION

1. PURPOSE OF THIS SPECIFICATION

The method of Failure mechanism driven reliability tests are in-house or are not public standards. Recently, this type of test results have been exchanged as a part of qualification data between the customers and the manufactures. Therefore the standardization of the test methods becomes necessary. The test method of five typical failure mechanisms (Electromigration, Hot Carrier Degradation, Time Dependent Dielectric Breakdown (TDDB), Bias-Temperature Stability (BT), and Soft Errors) was standardized in May, 2000 (**ED-4704**). This time JEITA (former EIAJ) started to establish the test standard of stressmigration and general matter of failure mechanism driven reliability test for LSIs.

2. OPEN ISSUES

The test method and acceleration model of TDDB of ultra thin dielectrics less than 4nm needs further study according to investigation in reliability society. Degradation model of hot carrier for deep sub micron MOSFET also needs further study according to investigation in reliability society. Electromigration of copper interconnect, cosmic ray induced soft error will need standardization in the future.

3. ASSIGNMENT OF TEST METHOD NUMBER

(1)	Front-end process related test	A-100_1xx
(2)	Back-end process related test	B-100_1xx
(3)	Others	C-100_1xx
(4)	General	E-100_1xx

4. MEMBERS OF PROJECT GROUP

This standard has been discussed by Failure Mechanical Wafer Reliability Project Group which belong to Group on Semiconductor Device Reliability of Technical Standardization Committee on Semiconductor Devices.

<Technical Standardization Committee on Semiconductor Devices>

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APPENDIX I

TEST METHOD B-102
STRESSMIGRATION TEST

1. SCOPE

This standard provides for the reliability test method to evaluate stressmigration of metal line and contact for LSI.

2. SAMPLE

TEG (Test Element Group) for stressmigration described below is used. It has two patterns, metal line and VIA chain. They can be selected according to test purpose.

2.1 Sample structure

2.1.1 Pattern of metal line

(1) Structure

Figure 1, **2** show TEG structure. Actual metal line number of metal layer should be identical with the targeted product. **Figure 1**, **2** show the example of four layer metal line TEG. Metal line pitch can be minimum, twice, and five times on the same metal line TEG pattern. Metal line TEG pattern to investigate influence which metal line density give on reliability characteristics can be installed. The probe pad may be installed for leading for detecting failure location. Two metal lines run in parallel in the same layer in **Figure 1**, **2**. They are installed to exclude initial failure mode (particle failure etc.) by measuring leak current between line(a) and line(b).

Figure 1 Metal 1, Metal 3 Layout

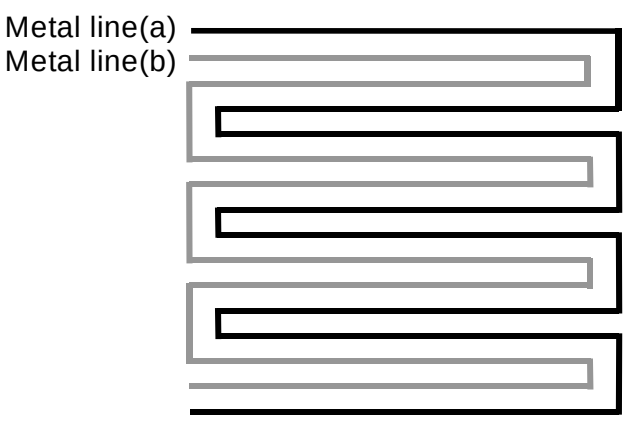
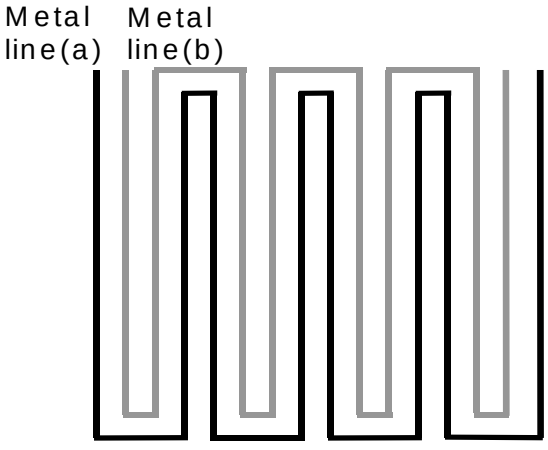


Figure 2 Metal 2, Metal 4 Layout



(2) Metal line width

Minimum metal line width of targeted product and technology, or the line width which gives the shortest life time. Metal line thickness should be the target value of the product.

(3) Metal line length

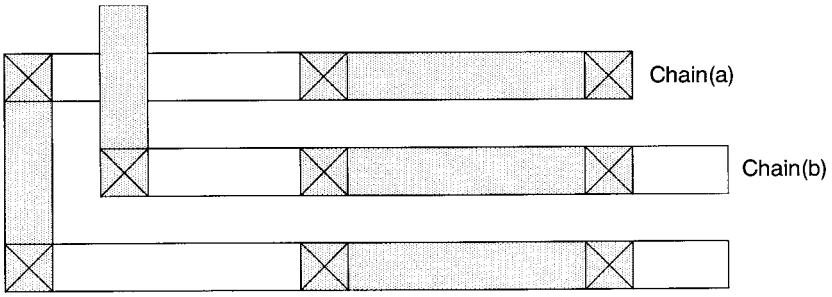
The metal line length is about from 1m to 10m.

2.1.2 VIA chain pattern

(1) Structure

Figure 3 shows TEG. The combination of metal line layer should be equal to targeted product.

Figure 3 Contact Chain Layout



(2) Line width and VIA size

Minimum metal line width of targeted product and technology, or the line width which gives the shortest lifetime. Metal line thickness should be the aim value of targeted product.

VIA size should be less than minimum one of targeted product. Recommended number of VIA is more than 100 k.

3. PROCEDURE

3.1 To determine test temperature and test time

High temperature storage test should be done in wafer level. In case of calculating activation energy Ea, recommended storage temperature is 150°C, 200°C and 250°C. The test may be done under the single temperature condition which gives the shortest lifetime when Ea is known.

3.2 Measurement condition

Recommended test duration is 0h, 168h, 504h, 1008h, 2016h and each measurement should be done at room temperature. The test can be terminated before the last duration time in case you can estimate lifetime when you have enough faults.

(1) Resistance measurement

Apply voltage should be 0.1V～0.2V (recommended), and current monitor should be done.

This apply voltage should not excessive the element to be destructed.

(2) Leak current measurement

Short check between line(a) and line(b), chain(a) and chain(b), metal1 and metal 2, metal 2 and metal 3, metal 3 and metal4 should be done by monitoring current value under supply voltage 0.1V to 0.2V.

3.3 Estimation of activation energy "Ea"

MTTF (Mean Time to Failure) is provided at the storage temperature of T=T1, T2 and T3, respectively. Using equation (1), Ea is calculated from the Arrhenius plot.

$$MTTF = A\exp\left(\frac{Ea}{kT}\right) \qquad \text{---------- (1)}$$

MTTF : Mean Time to Failure

A : Constant

T : Absolute Temperature (K)

Ea : Activation energy (eV)

k : Boltzmann's constant (8.62E-5 eV/K)

In general, activation energy "Ea" is recommended to 0.5eV～0.7eV.

3.4 Judgment

(1) Failure criteria

The failure criteria during stress test are defined by the change ratio of the resistance and by the level of leakage current on test sample. The resistance change ratio is calculated based on the initial resistance. An increase in the resistance change ratio of 10%~30% (recommended value) is used to be failure criteria. Regarding the leakage current, failure criteria are defined as that leakage current becomes larger than 1e-9[A] (recommended value).

(2) Failure analysis

When failures occurred on the tests, the failure analysis is executed to investigate if failures are caused by stress migration or not. For example, the failures that caused by dust or scratch are not counted as stressmigration failure.

3.5 Lifetime estimation

The lifetime is estimated by the log-normal distribution or Weibull distribution. Using Weibull distribution, time "t" that reaches to F(t)=63% and the measure parameter "η" are calculated from equation (2). Also the shape parameter "m" is given as the slope of straight line on Weibull plot.
Failure mode is categorized by m value as listed below.

m<1 --- decreasing failure rate → Early failure
m=1 --- constant failure rate → Random failure
m>1 --- increasing failure rate → Wear-out failure

If data points on Weibull plot do not have the straight line, there is a possibility of different failure modes or complex distributions.

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{m}\right] \qquad \text{---------- (2)}$$

η : Measure parameter
m : Shape parameter

In general, "2" is used as the shape parameter "m", if "m" can not be calculated.
The cumulative failure rate "F(t)" is calculated from following equation.

$$F(t) = i/(n+1) \qquad \text{---------- (3)}$$

i=1,⋯,n

The measure parameter "η" is given by,

$$\eta = t \times \left[-\ln(1 - F(t))\right]^{-1/m} \qquad \text{---------- (4)}$$

Finally, MTTF on the failure rate "f(t)" at operating temperature is calculated from equation (5).

$$MTTF = \eta \times \exp\left\{\frac{Ea}{k}\left(\frac{1}{Top} - \frac{1}{Tst}\right)\right\} \times \left[-\ln(1 - f(t))\right]^{1/m} \qquad \text{---------- (5)}$$

η : Measure parameter
Top : Operating temperature(K)

Tst : Stress temperature (K)
Ea : Activation energy (eV)
k : Boltzmann's constant (8.62E-5 eV/K)
m : Shape parameter

E-101 General failure mechanism driven reliability test methods for LSIs

1. SCOPE

This standard provides the general matter of failure mechanism driven reliability test methods for LSI.

2. PURPOSE OF FAILURE MECHANISM DRIVEN RELIABILITY TEST

Failure mechanism driven reliability tests are performed by followings.

(1) Reliability evaluation for LSI products or technology which failure mechanism is well known.

(2) Reliability monitoring for LSI products or technology which failure mechanism is well known

(3) Reliability evaluation which failure mechanism is difficult to evaluate by the reliability test of LSI products.

(4) Acquisition of baseline data for technology or production line, not for quality assurance of real LSI products.

This test method might not be effective because it is not necessarily clear what kind of failure mechanism is critical for LSI. And with the technology progress, some failure mechanisms will not be major, or some test methods will be newly needed.

3. GENERAL REQUIREMENT

Reliability test methods or samples should meet following requirements.

(1) The result obtained from the acceleration test must be able to convert to lifetime or failure rate under LSI use conditions.

(2) When the TEG is used for the test, structure of that TEG should be reflected the actual structure of LSI.

4. FAILURE CRITERIA

LSI is a combination of a lot of circuits, and each circuit is also combination of a lot of MOSFETs. Therefore, the relationship between the degradation of MOSFET performance and the degradation of performance of LSI is not necessarily correlated as well.

Because the influence on circuit characteristic due to each MOSFET, depends on the circuit system itself. So, it becomes a problem how the failure criteria (eg. MOSFET degradation, wiring resistance increase by EM, etc) should be defined.

Acceptable amount of degradation of the unit element can be estimated by performing circuit simulation only when the most critical circuit in a LSI is known in advance. By this estimation, failure criteria can be defined. When the estimation is not available, certain amount (eg. 10%) shift from initial measurement value/point is used to be defined for the criteria

5. STATISTICAL TREATMENT

(1) Handling of for statistical method

The number of test samples is decided in consideration of the dispersion of lifetime or an amount of degradation. The test results must be analyzed statistically, too. However, it is not necessary to treat statistically, when the cause is known even if it seems to be dispersion.

For example, when the dispersion of the hot carrier lifetime causes by the dispersion of the gate

electrode length, there is a fixed relationship between the gate electrode length and the hot carrier lifetime. Therefore, it is not necessary to use the many samples for statistical treatment, because the hot carrier lifetime is under the control if the gate electrode length is under the control.

On the contrary, in case of the electromigration, the relationship between the variant of interconnect line width and the lifetime is not clear. In such a case, it is necessary to use the number of the samples to determine the mean value and σ.

(2) Probability distribution

Either lognormal distribution or Weibull distribution is used for the probability distribution for the analysis of reliability test results.

There is no great difference between two distributions, when you use them around the mean time to failure, but the difference between the both distributions can be observed when a cumulative failure rate is small. It is uncertain which distribution is correct. Therefore, either distribution is selected from adoptability with the experimental result, experience, etc.

lognormal distribution

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma t} \exp\left[- \frac{}{2\sigma^2} \right] \qquad \text{----------(1a)}$$

$$F(t) = \int_0^t f(u)du \qquad \text{----------(1b)}$$

Weibull distribution

$$F(t) = 1 - \exp\left\{ -\left(\frac{t}{t_{63\%}} \right)^m \right\} \qquad \text{---------- (2)}$$

(3) Definition of reliability

There is the following kind of definition of the statistical reliability.

(a) Mean lifetime

Reliability is defined as the mean lifetime ($t_{50\%}$) at which cumulative failure rate reaches to 50%. When Weibull distribution is used, characteristic lifetime ($t_{63\%}$) is considered for the mean lifetime.

(*) These definitions are limited to specific life time distribution.

Neither $t_{50\%}$ nor $t_{63\%}$ necessarily correspond to the Mean life time for all distributions. $t_{63\%}$ in Weibull distribution, $t_{50\%}$ in lognormal distribution etc. are widely used instead of the Mean life time because they can be easily calculated.

(b) x% lifetime

Reliability is defined as $t_{0.1\%}$, $t_{1\%}$, which is the time at which the cumulative failure rate reaches to 0.1% and 1%, respectively.

(c) Cumulative failure rate

Reliability is defined as the cumulative failure rate after certain operating time.

(d) FIT

Reliability is defined in the FIT, which is failure rate per device hour from eqation(3)

$$FIT = \frac{x}{\text{sample} \times \text{time} \times \text{accelaration factor}} \times 10^9 \quad \text{---------- (3)}$$

X is obtained from χ^2 distribution with failure numbers and confidence level. A part of the $\chi^2/2$ distribution is shown in table 1.

Table 1 x value of the ($\chi^2/2$) using to calculate FIT number

Confidence Level			
60%		90%	
Failure number	x	Failure number	x
0	0.916	0	2.303
1	2.022	1	3.890
2	3.105	2	5.322
3	4.175	3	6.681

6. COMMENT (General matter of failure mechanism driven reliability test methods for LSIs)

6.1 Related standard

International and domestic alike standards, a related standard are shown in the following.

JEITA **EIAJ ED-4701** Environmental and endurance test methods for semiconductor devices
EIAJ EDR-4704 Guideline for accelerated endurance test on semiconductor devices

JEDEC **JESD22** JEDEC standard 22 series, Test Methods
JESD28 Nch MOSFET Hot carrier induced degradation
JESD34 Failure mechanism driven reliability qualification of silicon devices
JESD35 Wafer level testing of thin dielectrics
JESD60 Pch MOSFET Hot Carrier induced degradation
JESD61 Isothermal electromigration test
JESD78 IC latch-up test

MIL **MIL STD 883**

6.2 Acceleration model

The comparison between acceleration factor for **EIAJ ED-4704** and **JEDEC JEP122** is shown in the following.

Failure Mechanism	EIAJ ED-4704		JEDEC JEP122
	Thermal Accelerator Ea(eV)	Other Accelerators	
Gate Dielectric Breakdown	0.5(typical) (0.2~1.0)	AF(v)=exp[B(Estress-Euse)] B=1~7(cm/MV)	0.3eV (40nm) 0.7eV (<40nm) B=3.2 (E model)
Ionic Contamination	not specified	not specified	1.0eV
Electromigration (Al, Al-Si or Al-Cu)	0.5~0.7	AF(j)=(Jstress/Juse)^n n=2	0.6eV, n=2
Charge Loss/Gain	not specified	not specified	0.6eV (DRAM) 1.0eV (EPROM)
Corrosion	1.0	No model	0.70eV (Chlorine) 0.53eV (Phosphorus)
Manufacturing Defects	not specified	not specified	0.5eV (silicon/crystal defects) 1.0eV (Chemical contamination)
Nch Hot Carrier	not specified	(Isubs/Isubu)^(-m)	less than x10 from 0 to 100deg.C
BT Instability(Pch)	not specified	exp(B/E) B=50~100	not specified
Soft Error	not specified	not specified	not specified

APPENDIX II

REFERENCE FOR (Stressmigration)

1. Outline

Recently the standardization of the test method has become necessary , therefore five test method (Bias-Temperature Stability Test, Hot carrier Test , Time Dependent Dielectric Breakdown Test , Electromigration Test , Soft Error Test) has published in recent years. (**EIAJ ED-4704**)

The stressmigration life test method has standardized in this book, and in this chapter we will explain what phenomenon the stressmigration is.

In the stressmigration life test standard, we don't intend to make the unified definition and the judgment of the lifetime which can apply to all makers. The reason is that life time and the judgment standard depend on circuit structure which each semiconductor maker adopts each system and also they depend on the environment which LSI are used.

2. Background

The stressmigration has been known as a failure which cause the disconnection of wiring in the semiconductor products from the failure analysis of the semiconductor device and the effort of the cause investigation.

The electromigration is known as a defective phenomenon which causes the metal line disconnection as well as the stressmigration.

The electromigration phenomena can be explained that drift electron collides with metallic atom in the metal line , and gives the amount of the movement to a metallic atom and it moves in the direction, and finally make a disconnection of metallic wiring.

Therefore, if the current density in the metal line is not high , electromigration doesn't occur.

However, stressmigration occurs in the sample only left at the high temperature atmosphere where sample does not operate.

From these facts it can be understood that stressmigration is a phenomenon caused by a different mechanism from the electromigration.

The stressmigration was reported for the first time in IRPS (International Reliability Physics Symposium) in 1984[1][2]. At that time, even an effective evaluation method was not established.

To find the mechanism of this phenomenon, the way to avoid this failure, and the effective test method, the great effort was paid by the semiconductor device maker. The test method was used to done originally in each company in the past time, but the test method of the stressmigration have unified and been established in this book.

3. Contents

The stressmigration was described in this explanation by the following contents.

Section 4.4: We have explained important term which relate this chapter.

Section 4.5: We have shown another standard of stressmigration which should be compared with our standard.

Section 4.6: We have explained the mechanism of stressmigration for readers to understand the purpose of the life test and acceleration factor of stressmigration.

Section 4.7: We showed the example to avoid stressmigration.

Section 4.8: We explained the degradation model which JEITA adopted.

Section 4.9: We shows the reference document.

4. Explanation of term

(1) Stressmigration

The wiring metal is separated and cut by the stress of the insulation film. The atom of the wiring metal is moved by thermal mechanical stress.

(2) Electromigration

Phenomenon which wiring metal exchanges amount of movement with carrier and begins to move. The atom in metal lines moves when high density electric current is thrown into metal lines for a long time.

(3) Interlayer

Insulation film between over layer metal and lower layer metal.

(4) Passivation

Insulation film deposited over most top layer for protection of LSI chip

(5) VIA

Electric contact in metal lines structure for interlayer connection.

(6) Void

Defect in metal lines or VIA electric contact which generated by stressmigration.

(7) The activation energy

The temperature acceleration constant which depends on the failuremode.

5. Public life test standard

A public Standard of the stressmigrstion is still few. JEDEC have published the standard in December 2000.

EIA/JEP139 GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATION FOR STRESS-INDUCED VOIDING

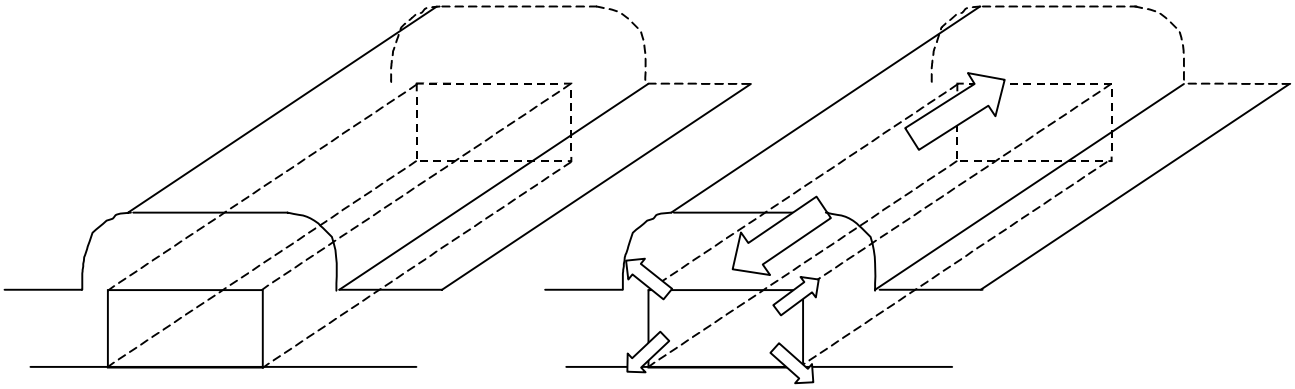
6. Mechanism of stressmigration phenomenon

6.1 Outline

After the wiring metal of LSI is formed, when the insulation film for the interlayer and passivation is formed, the wiring metal receives heat-treating (300-500°C). The wiring metal atom can move comparatively freely at the high temperature and the stress is not generated. However, a metallic atom cannot freely move at the temperature of the real use state condition. The stress is generated in the metal because there is a difference in the linear expansion coefficient of the wiring metal and the insulation film. (**Figure.1**) The void generates by the residual stress and grows up by the stress and the thermal diffusion. In the worst case, metal lines and VIA defect becomes open circuit.This phenomenon is called stressmigration because internal stress causes the defect.

Enough avoidance method against stressmigration should be necessary and clarify an appropriate evaluation method for the quality assurance of LSI.

Figure 1(a) The stress is not generated at high temperature.
(b) An internal stress is generated at low temperature



6.2 Mechanism of stressmigration

It is thought that the generation process of the stressmigration passes the following each process. [3]

(a) Deposition of insulation film

(b) After deposition of the insulation film, temperature decreases ,internal stress generates in the metal.

(c) Metal lines transforms plasticity by the internal stress. The void generates in the metal line. A metallic atom diffuses . The void grows up.

(d) Metal line, VIA is disconnected

We will explain one by one each process of defective generation for the metal line disconnecting and VIA opening.

(a) Deposition of insulation film

(b) After deposition of the insulation film, temperature decreases ,internal stress generates in the metal.

As we have described in the outline. After the wiring metal of LSI is formed, the wiring metal receives thermal-treating (300-500°C), when the insulation film for the interlayer and passivation is formed, The wiring metal atom can be moved comparatively freely at the high temperature. Therefore, the generation of the stress is eased and the internal stress is not generated. However, a metallic atom cannot be freely moved at the temperature of the real use state condition. The linear expansion coefficient of the wiring metal is larger than that of the insulation film. The linear expansion coefficient of each stuff of the semiconductor is shown below. The difference between wiring metal (Al) and SiO2 is about 40 times.

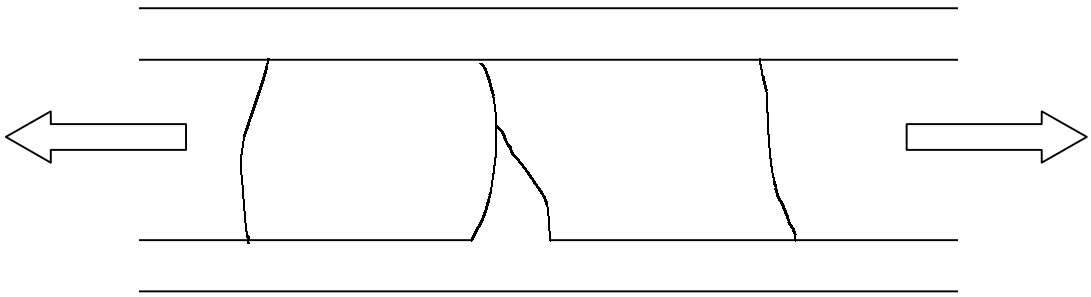
Al :23.1ppm(293K),26.4ppm(500K) Rika nenpyo(Chronological Scientific Tables)
Si :2.6ppm(293K),3.5ppm(500K) Rika nenpyo(Chronological Scientific Tables)
SiO2:0.6ppm [4]

Therefore, the wiring metal is about to shrink more than the insulation film at low temperature, and the tensilel stress is caused in the wiring metal.

(c) Metal lines transform plasticity by the internal stress. The void generates in the metal line. A metallic atom diffuses . The void grows up.

The residual stress generated in this metal arrives at the value of stress which exceeds the elasticity deformation of the wiring metal. (It is called the surrender stress) Therefore, metal lines transform plasticity. When the tensile stress remains after transforming plasticity the wiring metal diffuses in the direction of easing the remaining stress. In the macroscopic, it is generation of the void. Void grows up until the influence of the stress is lost.

Figure 2 wiring metal (Top View)



The wiring metal is disconnected by generating an internal stress.

(d) Metal line, VIA is disconnected

When void grows up until the void crosses the wiring metal. It causes a disconnection for metal lines of LSI.

The role as wiring is not already played and LSI failure has generated.

6.3 Cause of stressmigration

The factor to cause stressmigration is an internal tensile stress from insulation film to wiring metal.

And, the cause of the growth of the void is diffusion of a metallic atom.

That is, there are two factors for the stressmigration . It is a internal stress and diffusion.

The generation of the stress approaches zero in deposition temperature (300-500°C) of the insulation film.

Therefore, the stress is large at the low temperature.

On the other hand, is the diffusion rate of metal atom large or small in the low temperature?

The diffusion coefficient is generally expressed by the formula (1)

$$D=D0 \times \exp\left(\frac{-Ea}{kT}\right) \qquad \text{---------- (1)}$$

D0: Coefficient

Ea: Activation energy [eV]

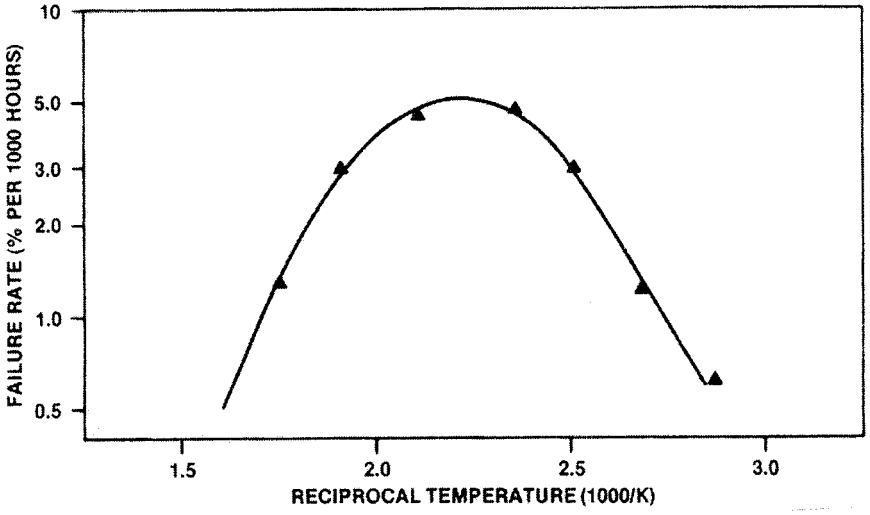
k: Boltzmann’s constant =8.62E-5 [eV/K]

T: Absolute temperature [K]

That is, diffusion becomes active at the high temperature and the Void growth becomes fastly.

The stress and diffusion have an opposite temperature characteristic. Therefore, defective generation will have the peak temperature. (**Figure 3**)

Figure 3 Temperature dependence of Stressmigration Failure



Failure rate versus reciprocal temperature.

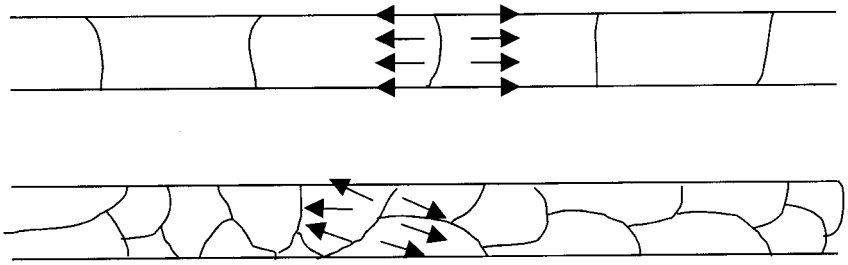
Reprinted from "Reliability Implications of Nitrogen Contamination During Deposition of Sputtered Aluminum silicon Metal Films" John Klema, Ronald Pyle and Edward Domangue IEEE proc. of the IRPS pp1-5 1984 (1984 IEEE)

6.4 Structural factor

Stressmigration comes to be generated easily when the film thickness is thin and the width of wiring is narrow.[5]

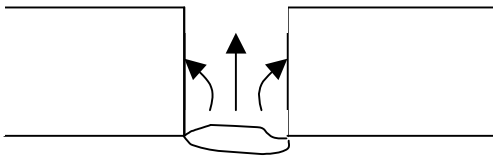
Especially, when the line width is narrower than the grain size (called bamboo structure), Stressmigaration is easier generated. However, it is no good policy reducing the grain size easily. The reason is that there is danger that Electomigration tolerance decreases when triple point increases while grain size becoming small.

Figure 4 Bamboo structure (upper) makes the Stressmigration occur easily.



VIA stressmigration occurred easier when the VIA diameter is small.

Figure 5 When the VIA diameter is small , Stressmigration is easier to occur.



7. How to avoid Stressmigration

To avoid stressmigration by design is difficult. Because the stressmigration is a defective phenomenon generated even if the electric current is not thrown, We can only make the design limitation to the width of the pattern and the VIA diameter. The thermal budget must be reduced as much as possible.

Chose the passivation film which linear expansion coefficient is near the one of wiring metal .

The tensile stress added to the wiring metal can be reduced by using combination of PSG/SiN etc.

Moreover, it is known that the stressmigration tolerance improves by adding Si or the different kind metal (If the wiring metal is Al, it is Cu) with the wiring metal. [6]

In recent year, it is known that the stressmigration tolerance improves by piling up the high melting point metals such as Ti, W, and Ta in the top and bottom of metal lines (It is called the cap metal and the barrier metal). [7]

8. Method of life test

Details of the life test method are mentioned in another chapter. (**APPENDIX I**)

We will explain the method of presuming the life time.

As we mentioned in 6.3.It is known that the peak temperature exists.[1]

Therefore, the formula (2) might be adopted. Formula (2) is good model which can show the existence of the peak temperature.[3]

$$\tau = A \times \left(\frac{1}{\Delta T} \right)^2 \times \exp\left(\frac{Ea}{kT} \right) \qquad \text{---------- (2)}$$

- τ : Life time
- A: Coefficient
- ΔT: Temperature difference life test temperature and deposition temperature of insulation film
- Ea: Activation energy [eV]
- k: Boltzmann’s constant = 8.62E-5 [eV/K]
- T: Life test temperature [K]

By use of formula (2), we can express the existence of the peak temperature.

However, this expression should put ΔT for the deposition temperature of the insulation film.

It is generally difficult to obtain the deposition temperature of the insulation film accurately.

Moreover, there is a difficult point that Ea changes according to the value of ΔT, too.

JEITA adopt the formula (3) for presuming life time.

$$\tau = A \times \exp\left(\frac{Ea}{kT}\right) \quad \text{---------- (3)}$$

τ : Life time

A: Constant

Ea: Activation energy [eV]

k: Boltzmann's constant = 8.62E-5 eV/K

T: Life test temperature [K]

This formula (3) is same with formula (1) which express diffusion phenomena, and the existence of the peak temperature cannot be expressed by this expression. However, there is no obstacle if we uses formula (3) below the peak temperature. Activation energy can be obtained easily with only life test temperature and life time.

9. Reference document

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