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Failure mechanism driven reliability test methods for LSIs

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Failure mechanism driven reliability test methods for LSIs

1. SCOPE

These standards provide failure mechanism driven reliability test methods of LSIs.

2. TEST METHODS

Refer to the Appendix for the test methods.

3. REMARKS

The intensity of stress or the failure criteria of failure mechanism driven reliability test are not defined absolutely. Test results such as life time obtained from individual test condition is reduced to the result of standard test condition because the stress and the lifetime are defined by quantitative acceleration model. Also the failure criteria of each elemental device such as MOSFET is dependent on the circuit design. Therefore, the stress conditions or the failure criteria are recommended values for typical case.

EXPLANATION

1. PURPOSE OF THIS SPECIFICATION

Failure mechanism driven reliability tests such as electromigration or hot carrier are widely employed for in-house reliability test of LSI manufacturers. The test methods are also in-house or are not public standards. Recently, this type of test results have been exchanged as a part of qualification data between the customers and the manufacturers. Therefore, the standardization of the test methods becomes necessary. In United States, JEDEC published several standards of this area. EIAJ started to establish the test standards of electromigration, hot carrier degradation, time dependent dielectric breakdown(TDDB), bias-temperature stability, and soft error.

2. PROCESS OF ESTABLISHMENT

At first, we started to survey in-house test method of LSI manufacturers. It was found that there were slight differences between that of each company. The reason of little difference may be due to long history of investigation of these failure mechanisms. However, there are two types of electric field acceleration model of TDDB because choice of the model is still discussed in reliability society. Although we made effort to unify the test method, we employed two test procedures for one failure mechanism when the unification was very difficult. Of course, we take into account of JEDEC standards. The process of establishment was published as two technical reports titled "Report on failure mechanism of LSI and its test method", part 1, April(1998) and part 2, May(1999) by the technical standardization committee on semiconductor devices, EIAJ. This standard is the essential of two reports.

3. OPEN ISSUES

Acceleration model of TDDB should be unified according to the development of investigation in reliability society. Test method and acceleration model of TDDB of ultra thin dielectrics less than 4nm needs further study. Degradation model of hot carrier for deep sub micron MOSFET will need further discussion. Electromigration of copper film, cosmic ray induced soft error, and stress migration will need standardization in the future.

4. ASSIGNMENT OF TEST METHOD NUMBER

(1) Front-end process related test A-100 – 1xx

(2) Back-end process related test B-100 – 1xx

(3) Others C-100 – 1xx

(4) General E-100 – 1xx

5. MEMBERS OF PROJECT GROUP

This standard has been discussed by Failure Mechanical Wafer Reliability Project Group which belong to Group on Semiconductor Device Reliability of Technical Standaedization Committee on Semiconductor Devices.

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A P P E N D I X

TEST METHOD A-101

Bias-Temperature Stability Test for MOSFET

1. SCOPE

This standard provides the test procedure for bias-temperature stability(BT test) of MOSFETs.

2. TEST EQUIPMENT

2.1 Equipment

(1) High temperature oven

Wafer prober equipped with hot chuck is used for wafer level reliability test(WLR test).

(2) Measurement instruments for DC characteristics of MOSFET.

2.2 Jigs

Wrist strap for ESD protection.

3. TEST SAMPLE

3.1 Sample

MOSFET described as followings is used.

(1) Channel length(Gate length)

Minimum channel length of targeted LSI or technology. Longer channel length may be added if necessary.

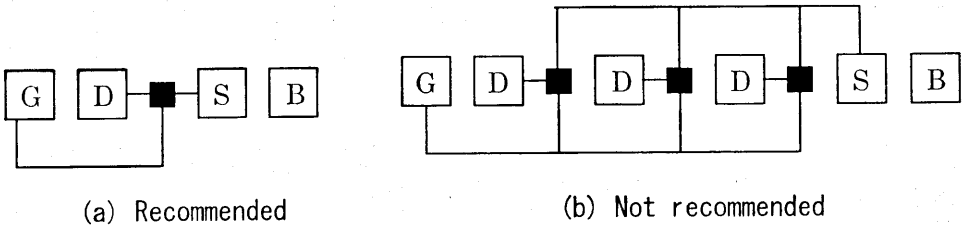
(2) Channel width(gate width)

Any channel width. The channel width from 3um to 20um is recommended unless other channel width is essential.

(3) Structure

It is recommended that four electrodes(gate, source, drain, substrate) are connected to individual external terminals of package.

Figure 1 Connection between MOSFET electrodes and external terminals



(a) Recommended (b) Not recommended

(4) Wafer process

It is strongly recommended that the wafer process such as impurity concentration, thermal treatment, wiring process shall be identical to the targeted LSI or technology.

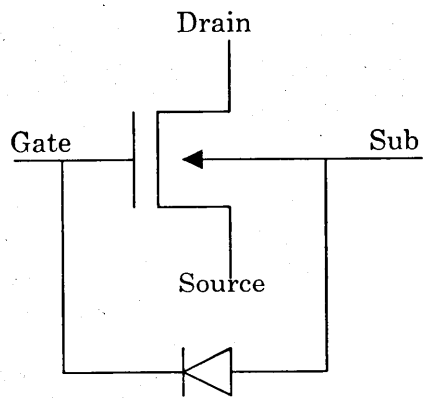
(5) Packaging

Any package type. Packaging is not needed for WLR test.

3. 2 Special attention

Special attention should be taken so that ESD damage is not applied on the samples during packaging process. It is recommended that ESD protection circuit is added to the gate electrode.

Figure 2 Example of ESD protection circuit



4. PROCEDURE

4. 1 Initial measurement and read point measurement

Measurement items are selected from items described below. It is recommended to select one of Vth(ci) or Vth(ext), and select one of Id(sat) or Id(lin). Ambient for electrical measurement is room temperature. In case of WLR, electrical measurement may be done at stress temperature.

(1) Vth(ci): constant current threshold voltage

The constant current threshold voltage is defined as :

$$Vth(ci) = Vgs(@Id = 0.1uA \times W) \qquad -----(1)$$

for linear region(Vds=0.05~0.1V approximately) or typical supply voltage of recommended operating condition. Vth(ci) is the gate voltage at which Id is equal to 0.1uA times gate width(W).

(2) Vth(ext): extrapolated threshold voltage

The extrapolated threshold voltage is defined as:

$$Vth(ext) = Vgs(gm_{(max)}) - \frac{Id(gm_{(max)})}{gm_{(max)}} \qquad -----(2)$$

for linear region(Vds=0.05~0.1V approximately). Vth(ext) is the gate voltage at which the slope of Id-Vgs curve becomes maximum. $Vgs(gm_{(max)})$ is the gate voltage at which gm becomes maximum and $Id(gm_{(max)})$ is the drain current measured when Vgs is equal to $Vgs(gm_{(max)})$. $Gm_{(max)}$ is the maximum DC conductance.

(3) Id(sat): saturated drain current

Id(sat) is the drain current measured when both Vds and Vgs are equal to typical supply voltage of recommended operating condition.

(4) Id(lin): linear drain current

Id(lin) is the drain current measured when Vds is from 0.05V to 0.1V and Vgs is equal to typical supply voltage of recommended operating condition.

(5) Id(leak): drain leakage current

Id(leak) is the drain current measured when Vds is equal to typical supply voltage of recommended operating condition and Vgs is zero. If the subthreshold current is not negligible, Vgs may be equal to substrate(well) voltage.

(6) Gm(max): maximum trans-conductance

Gm is the slope of Id-Vgs curve. Gm(max) is the trans-conductance measured when Vgs is equal to Vth(ext).Vds is linear region or Vds=0.05~0.1V(recommended).

4. 2 Test

Condition of the stress test is described below. Temperature, electric field, read point, and final test time are the values for typical case. It is preferable to do pre-stress test to determine appropriate test condition.

For Nch MOSFET, gate electrode is biased to positive. For Pch MOSFET, gate electrode is biased to negative. It is preferable to test both polarity for Nch and Pch.

For Go/NoGo test, the temperature and the electric field may be one point respectively. If the projected life time is the concern, the temperature and the electric field may be more than two points respectively to obtain activation energy and electric field acceleration factor.

(1) Stress temperature: 150~250 ℃ (recommended)

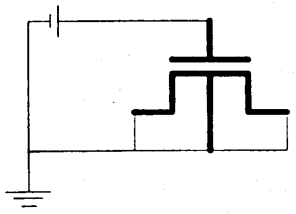
(2) Electric field strength: 4~8 MV/cm (recommended)

For Nch MOSFET, gate electrode is biased to positive.

For Pch MOSFET, gate electrode is biased to negative.

Source, Drain, and substrate(well) are connected to common.
The bias is aplied between gate and common.

Figure 3 MOSFET BT test circuit (Nch)



(3) **Read point**: 0(initial), 0.5h, 1h, 2h, 4h, 10h, ... (continued as same manner)

(4) **Final test time**:

Purpose	Final test time
Go/NoGo test:	1 ~ 10h (recommended)
Lifetime estimation:	10 ~ 1000h (recommended)

4.3 Judgement

Calculate the Vth shift from its initial value or relative change of other parameters(except for Id(leak)). For Go/NoGo test, the Vth shift or other parameter change is compared with pre-defined criteria. If the shift or the change exceeds the criteria, the judgement is made as fail. Example of the pre-defined criteria is delta-Vth=0.1V or delta-Id(sat)/initial Id(sat)=-10%. To obtain the projected lifetime, lifetime is calculated with activation energy and electric field acceleration factor. Though the allowable degradation which defines the lifetime is dependent on the circuit design or the field use condition, typical allowable degradation is delta-Vth=0.1V or delta-Id(sat)/initial Id(sat)=-10%. Relation between lifetime, temperature, and electric field is give by equation(3) or equation(4). Electric field acceleration model is different between equation(3) and equation(4). Because it has been still unkown which one is correct, it is recommended to confirm the acceleration model by additional electric field dependency experiment.

$$\tau = A \exp\left(\frac{Ea}{kT}\right) \exp\left(\frac{B}{E}\right) \qquad \text{-----(3)}$$

Ea: activation energy (eV) (typically, 1eV)
K : Boltzmann constant (8.62e-5[eV/K])
T : temperature (K)
B : electric accelaration factor (MV/cm) (typically, 50~100)
E : electric field (MV/cm)
A : constant

$$\tau = C \exp\left(\frac{Ea}{kT}\right) \exp(D \times E) \qquad \text{-----(4)}$$

D : electric accelaration factor (cm/MV)
C : constant

COMMENTS Bias-Temperature Stability Test for MOSFET

1. Wafer level reliability test(WLR test)

If the final test time is less than 10000seconds, WLR test may be applicable. WLR test is usually employed for Go/NoGo test.

2. Final test time

Final test time is dependent on the combination of stress temperature and electric field. To obtain the acceleration factor, variety of stress condition is employed. Therefore the final test time for moderate stress may be too long to complete within reasonable period. In that case, the stress test can be terminated before the degradation reaches failure criteria and the life time is estimated by extrapolation.

3. Field MOSFET

Field MOSFET can be tested in similar manner with following considerations.

(1) Channel length(gate length)

Channel length is the minimum of isolation length of targeted LSI or technology. Longer channel length may be added if necessary.

(2) Electrical characteristics

Most of electrical characteristics may not be measurable except for Vth(ci) or Id(leak) at typical supply voltage.

(3) Stress electric field

Typically, stress electric field is smaller than that of nominal MOSFET test because thickness of field oxide is thicker than gate oxide. It is recommended the gate voltage of field MOSFET is from typical supply voltage to twice of it.

4. Technical information

Further technical information and background are given in "Report on failure mechanism of LSI and its test method, Part 2", May(1999), Technical Standardization Committee on Semiconductor Devices, EIAJ.

TEST METHOD A-102
Hot Carrier Test for MOSFET

1. SCOPE

This standard provides the test procedure for the drain avalanche hot-carrier-induced degradation of MOSFETs.

2. TEST EQUIPMENTS

2.1 DC power supply

The measurement system must be capable of the simultaneous application of voltage and current at the all terminals (Gate, Drain, and Source, Substrate). It is recommended to employ automatic test system because the test is repetition of measure and stress and the stress time varying exponential manner. Automatic test system consists of PC controled DC measurement instruments. The wafer prober is required for the wafer level hot carrier test.

2.2 Jigs

A wrist strap to avoid electrical static damage

3. TEST SAMPLES

3.1 Test Structures

(1) **Channel Length**

Minimum channel length of targeted LSI or technology. Longer channel length may be added if necessary. The channel length is defined by designed gate length. The effective channel length may be used if necessary.

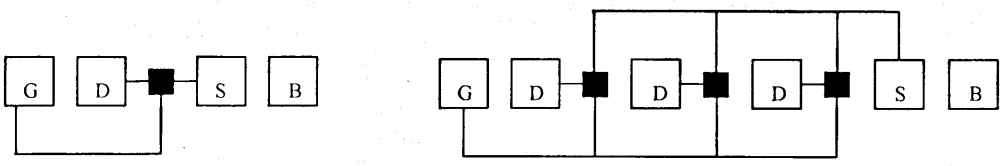
(2) **Channel Width**

A minimum channel width of 3 – 20 um is recommended to avoid narrow channel effects, joule heating, or increasing off current for wider channel MOSFET.

(3) **Structures**

It is recommended that four electrodes(gate, source, drain, substrate) are connected to individual external terminals of package.

Figure 1 Connection between MOSFET electrodes and external terminals



(a) Recommended (b) Not recommended

(4) Wafer process

The manufacturing process should be same as that of the technology of hot carrier test sample, but other processed devices may be used for different purpose.

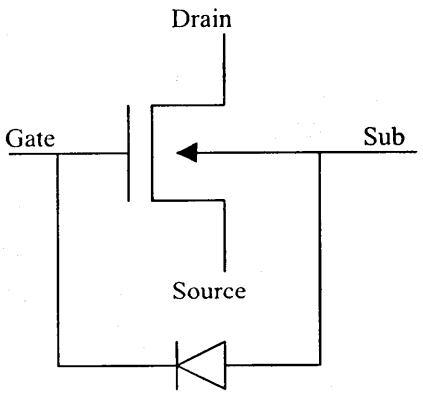
(5) Packaging

The long time hot carrier test with packaged sample is recommended to estimate the lifetime correctly.

3.2 Attention

In case of packaging, the structure is required with the protection diode to avoid electrodes static damage. (See Figure-2)

Figure 2 Example of ESD protection circuit



4. PROCEDURES

4.1 Measurements

(1) Polarity of Drain/Source

The polarity of drain and source during measurement is same as that of during stress test (This means forward bias). Generally, the degradation at the reverse bias is larger than that of forward bias, so it is recommended the reverse measurements is added.

(2) Drain Voltage

0.05V or 0.1V are recommended for linear region. Vdd should be used for Vds of the saturation region. Basically the degradation of linear region is lager than that of saturation region, so the hot carrier test is required the measure both linear and saturation region.

(3) Source Voltage / Substrate Voltage

Source voltage is 0V. Substrate voltage is same as back bias of device or well bias.

(4) Gate Voltage

Gate voltage should be biased from 0V to Vdd.

(5) Temperature

Room temperature (20-30 deg C) is required.

(6) Attention

The excess voltage during the measurement of leak current or breakdown voltage may change the characteristics of MOSFET. Therefore, the measurement of breakdown voltage shall be avoided. If the high voltage is applied for some reason prior to the hot carrier test, the effect to the sample should be confirmed.

The measurement should be started as soon as possible after the stress test ends.

(7) Measurement Parameters

Basically five parameters described below are recommended to measure MOSFET. The degradation of each parameter depends on the MOSFET type or the manufacturing process, etc. So the measurement parameters should be chosen according to the purpose of hot carrier test. The failure criteria also can be decided according to the purpose.

(a) Vth (ci) / Vth (ext)

The constant current threshold voltage Vth (ci) is defined as

$$Vth(ci) = Vgs(@Id = 0.1uA \times W) \qquad \text{--- (1)}$$

Vth (ci) is the gate voltage applied to device at which the drain current is equal to 0.1 uA per gate width (W) in the linear and saturation region.

The extrapolated threshold voltage is defined as

$$Vth(ext) = Vgs(gm_{(max)}) - \frac{Id(gm_{(max)})}{gm_{(max)}} \qquad \text{--- (2)}$$

Vth (ext) is the gate voltage extrapolated at Id=0 based on a measurement slope (Gm (max)) of Id-Vgs curve in the linear region.

(b) Id (sat)

The drain current Id (sat) is measured when the transistor is biased at Vds=Vgs=Vdd in the saturation region.

(c) Id (lin)

The drain current Id (lin) is measured when the transistor is biased at Vds=0.1V or 0.05V in the linear region.

(d) Id (leak)

The drain current Id (leak) is measured when the transistor is biased at Vds=Vdd, Vgs=0V in the saturation region. When the sub-threshold current is measured, Vds is equal to Vbb.

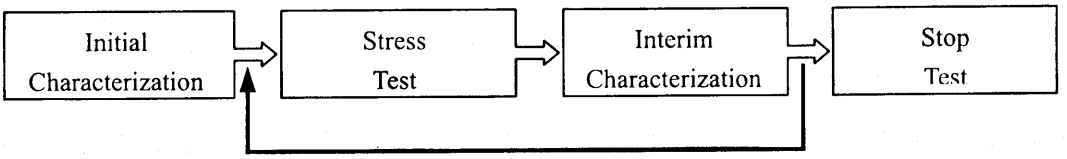
(e) Gm (max)

The maximum linear transconductance is the maximum slope of the Id-Vgs curve in the linear region.

4.2 Stress test

(1) Procedures

Figure3



After getting the initial data, the stress test and the characterization are repeated. (See Figure3) If the parameter degradation exceeds the termination criterion (recommended criterion are 10% for Id, 0.1V for Vt), the test ends. When the time after the stress to the interim characterization is long, the degradation is recovered. So the use of auto measurement system is recommended.

(2) Stress Time

In case of wafer level test, the total stress time is recommended 1E4-1E5 sec and in case of package level test, the total stress needs much longer time. The recommended stress intervals are logrithromic.

Recommended stress time: 1, 2, 5, 10, 20, 50, 100, ...

(3) Stress Conditions

(a) Drain Voltage

To determine the stress conditions, Id-Vds curves for the device must be investigated. Vds stress is recommended to limit maximum drain voltage to less than 90% of transistor breakdown voltage. Note that the short channel MOSFET is difficult to read breakdown voltage. Also the samples measured never be used to hot carrier test because the units is already damaged

(b) Gate Voltage

Gate voltage should be set to induce the maximum substrate current for n-channel MOSFET and the maximum gate current for p-channel MOSFET. The recommended Vgs is Vds/2 for n-channel MOSFET and Vds/5 for p-chnnel MOSFET. The maximum substrate current or gate current measurements induce hot carrier degradation, so the samples should not be used to the hot carrier test.

(c) Source Voltage / Substrate voltage

The source and the substrate voltage are the same as that of the bias conditions of measurement.

5. DATA ANALYSIS

5.1 Parameter degradation

(1) Vth degradation

Relative shift for Vth(ci) and Vth(ext) are calculated from

$$\Delta Vth(t) = Vth(t) - Vth(0) \quad \text{----- (3)}$$

Vth(0) is the initial parameter value. Vth(t) is the parameter value at time t.

(2) Id, Gm degradation

Percent change for Gm (max) and Id is calculated from

$$\Delta Id(t) = \frac{Id(t) - Id(0)}{Id(0)} \quad \text{----- (4)}$$

$$\Delta Gm(t) = \frac{Gm(t) - Gm(0)}{Gm(0)} \quad \text{----- (5)}$$

Id(0), Gm(0) is the initial parameter value. Id(t), Gm(t) is the parameter value at time t.

(3) Data analysis

The parameter change versus the stress time is a straight line on a log-log plot. The slope of the log-log degradation curve saturates with increasing stress time. If the shift criterion is exceeded during a stress, the hot carrier lifetime (τ) should be determined by the time reached to the criterion. If the shift criterion is not exceeded during a stress, the lifetime (τ) should be determined by a linear extrapolation.

5.2 Estimation of DC lifetime

(1) exp(1/Vds) model for n-channel, p-channel MOS

Hot carrier lifetime (τ) is calculated from

$$\tau = A \times \exp\left(\frac{B}{Vds}\right) \quad \text{--- (6)}$$

A is a constant value. B is a constant value.

The hot carrier lifetime (τ) versus the stress voltage (1/Vds) is a straight line on a semi-log plot. The hot carrier lifetime can be calculated with various Vds. 120 is recommended as the default value. If possible, B should be calculated with the experiment data more than 3 points.

(2) Substrate current (Isub) model for n-channel MOSFET

Hot carrier lifetime (τ) is calculated from

$$\tau = C \times I_b^{-m} \quad \text{--- (7)}$$

C is a constant value; m is a constant value.

The hot carrier lifetime (τ) versus the substrate current (Isub) during stress is a straight line on a log-log plot. The hot carrier lifetime (τ) can be calculated with the substrate current (Isub) measured from various Vds. Three(3) is recommended as the default value of m. If possible, m should be calculated with the experimental data obtained from test conditions more than 3 points.

Submicron n-channel MOSFET less than 0.5 um is recommended to calculate from

$$\tau \times I_d = C \times \left(\frac{I_b}{I_d} \right)^{-m} \quad \text{--- (8)}$$

C is a constant value; m is a constant value.

(3) Gate current (Ig) model for p-channel MOSFET

Hot carrier lifetime(τ) is calculated from

$$\tau = C \times I_g^{-m} \quad \text{--- (9)}$$

C is a constant value; m is a constant value.

The hot carrier lifetime (τ) versus the gate current (Ig) during stress is a straight line on a log-log plot. The hot carrier lifetime (τ) can be calculated with the gate current (Ig) measured from various Vds. m should be calculated with the experiment data more than 3 points. A constant value m for pMOSFET is difficult to set the default value because of no information from other technical reports.

5. 3 Estimation of AC lifetime

The degradation of hot carrier occurs arround the bias of maximum substrate current or maximum gate current. Actually the bias condition such as DC acceleration bias is instantaneously generated in the transient period of CMOS circuit. So the AC lifetime should be converted from the DC lifetime. Generally the duty factor method t(AC)/t(DC) is used to calculate the AC lifetime. This method tend to overestimate hot carrier degradation, but the calculation is very easy and also the accuracy is enough to estimate the lifetime. The duty ratio is calculated from one cycle time (t-cycle), rise time (tr) and fall time (tf). Then the AC lifetime τ (AC) is defined as

$$\tau(AC) = \tau(DC) \times \frac{t_{cycle}}{t_r + t_f} \quad \text{----- (10)}$$

BERT or Waveform division method is also used to estimate the AC lifetime. Anomalous degradation caused by "AC effect" is not taken into account on above mentioned method. Therefore, real AC/DC factor should be used to estimate AC lifetime more correctly. The real AC/DC factor is obtained from the AC stress test of MOSFET. The AC stress can be generated with the pulse generator. If possible, the ring oscillator designed in the test chip is recommended to avoid parasitic effect of AC stress equipment.

COMMENTS Hot Carrier Test for MOSFET

1. Technical information

Further technical information and background are given in "Report on failure mechanism of LSI and its test method, Part 2", May(1999), Technical Standardization Committee on Semiconductor Devices, EIAJ.

Test Method A-103
Time Dependent Dielectric Breakdown Test

1. SCOPE

This standard provides for the test method to evaluate time dependent dielectric breakdown (TDDB) for gate dielectric films of semiconductor devices.

2. TEST EQUIPMENTS

TDDB test can be applied for both package level test and wafer level tests. High temperature oven is used for the package level test. In case of the wafer level tests, wafer prober is necessary. Additionally, the measurement instrument that can measure very low level current is necessary for measuring gate current.

3. TEST SAMPLES

Test samples for TDDB test should have the following test structure and area.

(1) **test structure** : capacitor structure

(2) **area** : >0.001mm2

Test sample has a capacitor structure which consists of the gate dielectric film and gate electrode formed on silicon substrate. The area, shape (square, rectangle, comb and so on) and with/ without the source/drain of capacitor structure are selected for the purpose of the test.

4. PROCEDURES

Test method uses the constant voltage stress method to estimate TDDB lifetime and failure rate. Fig.1 shows a procedure of the constant voltage stress method.

4. 1 Initial Measurements

Initial measurements are performed for identifying initial failed samples. The gate current is measured at the applied operating voltage. If the measured current is larger than the defined criterion, then , that sample is rejected as a initial failed sample.

4. 2 Test Conditions

The following test condition is recommended for TDDB test.

(1) **Electric field** : 6 to 14MV/cm

(2) **Temperature** : Room temperature to 250℃

It is preferable to select more than 3 electric fields or 3 temperatures for estimating the field acceleration factor or temperature acceleration factor (activation energy).

4.3 Judgement

Select either of the following failure criteria

(a) When gate current becomes larger than the defined constant value.

(b) When gate current from initial current or measured current of former lap becomes larger than the defined constant value.

The measurement condition (temperature, electric field) for the pass judgment should be set up at operating conditions or stress conditions. The gate current or the gate current shift for failure should be established in consideration of the initial current , the measurement resolution and the products specifications.

4.4 Lifetime estimation

4.4.1 Acceleration model

Eox model and 1/Eox model are widely used models. Both models usually contain temperature acceleration model(Arrhenius model). To contrast the two models, Eox model gives more safety estimation result of lifetime than 1/Eox model gives.

(1) Eox model

$$TTF = A \times \exp\left(\frac{E_a}{kT}\right)\exp(-\beta E_{ox}) \qquad \text{----- (1)}$$

or

$$TTF = A \times \exp\left(\frac{E_a}{kT}\right) \times 10^{-\beta E_{ox}} \qquad \text{----- (2)}$$

TTF: Time to failure

A: Constant

Eox: Oxide electric field

k: Boltzmann constant

β : Electric field acceleration factor

β =1 to 7 (equation(1)) , around 0.43 to 3 (equation(2))

Ea: Activation energy

Ea=0.5eV(Typical) 0.2eV to 1.0eV

(2) 1/Eox model

$$TTF = A \times \exp\left(\frac{E_a}{kT}\right)\exp\left(\frac{\gamma}{E_{ox}}\right) \qquad \text{----- (3)}$$

TTF: Time to failure

A: Constant

Eox: Oxide electric field

k: Boltzmann constant

γ : Electric field acceleration factor γ =200 to 800

Ea: Activation energy Ea=0.5eV(Typical) , 0.2eV to 1.0 eV

4. 4. 2 A procedure of lifetime estimation

(a) Make plot of each stress data using Weibull distribution or Lognormal distribution. Label left axis cumulative failure rate and bottom axis breakdown time(see Fig.2).

(b) Calculate the each failure time t(F%). Next ,make plot of each failure time versus electric field values (Eox model)or reciprocal number of electric field(1/Eox model). Calculate electric field acceleration factor from the slope.(see Fig.3)

then ,make plot of each failure versus reciprocal number of temperature (1/T). Calculate temperature acceleration factor from the slope (activation energy) .(see Fig.4).

(c) Using above acceleration factors, estimate lifetime t(F%) in the use condition (a certain temperature and voltage)

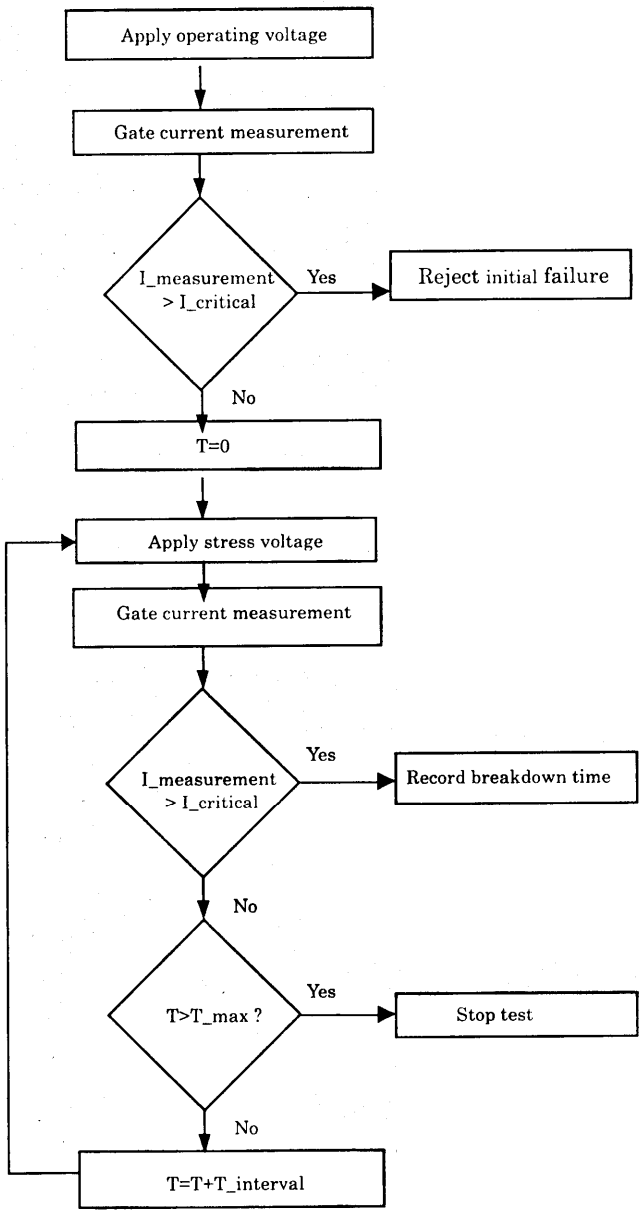


Fig.1 Test flow diagram of constant voltage stress method

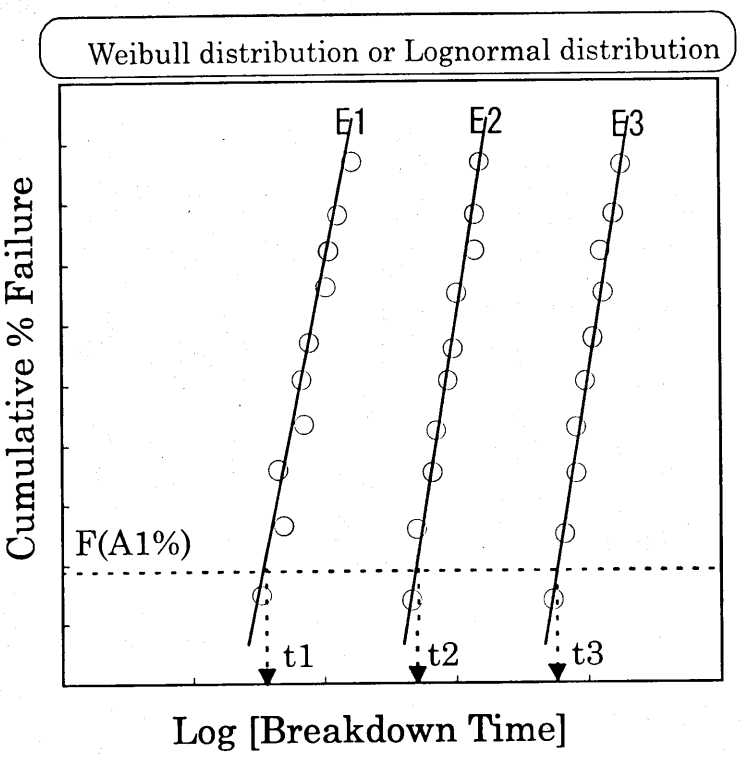


Fig.2 Graph fitted Weibull/Lognormal distribution

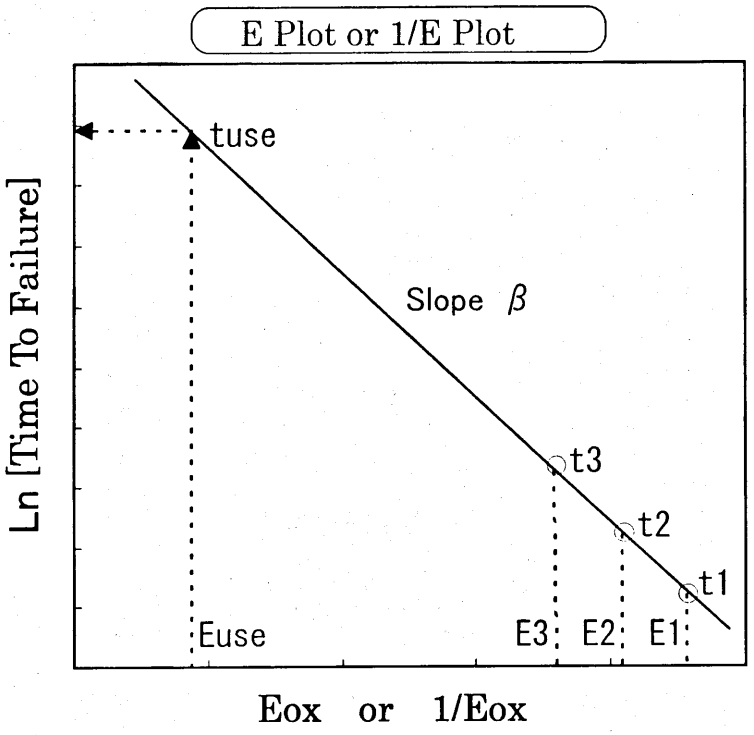


Fig.3 Estimate procedure of electric acceleration factor

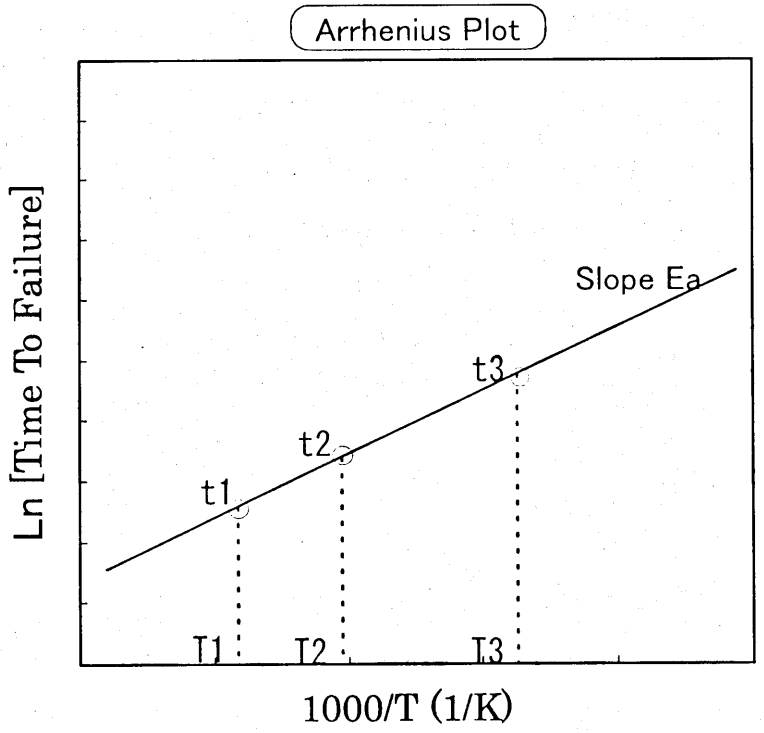


Fig.4 Estimation procedure of activation energy

COMMENTS Time Dependent Dielectric Breakdown Test Method for Semiconductor Devices

1. Lifetime dependence on gate oxide area .

Revised lifetime is often used to carry out lifetime estimation of actual products with various gate area.

To convert the test sample lifetime with a certain gate area into a actual product lifetime with different one, Poisson distribution is used broadly.

$$F = 1 - \exp(-D \times A) \qquad \text{----- (4)}$$

F: Cumulative Failure rate

D: Defect density

A: Gate oxide area

Next formula shows more simple and easy procedure which convert the lifetime fitting with Weibull distribution.

$$TTF_2 = TTF_1 \times \left(\frac{A_1}{A_2}\right)^{1/m} \qquad \text{----- (5)}$$

TTF_1 , A_1 : Time to Failure of the test sample, it's gate area

TTF_2 , A_2 : Time to Failure of the actual product ,it's gate area

m : Shape parameter of Weibull distribution

2. Techinical Background

Further technical information and background are given in "Report on fuilure mechanism of LSI and its test method, Part 1", Apr.(1998), Technical Standardization Committee on Semiconductor Devices, EIAJ.

TEST METHOD B-101
Electromigration Test

1. SCOPE

This standard provides for the method to evaluate the endurance and resistance of metal line against electromigration.

2. SAMPLE

2.1 Samples

The sample is TEG (Test Element Group) described below. Because lifetime of VIA TEG is shorter than that of stripe TEG, the test for stripe TEG can be omitted.

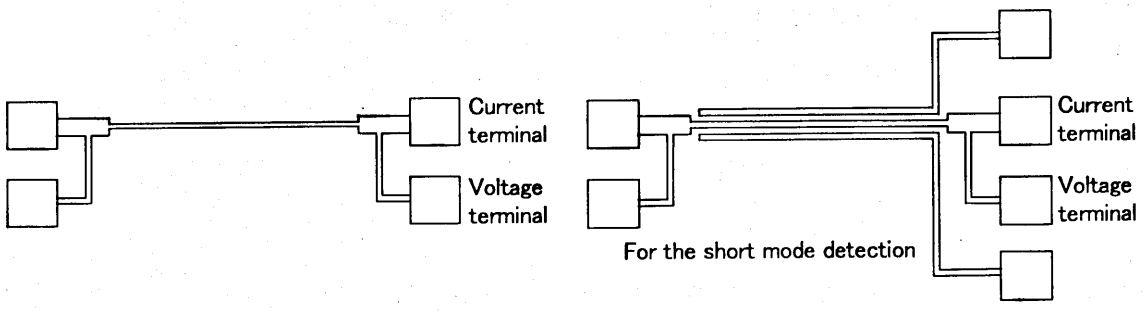
2.1.1 Stripe TEG

(1) Structure

There are two types of structure. One is the TEG of two terminals by which voltage terminal was combined with current terminal. Another one is the TEG of four terminals which contains the voltage terminal as **Figure 2.1.** The four terminals structure is preferable because of high accuracy of resistance measurement.

Metal line for the short mode detection may be installed in parallel with metal line under electromigration test, if necessary.

Figure 2.1. TEG of electromigration evaluation for metal line



(a) TEG of four terminals

(b) TEG with short mode detection line

(2) Metal line width

Minimum line width of targeted product and technology, or the line width which gives the shortest life time. The sample of another line width may be added if necessary.

(3) Metal line length

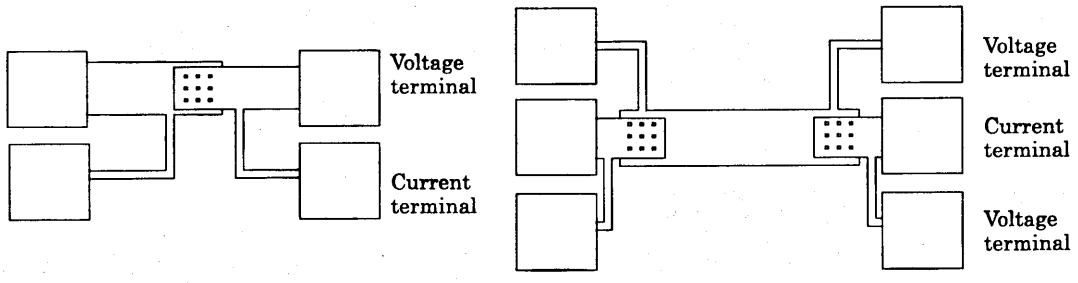
The metal line length is from 800 μ m to 1500 μ m. (recommended)

2.1.2 TEG for VIA evaluation

(1) Structure

TEG of the four terminal structure like **Figure 2.2.** is used as well as stripe TEG. There are two types of structures. One is the single direction TEG. Another one is the both direction TEG. Appropriate one or both ones is selected according to the application. The number of VIA is decided according to the line width so that carrying current of VIA will be proper acceleration test condition. Generally, number of VIA is from 1 to 10.

Figure 2.2. TEG of electromigration evaluation for VIA



(a) Single direction TEG (b) Both direction TEG

(2) VIA size

Minimum size VIA of targeted product and technology.

(3) VIA-VIA space

The VIA-VIA space is 200um or more. When VIA-VIA space longer than 200um is needed, the length is limited so that the metal line resistance does not disturb the detection of the resistance change caused by electromigration. when VIA-VIA space is shorter than 200um, it is necessary to confirm the relation between the lifetime and VIA space because the lifetime tends to become longer as VIA space becomes shorter by the back-flow effect.

3. PROCEDURE

3. 1 TCR (Temperature Coefficient of Resistance) measurement

Relation between temperature and resistance of test structure is given in equation(1). Ct in equation(1) is TCR. The resistance shall be measured in the current that joule heating can be negligible. The average stress temperature during electromigration test can be calculated by this temperature coefficient.

$$R=Ri\{1+Ct(T-Ti)\} \quad \text{----- (1)}$$

R : Resistance of sample at stress temperature (Ω)
Ri : Resistance of sample at reference temperature) (Ω)
T : Temperature of sample during electromigration test (℃)
Ti : Reference temperature(room temperature, typically (℃)
Ct : Temperature coefficient of resistance

3. 2 Decision of stress current density (J) and line temperature (T)

Large current density "J" is desirable to obtain higher acceleration. However allowable current density is limited as enough small value which causes melting of metal line due to Joule heating. Typical, current density is from 5E+5 to 3E+6A/cm^2 (recommendation). The ambient temperature "Ta" should be the range that the package material is not degraded. Typically, ambient temperature is from 150 to 250 ℃ (recommendation). Line temperature "T" is calculated from equation(1).

3. 3 Calculation of activation energy "Ea" and current density coefficient "n"

Lifetime under actual operating condition is calculated based on Black model of equation (2). The original expression of Black model contains W (line width) and t (line thickness) in the equation, but recently these parameters are included into constant "A".

$$MTTF = A \times J^{-n} \exp\left(\frac{E_a}{kT}\right) \qquad \text{----- (2)}$$

MTTF : Mean Time to Failure
A : Constant
J : Current density (A/cm^2)
T : Temperature (K)
Ea : Activation energy (eV)
n : Current density coefficient
k : Boltzmann constant (8.62E-5 eV/K)

Activation energy "Ea" and current density acceleration factor "n" are estimated by electromigration test.

First of all, on defined current density "J", MTTF of t1, t2 and t3 for test temperature of T1, T2 and T3 are extracted from log-normal plot. Then relation between t1, t2, t3 and 1/T1, 1/T2, 1/T3 is plotted on semi-log paper and straight relationship is obtained. The slop of the relationship is the Ea.

Next step, on defined temperature, MTTF of t11, t22, t33 for test current density J1, J2 and J3 are extracted from log-normal plot. Then relation between t11, t22, t33 and J1, J2, J3 is plotted on log-log paper and straight relationship is obtained. The slop of the relationship is the n.

In general, activation energy is from 0.5 to 0.7eV. Current density acceleration factor of stripe TEG is around 2 and the factor for via TEG is from 1 to 2.

3. 4 Judgement

The failure criteria of stress test is defined by the change ratio of the resistance of test structure. The resistance change ratio is defined as the ratio between the resistance after stress test and the initial resistance. Allowable resistance change is dependent on the circuit design, operating condition, and reliability target. Therefor the failure criteria is dependent on them. In general, failure criteria is from 10% to 30%.

3.5 Life time estimation

The extrapolated life time under the actual operating condition is calculated from the result of electromigration test. Acceleration factor between the test condition and the actual operating condition is given as equation (3) which is transformed from Black model of equation (2).

$$AF = \left(\frac{J_{st}}{J_{op}} \right)^{-n} \exp\left\{ \frac{E_a}{k} \left(\frac{1}{T_{op}} - \frac{1}{T_{st}} \right) \right\} \qquad \text{----- (3)}$$

AF	: Acceleration factor
J_{st}	: Stress current density
J_{op}	: Current density under the actual operating condition (A/cm^2)
T_{st}	: Stress temperature (K)
T_{op}	: Temperature under the actual operating condition (K)
E_a	: Activation energy (eV)
n	: Current density coefficient
k	: Boltzmann constant (8.62E-5 eV/K)

The time to certain failure rate is calculated from equation (4).

$$t_x = AF\left\{ \frac{MTTF}{\exp(\sigma \times Z)} \right\} \qquad \text{----- (4)}$$

t_x	: Time to cumulative failure x%
AF	: Acceleration factor
MTTF	: Mean time to failure by stress test
σ	: Standard deviation by stress test
Z	: Probability

COMMENTS Electromigration Test

1. TEST DURATION

The electromigration test duration is widely diferent between test conditions when the test purpose is obtaining Ea and/or n(current density acceleration factor) because the combination of stress temperature and current are various. Electromigration test is usually performed until the failure rate reaches to sufficient value for data analysis. However the test can be terminated at certain test time and extrapolation technique is used for TTF when expected test duration is too long.

2. TECHNICAL BACKGROUND

Further technical information and background is given in "Report on failure mechanism of LSI and its test method", April(1998), Technical Standardization Committee on Semiconductor Devices, EIAJ.

Test Method C-101
Soft Error Test Method for Memory Devices

1. SCOPE

This standard provides the test method of data retention ability of LSI memories against energetic particle such as alpha ray. This standard is applied on any type of LSI memories.

2. TEST EQUIPMENT

2.1 Equipment

The equipment should be able to measure the functions of the integrated circuit devices, and measure the time until the change of stored data by the exposure of energetic particles such as alpha ray (It is called the soft error). Or, the test equipment (memory tester etc.) which has the function that can count number of soft errors in unit time.

2.2 Alpha ray source

(a) Nuclide :Seal Type Am241

(b) Radioactivity :3.7×10^{3}~3.7×10^{6} Bq {0.1~100uCi}

The energy spectrum of the alpha ray source should be confirmed because the different test result is caused by the difference of the energy spectrum even if the alpha ray source have the same radioactivity.

If the emission area of the alpha ray is extremely smaller than the chip area, the correct result is not obtained because the decaying effect of the alpha ray through atmosphere and the chip protection film, and the incident angles effect are not taken into account. Therefore, to execute an accurate test, the extremely small emission area of the alpha ray in comparison with the chip area should not be used.

3. TEST SAMPLE

3.1 Sample

Any type of memory LSI's. The device parameters (capacitance of memory cell in DRAM etc.) which may affect soft error rate should be understood well.

3. 2 Notes for test samples

Bare surface of the sample is exposed by the method which does not ruin the electric characteristics. For example, the upper side of the package is cut with a small knife, the molding resin on the upper surfaces of the chips is dissolved chemically, etc. Unless otherwise specified, the chip coatings should be removed by the method which dose not ruin the electric characteristic because alpha ray from Am241 source(peak energy 5MeV approximately) is decayed by the chip coating. There are alpha rays of higher energy in the package materials or the natural radio-actives. However chip coating is not removed when the test purpose is evaluation of the effect of chip coating.

4. TEST PROCEDURE

4. 1 Alpha ray accelerated soft error test

(1) **Power supply voltage:**

The minimum voltage of recommended operating condition

(When required, the supply voltage dependence should be measured.)

(2) **Ambient temperature:**

Room temperature

(3) **Operation frequency:**

Depend on the samples.

(When required, the operation frequency dependence should be measured.)

(4) **Data pattern:**

Depend on the samples.

(The checker board or all "0/1"- read/write pattern is recommended.)

(5) **Distance between chip and radiation source: 1–5mm**

(6) **Number of measurement samples:**

Plural samples should be measured in consideration of the measurement dispersion. Moreover, the test should be done in a vacuum chamber to exclude the damping effect of the alpha ray energy in the atmosphere.

4. 2 System soft error test

In this method, the samples are mounted on memory boards of system machine which has similar function to the test equipment described in 2. 1. The soft errors under the similar condition to the actual use environment without acceleration alpha source.

(1) **Power supply voltage:**

The minimum voltage of recommended operating condition

(2) **Ambient temperature:**

From room temperature to maximum temperature of recommended operating condition

(3) **Operating frequency:**

Operating frequency depends on the samples but the evaluation is recommended to be performed about tCYC=0.5us-1us because the frequency for the stable operation that depends on the performance of the test equipment.

(4) **Data pattern:**

Depends on the samples

(The checker board or all "0/1"- read/write pattern is recommended.)

(5) **Test time:**

For 1000 hours or more (recommended)

(6) **Number of test samples:**

1000 pieces or more (recommended)

Especially, in the data retention test for SRAM etc. all "1" are written in the test samples in initial, the test samples are left with the battery back up mode and the evaluation by reading out is performed every predetermined intervals.

4. 3 Judgments

(1) **Alpha ray accelerated soft error test**

The soft error rate (SER) is calculated by the following equation.

$$SER = \frac{\text{SER in accelerated soft error test}}{\text{alpha ray flux in accelerated soft error test}} \times \text{alpha ray flux from package} \quad \text{-----(1)}$$

where, SER: soft error rate (fit).

In this method the conversion is performed with 1Bq=1 α /cm^2 · s. But the conversion should be paid attention because the error rates depend on the energy spectrum. In addition, the results of equation (1) is not corresponding to an actual soft error rate because the difference on the incident angle of alpha ray and the alpha ray damp in the atmosphere between the alpha ray source and the chip. Therefore, this test method should be used for a relative comparison betweeen current devices.

(2) System soft error test

This test is usually broken off to confirm the determined standard (for instance, 1000fit or less) or below because this test is not accelerated test and requires a large number of samples and time to understand the ability value.

$$SER = \frac{x}{\text{sample number} \times \text{test time}} \times 10^9 \quad \text{[FIT]} \qquad \text{----- (2)}$$

x is given by Chi-square distribution.

$\chi^2/2$ is given in table 1.

Table 1 x for FIT calculation ($\chi^2/2$)

Confidence Level			
60%		90%	
failure	x	failure	x
0	0.916	0	2.303
1	2.022	1	3.890
2	3.105	2	5.322
3	4.175	3	6.681

COMMENTS Soft Error Test Method for Memory Devices

1. Evaluation of soft error caused by neutron rays (cosmic rays)

There are few papers on the soft error accelerated test by neutron rays. Neutron soft error test requires neutron flux generated with nuclear reactor and accelerator. The particle accelerators to be able to generate neutron rays to perform soft error accelerated test are installed in only very few laboratories. It is widely recognized that the equipment which can generate neutron flux simulating the energy spectrum of cosmic rays exists only in Los Alamos national laboratory of the United States. Therefore, the execution of this test is difficult and test standard has not been established.

Neutron-induced soft error is included in the soft error rate of system soft error test because neutron flux is hard to shield. The evaluation should be performed in consideration of the environment as follows, because the neutron flux may depend on the place.

(a) Altitude

(b) Region/Latitude

(c) Room/Outdoor

(d) In case of room Structure, Floor, Thickness and Material of building

2. Technical Background

The other technical information and background is given in "Report on failure mechanism of LSI and its test method, Part 2", May (1999), Technical Standardization Committee on Semiconductor Devices, Failure Mechanism Driven/Wafer Reliability PG, EIAJ.