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Standard for I/O Interface Model for Integrated Circuits (IMIC)

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Standard for I/O Interface Model for Integrated Circuit (IMIC)

1. Scope

To standardize the electrical modeling of input signals, output signals, power supply and ground terminals of integrated circuits, in order to provide for analysis of electric characteristics of equipment using them. In the work, the following items shall be considered:

(1) To standardize in order to solve current problems and in order to extend capabilities of analysis, on the basis of results of the past standardization activities.

(2) To make the description rules for electric circuits more flexible, so that problems may be solved more easily.

(3) To introduce the concept of modeling levels to exchange relevant data for each application.

(4) To enhance electric modeling for packages and modules.

2. Outline

(1) Covered Range of Model

The model is described as circuits covering the whole or a part of the I/0 buffers and the package.

(2) Language for Circuits

The circuits are written in SPICE format. The structure allows to describe simple buffers, complex buffers, power and ground lines, packages and complex memory module boards in an unified format.

(3) Device Model

The characteristics of non-linear devices are described in 1-D, 2-D or 3-D table format.

(4) Structure of Data

The data of the model are separated into IC, package and module portions, so that each portion can be made independently by each designer.

(5) Simulation

The circuits of the models and the board on which ICs are mounted are merged for simulation. This brings accurate simulation result in any loading condition of the board.

(6) Relation to IBIS

Tools that can extract IBIS data from this model will be provided. Once IC makers provide this model, users can obtain both this model and the IBIS model drawn from it.

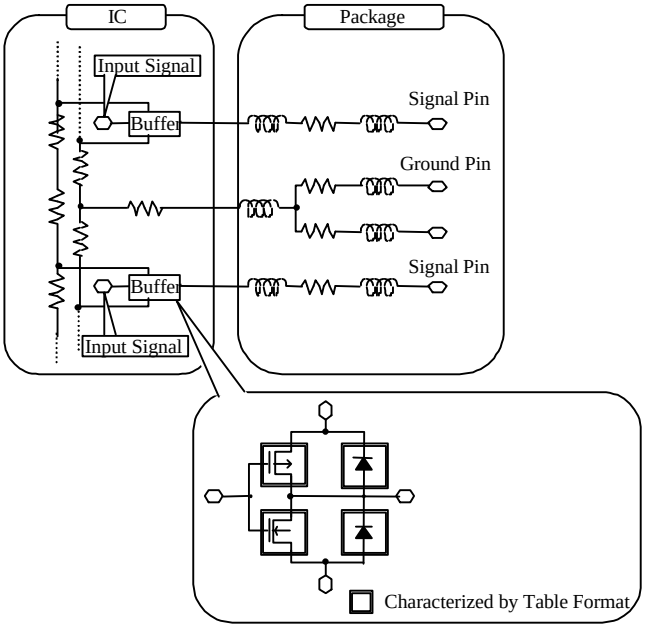


Figure 2.1 Outline of Model

3. Model Structures

The model must describe internal ICs, packages and module boards as shown in **Figure 3.1**.

The internal IC, package and module board models consist of the elements in **Table 3.1**.

The data structures of the internal IC, package and module board models are shown in **Figure 3.2**, **Figure 3.3**, and **Figure 3.4**, respectively.

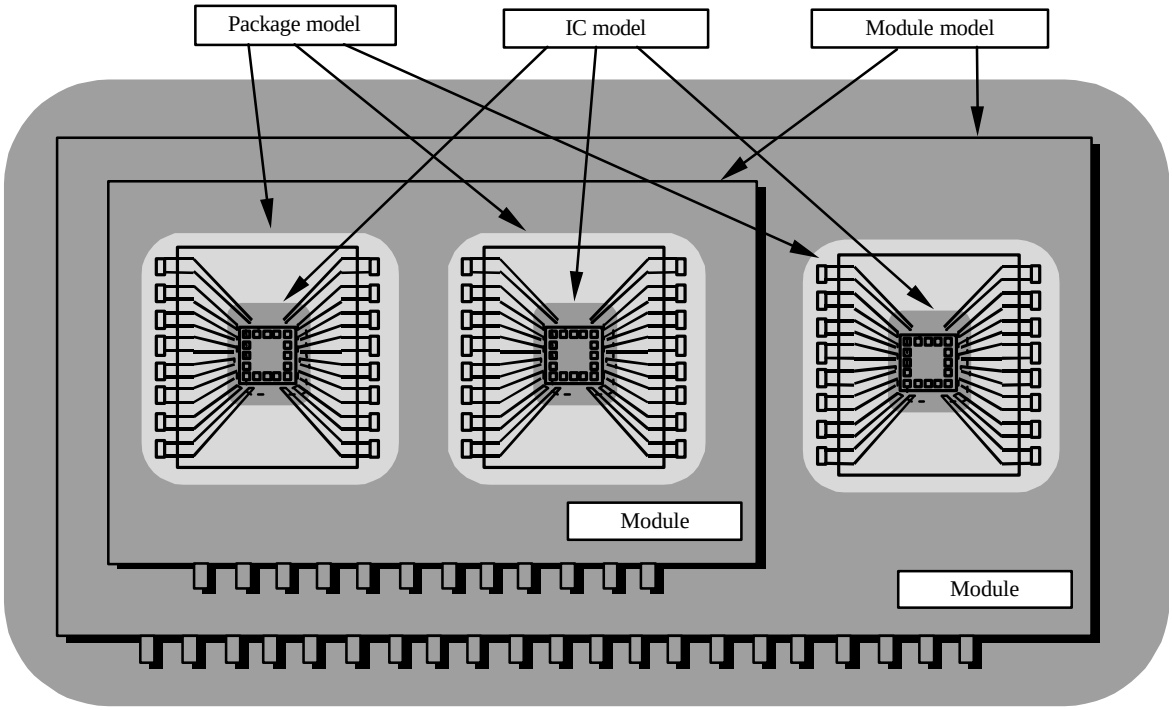


Figure 3.1 Hierarchy of Three Models

Table 3.1 Element of Model Structures

File	Element	Description
IC Model File	Header	IC type, model version, model level etc.
	External Terminal	IC external terminals (package pins).
	Pad Assignment	Connection between IC pads and package inner terminals.
	Circuit Description	Internal circuits and their connections.
	Input Stimulus Assignment	Internal circuits and their stimuli to generate output waveforms.
	Input Stimulus	Input waveforms.
	Device Model	Characteristics of nonlinear circuits in 1D-, 2D- and 3D-table data. Non-linear devices are transistors, diodes and so on.
	Package Model Reference	Name of the package model to be used.
Package Model File	Header	Package name, model version, model level, etc.
	Model Name	List of models in package circuit model.
	Inner Terminal	Cross-reference between internal terminals and package internal circuit model.
	Outer Terminal	Cross-reference between external circuit and package internal circuit model.
	Circuit Description	Internal circuits and their connections.
	Device Model	Characteristics of nonlinear circuits in 1D-, 2D- and 3D-table data. Non-linear devices are transistors, diodes and so on.
	Structure	Material, position, 3D-structures.
Module File	Header	Module name, model version, model level, etc.
	External Terminal	External terminals (pins) of module.
	Circuit Description	Internal circuits and their connections.
	Signal Source	Internal circuits and their terminals to generate output waveforms at corresponding external terminals.
	Device Model	Characteristic of nonlinear circuits in 1D-, 2D- and 3D-table data. Non-linear devices are transistors, diodes and so on.
	IC/Module Model Reference	Names of IC/module model files and model names used.
	Structure	Material, position, 3D-structures.

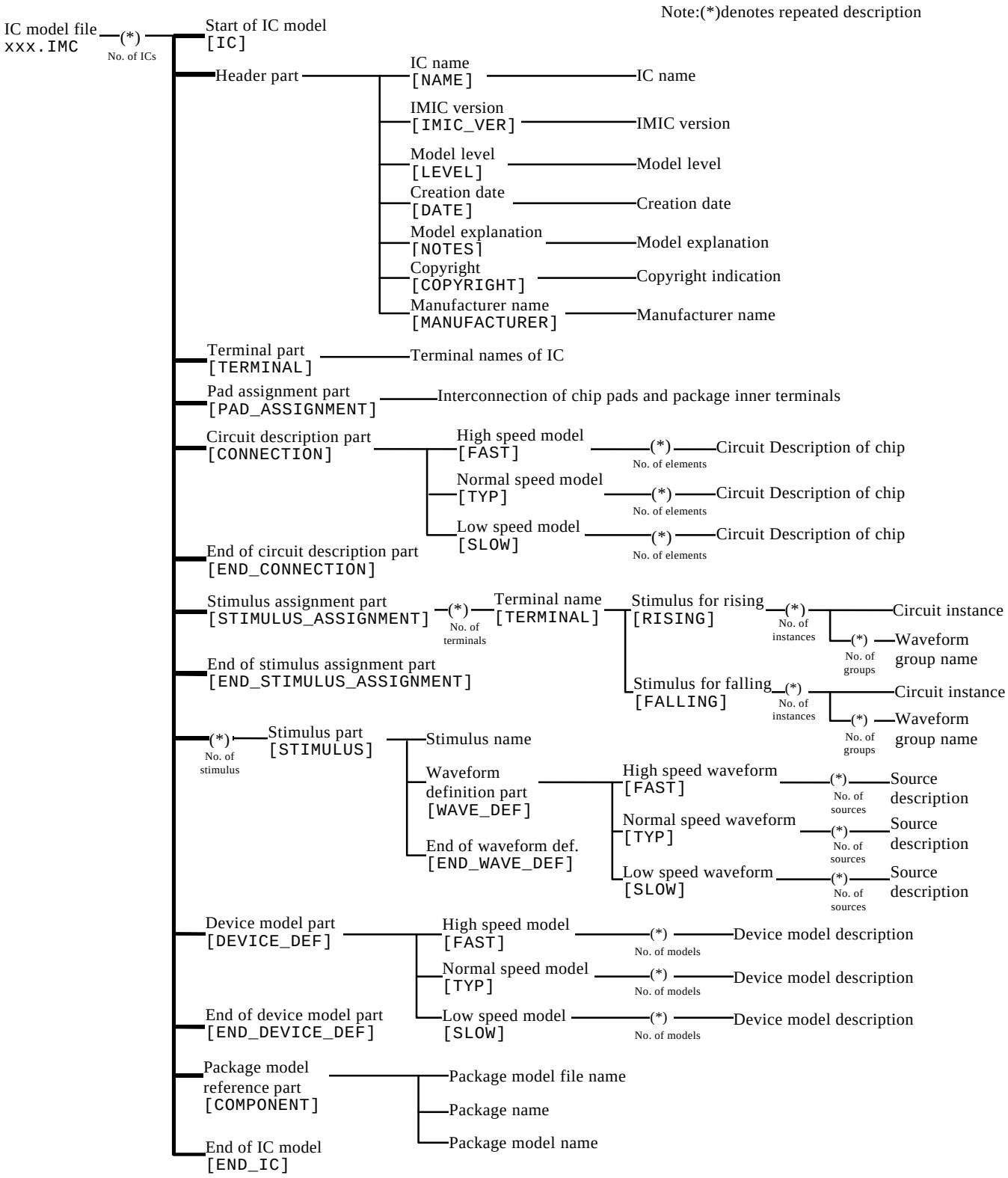


Figure 3.2 Data Structure of an IMIC IC Model File

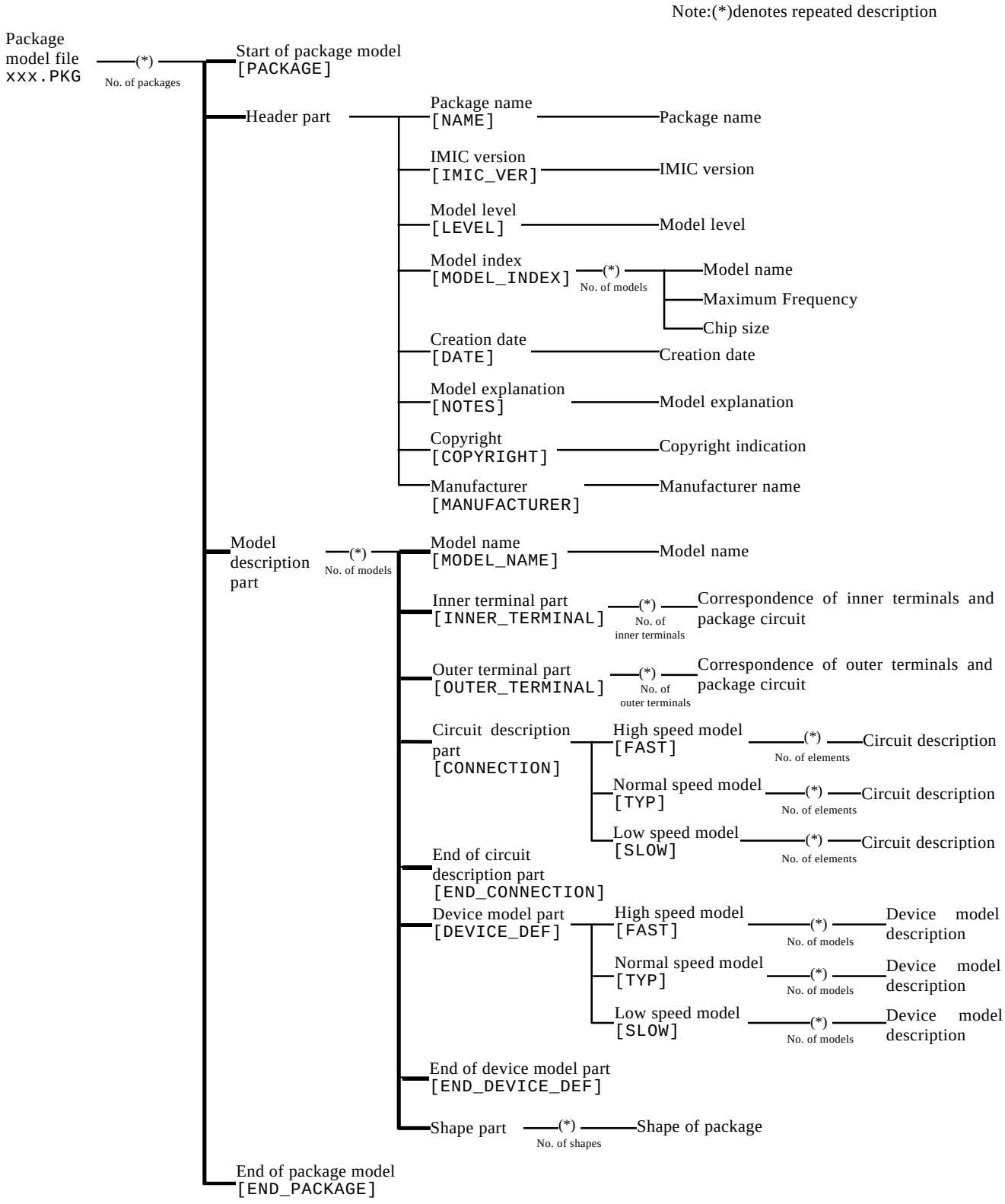


Figure 3.3 Data Structure of an IMIC Package Model File

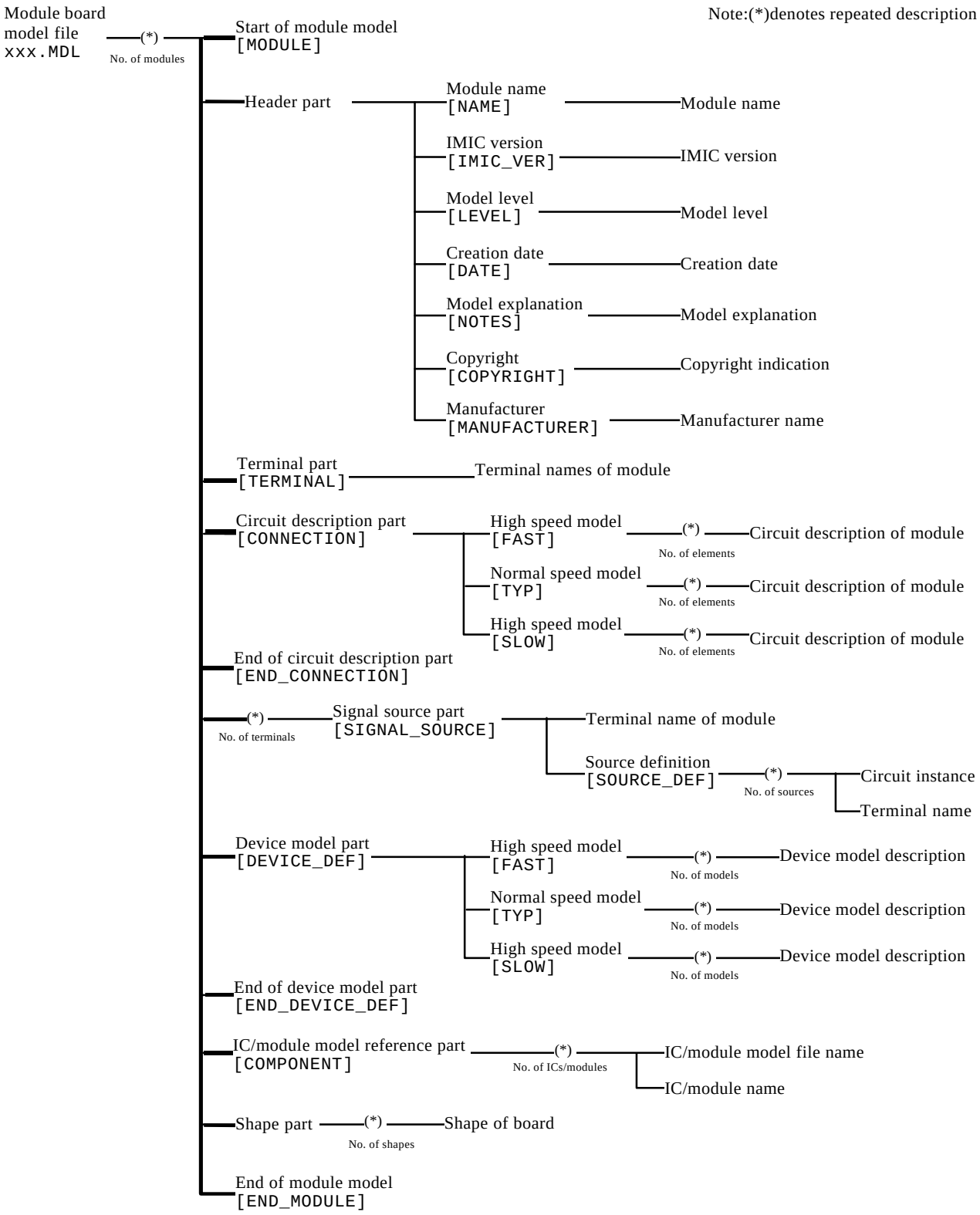


Figure 3.4 Data Structure of an IMIC Module Model File

4. Model Description Details

4.1 Description Rules

4.1.1 Characters

Recognition of characters in the model files is case insensitive. For instance, 'M' and 'm' are treated as the same character. It is recommended that all upper case or all lower case characters should be used.

4.1.2 Available Characters

(a) Available Characters

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890 + - /#!<>_%

(b) Special Characters

[ ] : Keywords

" ' : Equations

. : File Extension

Space, TAB : Delimiter

4.1.3 Keywords

Keywords must be enclosed in square brackets, [ ], and must start in column 1 of the line. Tab or space should not be used within [ ]. The details will be described on the same line as the keyword, and/or the following lines. There are three types of keyword/detail formats:

(a) Type-1

The details are described in the following lines.[END_ ...] is used to declare the end of the details of the keyword.

Example:

```
[IC]
....
[END_IC]
```

(b) Type-2

The details are described in the following lines. There is no END_ marker.

Example:

```
[TERMINAL]
.SUBCKT ALVCH16244 SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG
```

(c) Type-3

The details are described in the same line as the keyword. There is no END_ marker.

Example:

```
[NAME] ALVCH16244
```

4.1.4 Numbers

A scaling factor or scientific notation is allowed. However, these may not be used in combination.

(a) Scaling factor

T (tera) : 10^{12} G (giga) : 10^{9} MEG, X (meg) : 10^{6} K (kiro) : 10^{3}

M (mili) : 10^{-3} U (micro) : 10^{-6} N (nano) : 10^{-9} P (pico) : 10^{-12}

F (femto) : 10^{-15}

(b) Scientific notation

Scientific notation should use "E".

(c) Examples

```
1.3X=1.3E6=1300K=1300E3=1300000
0.5U=5E-7=500N=500E-9=0.0000005
```

4.1.5 Comment

If an asterisk "*" appears in the first column in a line, the following characters are considered as a comment. If a "$" exists anywhere in a line, the following characters are considered as a comment.

4.1.6 Order of Descriptions

Descriptions in the file must be ordered as shown in Figures 3.2, 3.3, and 3.4, where items at the top of a solid vertical line are to be at the beinning, and items at the bottom are to be at the end. Items along horizontal line may appear in any order with respect to each other.

4.2 IC Model File

4.2.1 File name

The name of the model file should start with any alphabetical or numerical characters, with IMC as an extension.

No limit is specified for the number of characters in a file name.

(a) Example

ALVCH16244.IMC

(b) Notes

For DOS, more than 9 characters other than extension will be ignored.

4.2.2 Start and End of Model Description

One model description should be provided per single IC model.

(1) Start of IC model description

(a) Description

[IC]

(b) Explanation

The contents of the model follow.

(2) End of IC model description

(a) Description

```
[END_IC]
```

(b) Explanation

The description of the IC model will be terminated by this description.

4.2.3 Header

IC type, model level etc. will be described Start of IC model description

(1) IC type

(a) Description

`[NAME]` Characters

(b) Explanation

IC type identifier (Product Number/Name). This is used by simulators to locate the correct model for an IC in a design.

(c) Example

```
[NAME] ALVCH16244
```

(2) Model version

(a) Description

[IMIC_VER] Characters

(b) Explanation

The IMIC specification version that the file conforms to. Currently only version 1.3 is supported. Parsers must follow appropriate syntax rules for the entire IC model.

(c) Example

```
[IMIC_VER]  1.3
```

(3) Model level

(a) Description

[LEVEL] Integer

(b) Explanation

Level 1: SI (Signal Integrity) model for the analysis of signal noise.

Level 2: PI (Power Integrity) model for the analysis of power noise including signal noise.

Level 3: EMI (Electromagnetic Interference) model for the analysis of radiated emission noise.

Details will be explained in Chapter 5.

(c) Example

```
[LEVEL]  2
```

(4) Date

(a) Description

[DATE] Characters

(b) Explanation

The model release date is described using any of the following formats.

· Month / Day / Year Example : 3/23/98

· Day / Month / Year Example : 23MAR98

· Month Day, Year Example : MARCH 23, 1998

(c) Example

```
[DATE]  3/23/98
```

(5) Explanation of model

(a) Description

[NOTES]

Arbitrary notes concerning the model. This may be used for explanations of the origin, usage, and testing of the model, for example.

(b) Explanation

Any comments can be described on the lines following the keyword [NOTES].

(c) Example

```
[NOTES]
ELECTRICAL MODEL FOR ALVCH16244
```

(6) Copyright

(a) Description

[COPYRIGHT] Characters

(b) Explanation

Copyright holder and related terms are stated.

(c) Example

```
[COPYRIGHT] COPYRIGHT 1998, ZYX CORP., ALL RIGHTS RESERVED
```

(7) Manufacture

(a) Description

[MANUFACTURER] Characters

(b) Explanation

Manufacture is declared here.

(c) Example

```
[MANUFACTURER]   ZYX CORP.
```

4.2.4 Terminals

The external terminals of IC are defined. The external terminals are the IC pins.

(a) Description

[TERMINAL]

(b) Explanation

The external terminals of the IC are defined.

The data begins on the line following the keyword [TERMINAL].

Signal names of IC external terminals at the "pad assign" should be described.

The IC type name follows the string ".SUBCKT", and the names of terminals follow that.

Continuation lines, if needed, start with "+" in the first column.

(c) Example

```
[TERMINAL]
.SUBCKT ALVCH16244 SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG
```

4.2.5 Pad Assignment

The interconnections between chip pads and package inner terminals are described.

(a) Description

[PAD_ASSIGNMENT]

(b) Explanation

The interconnections between chip pads and package inner terminals are described.

The data begins on the line following the keyword [PAD_ASSIGNMENT].

Signal names of package inner terminals that are connected to chip pads must match the signal names of the corresponding chip pads in .SUBCKT" statement of [CONNECTION].

The data is given as subckt instance statements, starting with "X".

The subckt name of the top level ".SUBCKT" in [CONNECTION] should appear at the end, after the terminal names.

Following SPICE conventions, use of a particular node name (also known as a signal name) on both the chip instance and the package instance signifies a connection between these

terminals.

Continuation lines start with "+" in the first column.

(c) Notes

If a chip pad is not connected to any package pad, the chip pad terminal should be connected to signal "NO_CONNECTION". If a package inner terminal is not connected to any chip pad, the inner terminal should be connected to signal "NO_CONNECTION".

(d) Example

In the example below, the signal "SIG1I" is connection of the first terminal of the CHIP to the first terminal of the PACKAGE.

```
[PAD_ASSIGNMENT]
XCHIP SIG1I SIG2I SIG3I SIG4I SIG5I SIG6I CHIP
XPACKAGE  SIG1I SIG2I SIG3I SIG4I SIG5I SIG6I
+ SIG1  SIG2  SIG3 SIG4 SIG5 SIG6  SIG7  REFG  PACKAGE
[CONNECTION]
.SUBCKT   CHIP  PAD1   PAD2   PAD3   PAD4   PAD5  PAD6
.....
.ENDS CHIP

<Package model file>
[CONNECTION]
.SUBCKT  PACKAGE  L1I  L2I  L3I  L4I  L5I  L6I
+ LEAD1  LEAD2  LEAD3  LEAD4  LEAD5  LEAD6  LEAD7  REFG
.....
.ENDS  PACKAGE
```

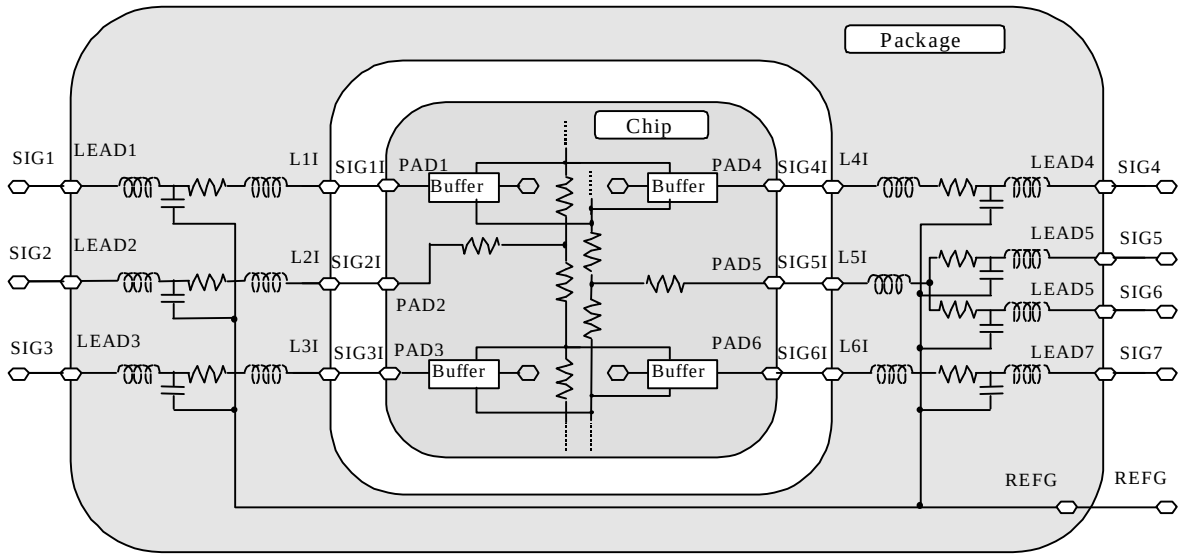


Figure 4.1 Pad Assignment

4.2.6 Circuit Description

This describes elements of the internal circuit and their interconnections.

(a) Description

```
[CONNECTION]
[FAST]
[TYP]
[SLOW]
[END_CONNECTION]
```

(b) Explanation

This describes elements of internal circuit and their interconnections. The description is terminated with `[END_CONNECTION]`.
Circuit descriptions with sub-keywords are described after `[CONNECTION]`.
These sub-keywords are optional.

`[FAST]` Circuit description for the highest speed.
`[TYP]` Circuit description for typical speed.
`[SLOW]` Circuit description for the lowest speed.

The internal circuit of the chip contains the pad capacitance model statements.
The top level description of the internal circuit is located between .SUBCKT and .ENDS.
.SUBCKT Subcircuit name of the top level circuit <Pad Signal Names>
.ENDS Subcircuit name of the top level circuit

The general circuit description is as follows.

Element_Name <Node_Name> [Value] [Model_Name] <[Parameter = Parameter_Value]>

Where < > indicates repeatable and [ ] indicates optional.
Any statement beginning with + is considered to be a continuation of the previous statement.
Available elements are resistor, capacitor, inductor, coupling coefficient, diode, MOS Transistor, Bipolar Transistor, Voltage Controlled Voltage Source, Current Controlled Current Source, Voltage Controlled Current Source, Current Controlled Voltage Source, Lossless Transmission Line, Independent Voltage Source, Independent Current Source, Subcircuit Call, and Subcircuit Description. The first character of each element statement denotes the element type. The model name must be the name defined in the device description.
Each element description is as follows.

(i) Resistor

Rxxxxxxx node1 node2 value or model_name
Where unit of *value* is Ω

(ii) Capacitor

Cxxxxxxx node1 node2 value or model_name

Where unit of *value* is (F) Farad.

(iii) Self-Inductor

Lxxxxxxx node1 node2 value

Where unit of *value* is (H) Henry.

(iv) Mutual-Inductor

Kxxxxxxx lname1 lname2 Coupling_coefficient

Where *lname1* and *lname2* are self-inductance names.

(v) Diode

Dxxxxxxx node1 node2 model_name AREA=area_factor

(vi) MOS Transistor

Mxxxxxxx node1 node2 node3 node4 model_name L= gate_length W= gate_width

[+ AD= drain_diffusion_area AS= source_diffusion_area]

[+ PD= perimeter_of_drain_junction PS= perimeter_of_source_junction]

[+ NRD= number_of_squares_of_drain_diffusion NRS= number_of_squares_of_source_diffusion]

Where the units of gate_length, gate_width, perimeter_of_drain_junction, perimeter_of_source_junction are meters, and those of drain_diffusion_area and source_diffusion_area are m^2.

AD, AS, PD, PS, NRD and NRS are optional. The default value for these is 0.0.

These values are not necessarily the real size of any chip dimension. Characteristics of individual transistors will be calculated by using equations with dependence of L, W, AD, AS, PD and PS, which are defined in device model description.

It will be described in detail in 4.2.8 (g) and (h).

(vii) Bipolar Transistor

Qxxxxxxx node1 node2 node3 model_name AREA=area_factor

(viii) Voltage Controlled Voltage Source

Exxxxxxx node1 node2 POLY=n <cnode1 cnode2> <k>

Where *cnode1* and *cnode2* are controlling nodes, *k* is the list of polynomial coefficients.

(ix) Current Controlled Current Source

Fxxxxxxx node1 node2 POLY=n <vname> <k>

Where *vname* are voltage sources, *k* is the list of polynomial coefficients.

(x) Voltage Controlled Current Source

Gxxxxxxx node1 node2 POLY=n <cnode1 cnode2> <k>

Where *cnode1* and *cnode2* are controlling nodes, *k* is the list of polynomial coefficients.

(xi) Current Controlled Voltage Source

Hxxxxxxx node1 node2 POLY=n <vname> <k>

Where *vname* are voltage sources, *k* is the list of polynomial coefficients.

(xii) Lossless Transmission Line

Txxxxxxx node1 node2 node3 node4 Z0=characteristic_impedance

+ TD= transmission_delay

(xiii) Independent Voltage Source

Vxxxxxxx node1 node2 [tranfun] [DC=]dcvalue [AC=acmag, [acphase]]

Where *dcvalue* is DC source value. *Acmag* is AC magnitude and *acphase* is AC phase.

Tranfun is transient source function described below:

- Pulse Source Function

PULSE *v*1 *v*2 [*td* [*tr* [*tf* [*pw* [*per*]]]]]

Where *v*1 is initial value, *v*2 is pulse plateau value, *td* is delay time, *tr* is duration of the onset ramp, *tf* is duration of the recovery ramp, *pw* is pulse width, and *per* is pulse repetition period.

- Sinusoidal Source Function

SIN *v*o *v*a [*freq* [*td* [θ[φ]]]]

Where *v*o is voltage or current offset, *v*a is voltage or current amplitude, *freq* is frequency, *tr* is delay, θ is damping factor, and φ is phase delay.

- Exponential Source Function

EXP *v*1 *v*2 [*td* [τ1 [*td*2 [τ2]]]]

Where *v*1 is initial voltage or current, *v*2 is pulsed value of voltage or current, *td* is rise delay time, *td*2 is fall delay time, τ1 is rise time constant and τ2 is fall time constant.

- Piecewise Linear Source Function

PWL t1 v1 [t2 v2 t3 v3 ...] [R [=repeat]] [TD=delay]

Where *v*1... is voltage or current values, *t*1 ... is segment time, *repeat* is the start point of the waveform, which is to be repeated, and *delay* is delay time. R causes the function to repeat.

- Single-Frequency FM Source Function

SFFM *vo* *va* [*fc* [*mdi* [*fs*]]]

Where *vo* is voltage or current offset, *va* is voltage or current amplitude, *fc* is carrier frequency, *mdi* is modulation index and *fs* is signal frequency.

(xiv) Independent Current Source

Ixxxxxxx node1 node2 [tranfun] [DC=]dcvalue [AC=acmag, [acphase]]

Where *dcvalue* is DC source value. *Acmag* is AC magnitude and *acphase* is AC phase.

Tranfun is transient source function described in (xiii).

(xv) Subcircuit Call

Xxxxxxxx <node> subcircuit_name

(xvi) Subcircuit Definition

.SUBCKT subcircuit_name <node>

(c) Example

```
[CONNECTION]
[TYP]
.SUBCKT CHIP OUT1 OUT2 VCC GND0 SUB
R1 VCC2 VCC1 1.0
R2 VCC1 VCC3 1.2
R3 GND2 GND1 1.1
R4 GND1 GND3 0.9
R5 VCC1 VCC 0.5
R6 GND1 GND0  0.5
C1 VCC2  SUB   1P
C2 VCC3  SUB   1P
X1 IN1 OUT1 VCC2 GND2 BUFFER
X2 IN2 OUT2 VCC3 GND3 BUFFER
.ENDS CHIP
.SUBCKT BUFFER IN OUT VCC GND0
M1 IN OUT VCC VCC PMOS L=1U W=10U
M2 IN OUT GND0 GND0 NMOS L=1U W=10U
D1 OUT VCC D AREA=2
D2 GND0 OUT D
.ENDS BUFFER
[END_CONNECTION]
```

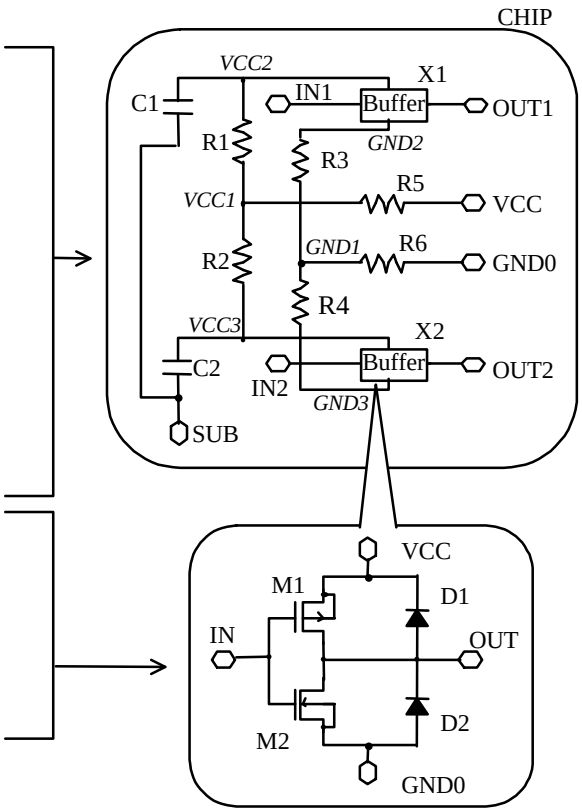


Figure 4.2 Example of circuit description

(d) Notes

The grounds of internal circuits of ICs are connected to package ground terminals. Therefore, the reserved node names for ideal reference ground such as 0, GND, GND! or GROUND cannot be used as signal names for these connections.

4.2.7 Input Stimulus

In order to describe the effect of loading on the output waveforms of buffer circuits, the input stimuli should be defined both for rising and falling edges of the output buffer circuits.

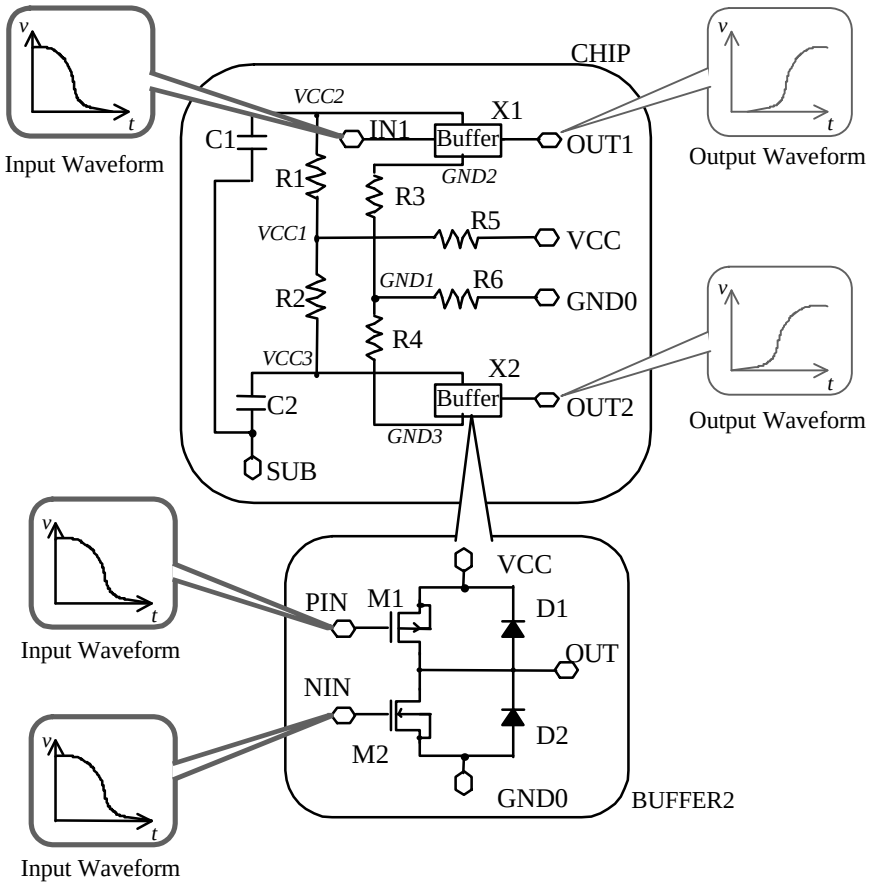


Figure 4.3 Input stimulus

(1) Input Stimulus Assignment

(a) Description

```
[STIMULUS_ASSIGNMENT]
[TERMINAL] External terminal name of IC
[RISING]
[FALLING]
[END_STIMULUS_ASSIGNMENT]
```

(b) Explanation

This defines the input stimulus names of output buffer circuits so that it can control the output waveforms of IC. The input stimulus section begins with `[STIMULUS_ASSIGNMENT]` and is terminated with `[END_STIMULUS_ASSIGNMENT]`. The `[STIMULUS_ASSIGNMENT]` section contains one or more `[TERMINAL]` subsections, each defining the stimulus waveform to be used for one chip pad terminal.

`[TERMINAL]` External terminal name of IC

The external terminal name of the IC should match one of the signal names at the external terminals defined by the .SUBCKT in `[TERMINAL]`. Each `[TERMINAL]` section contains `[RISING]` and `[FALLING]` subsections to introduce separate stimulus waveforms to be used for rising and falling edges of the signal.

[RISING]

The input stimulus to control the rising waveforms of external terminals should be defined following this keyword.

The first parameter is a reference name for the circuit that provides the stimulus.

To reference the top hierarchy of the chip, the reference name should be one of the items defined by [PAD_ASSIGNMENT].

To reference the lower hierarchy level of the chip, the reference name should be one of the subcircuit call names defined in [CONNECTION].

The other parameters are the names of waveforms defined by [STIMULUS]. These can be described in the same line such as Circuit_reference_name Stimulus_1 Stimulus_2 Stimulus_3...

[FALLING]

The input stimulus to control the falling waveforms of external terminals should be defined following this keyword. Usage rules for [RISING] apply to [FALLING] as well.

(c) Example

```
[STIMULUS_ASSIGNMENT]
[TERMINAL] OUT1
[RISING]
XCHIP   WAVE1R
[FALLING]
XCHIP   WAVE1F
[TERMINAL] OUT2
[RISING]
XCHIP.X2   WAVE2R
[FALLING]
XCHIP.X2   WAVE2F
[END_STIMULUS_ASSIGNMENT]
```

(2) Input Stimulus Definition

(a) Description

```
[STIMULUS] Stimulus Names
[WAVE_DEF]
[FAST]
[TYP]
[SLOW]
[END_WAVE_DEF]
```

(b) Explanation

This defines the input stimuli of output buffer circuits so that they can control the output waveforms of the ICs.

Stimulus names are described after the [STIMULUS] keyword. These are the names to be used for [WAVE_DEF]. Actual waveforms should be described by the circuit statements following these keywords.

[FAST] : Definition of the highest speed.
[TYP] : Definition of the typical speed.
[SLOW] : Definition of the lowest speed.

These keywords are optional. Actual waveforms should be defined from the next line of these keywords. The waveforms can be described using an independent voltage source or independent current source. More than one stimulus can be described.
The description of actual waveforms is terminated with [END_WAVE_DEF].

(c) Example

```
[STIMULUS] WAVE1R
[WAVE_DEF]
[FAST]
VIN1 IN1 GND PWL 0 3.3 4.8N 3.3 5.5N 0
[TYP]
VIN1 IN1 GND PWL 0 3.3 5N 3.3 6N 0
[SLOW]
VIN1 IN1 GND PWL 0 3.3 5.2N 3.3 6.4N 0
[END_WAVE_DEF]
[STIMULUS] WAVE2R
[WAVE_DEF]
[FAST]
VIN2 PIN GND PWL 0 3.3 2.8N 3.3 3.6N 0
VIN3 NIN GND PWL 0 3.3 2.6N 3.3 3.6N 0
[TYP]
VIN2 PIN GND PWL 0 3.3 3N 3.3 4N 0
VIN3 NIN GND PWL 0 3.3 3N 3.3 4N 0
[SLOW]
VIN2 PIN GND PWL 0 3.3 3.2N 3.3 4.3N 0
VIN3 NIN GND PWL 0 3.3 3.2N 3.3 4.3N 0
[END_WAVE_DEF]
[STIMULUS] WAVE1F
[WAVE_DEF]
[FAST]
VIN1 IN1 GND PWL 0 0 4.8N 0 5.6N 3.3
[TYP]
VIN1 IN1 GND PWL 0 0 5N 0 6N 3.3
[SLOW]
VIN1 IN1 GND PWL 0 0 5.2N 0 6.5N 3.3
[END_WAVE_DEF]
[STIMULUS] WAVE2F
[WAVE_DEF]
[FAST]
```

```
VIN2 PIN GND PWL 0 3.3 2.8N 3.3 3.6N 0
VIN3 NIN GND PWL 0 3.3 2.N 3.3 3.6N 0
[TYP]
VIN2 PIN GND PWL 0 3.3 3N 3.3 4N 0
VIN3 NIN GND PWL 0 3.3 3N 3.3 4N 0
[SLOW]
VIN2 PIN GND PWL 0 3.3 3.2N 3.3 4.4N 0
VIN3 NIN GND PWL 0 3.3 3.2N 3.3 4.4N 0
[END_WAVE_DEF]
```

(d) Notes

The stimuli defined by [FAST], [TYP] and [SLOW] correspond to the characteristics of nonlinear devices for [FAST], [TYP], and [SLOW] operating conditions, respectively. Thus, simulation for [TYP] stimulus should use corresponded [TYP] nonlinear characteristics of device models.

4.2.8 Device Model

This describes characteristics of nonlinear devices. Variables are one-, two-, and three-dimensional data. Nonlinear devices are transistor, diode, voltage dependent capacitor and so on.

(a) Description

```
[DEVICE_DEF]
[FAST]
[TYP]
[SLOW]
[END_DEVICE_DEF]
```

(b) Explanation

This defines device models to be used in the definition of the internal circuit of the IC. The definition of the device model should be terminated with [END_DEVICE_DEF]. The device model of the internal circuit can be defined by using the following keywords after [DEVICE_DEF].

[FAST] : Definition of the highest speed.
[TYP] : Definition of the typical speed.
[SLOW] : Definition of the lowest speed.

These keywords are optional. General description of device models is as follows.
.MODEL Model_name Model_type <[Parameter_name = Parameter_value]>
Where < > indicates repeatable and [ ] indicates optional.
Any statement beginning with + is considered to be the continuation of the previous statement.

(i) Diode Model

The Model_type should be followed by "MODEL= TABLE", "RS=series_resistance_value", "POINTS=Number_of_data_points" and <Voltage_value, Current_value, Capacitance_value>.

A set of numbers is composed of 3 parameter values. If any parameter has the same value in every set of numbers, the parameter can be removed from every set of numbers, adding "*Parameter_name=Parameter_value*" following "POINTS=*Number_of_data_points*". *Number_of_data_points* is the number of sets of parameter values.
"RS=*series_resistance_value*" is optional. In default, RS=0.0.

Equivalent Circuit

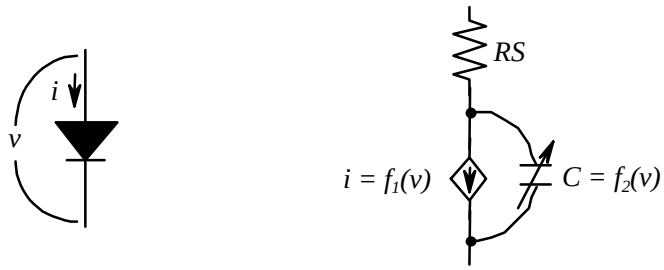


Figure 4.4 Diode Equivalent Circuit

Example

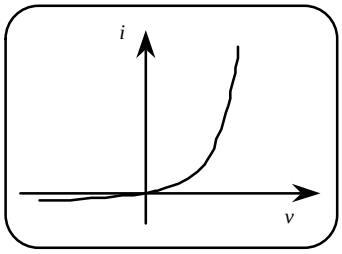


Figure 4.5 Diode Characteristics

```
[DEVICE_DEF]
 [FAST]
.MODEL DIODE D MODEL=TABLE
+ RS=3.2
+ POINTS=40
*  V     I      C
+ -0.5  0.001  0.2P
+  0.0  0.095  0.2P
+  0.2  2.0    0.2P
+  0.5  3.5    0.2P
+  ...
[END_DEVICE_DEF]
```

(ii) MOS Transistor Model

The Model_type should be followed by "MODEL= TABLE", "L=gate_length", "W=gate_width", "AD=drain_diffusion_area", "AS=source_diffusion_area",

"PD=perimeter_of_drain_junction", "PS=perimeter_of_source_junction" and "RSH=drain_and_source_diffusion_sheet_resistance".

AD, AS, PD, PS and RSH are optional. default value for these is 0.0.
If any value is 0.0, the dependency equations corresponding to the value will not be used.
The dependency equations will be described in detail in 4.2.8 (e) and (f).

Equivalent Circuit

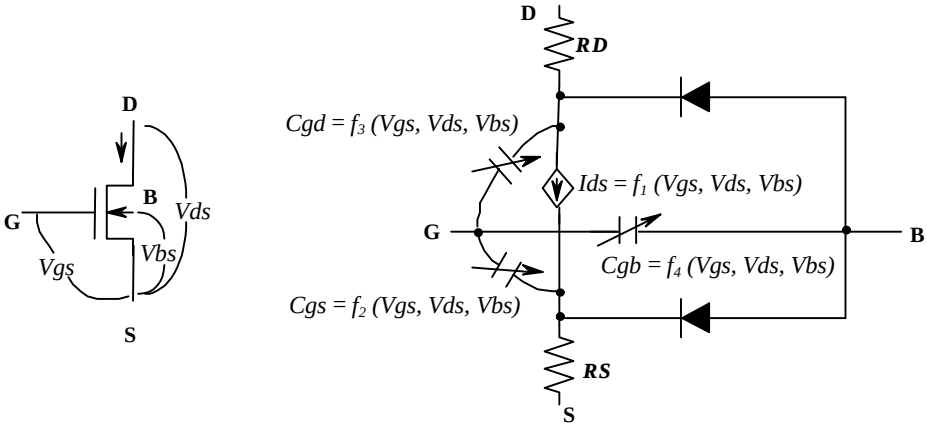


Figure 4.6 NMOS Transistor Equivalent Circuit

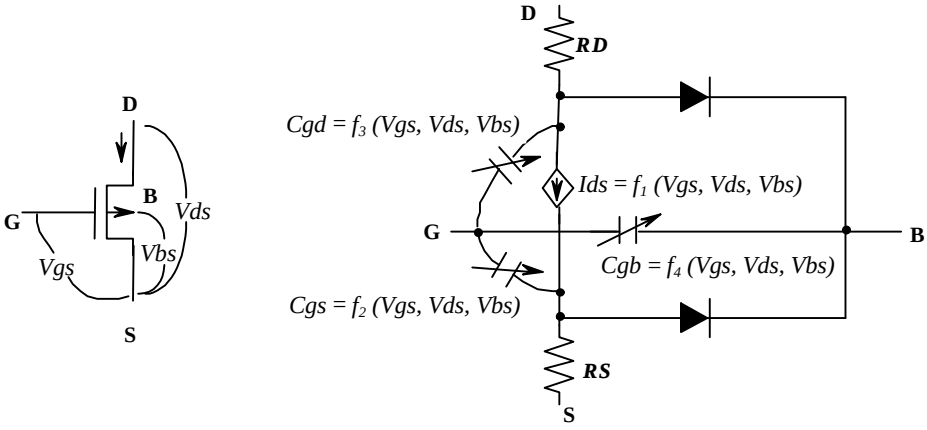


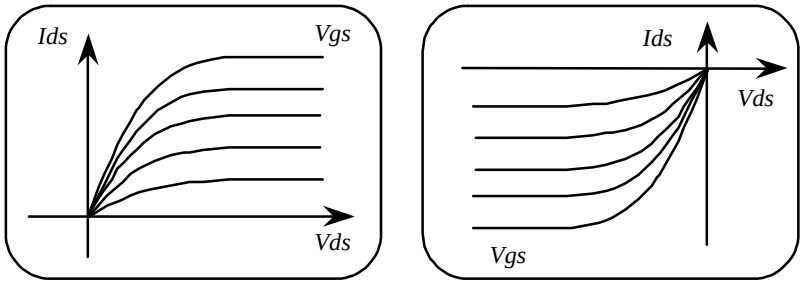
Figure 4.7 PMOS Transistor Equivalent Circuit

- Gate Channel Characteristics

DC and capacitance characteristics of the gate channel of MOS transistors should be described. "DATA=CHANNEL" should be followed by "POINTS=*Number_of_data_points*", <*Gate-source_voltage_value* (*Vgs*), *Drain-source_voltage_value* (*Vds*), *Bulk-source_voltage_value* (*Vbs*), *Drain_current_value* (*Ids*), *Gate-source_capacitance_value* (*Cgs*), Gate-drain_capacitance_value (Cgd), and Gate-bulk_capacitance_value (Cgb)>.

A set of numbers is composed of 7 parameter values. If any parameter has the same value in

every set of numbers, the parameter can be removed from every set of numbers, adding "*Parameter_name=Parameter_value*" following "POINTS=*Number_of_data_points*".
For example, if *Vbs* is 0.0 in every set of numbers, "VBS=0.0" is described following "POINTS=*Number_of_data_points*". In this case, the set of numbers is composed of 6 parameter values.
Number_of_data_points is the number of sets of parameter values.
The polarities of the values at the saturation region of MOS transistor are such that for NMOS all the parameters are positive, but for PMOS *Vgs*, *Vds* and Ids are negative and *Cgs*, *Cgd*, and *Cgb* are positive.



NMOS PMOS

Figure 4.8 Gate Channel Characteristics of MOS Transistor

Example

```
[DEVICE_DEF]
[TYP]
.MODEL MODEL1 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=30U PS=30U RSH=10.2
+ DATA=CHANNEL
+ POINTS=40
* Vgs   Vds    Vbs   Ids    Cgs    Cgd   Cgb
+ 0.0  0.095   0.2   2.0M   0.5N   0.5N  3.5N
+ 0.0  0.095   0.3   2.1M   0.7N   0.5N  4.0N
+ 0.2  2.1     0.2   2.0M   0.5N   0.5N  3.5N
+ 0.5  4.0     0.3   2.1M   0.7N   0.5N  4.0N
+  ...
.MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P 100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=90
+ VBS=0
* Vds    Vbs   Ids    Cgs    Cgd    Cgb
+ 0.0  0.095   2.0M  0.5N   0.5N   3.5N
+ 0.0  0.095   2.1M  0.7N   0.5N   4.0N
+ 0.2  2.1     2.0M  0.5N   0.5N   3.5N
```

```
+ 0.5  4.0     2.1M  0.7N   0.5N   4.0N
+  ...
[END_DEVICE_DEF]
```

- Junction Diode Characteristics

The DC and capacitance characteristics of junction diodes between source and substrate and between drain and substrate should be described.

"DATA=DRAIN" for the characteristics of DC and capacitance between drain and substrate of junction diode should be followed by "POINTS=*Number_of_data_points*", <*Bulk-drain_voltage_value* (*Vbd*), *Bulk-drain_current_value* (*Ibd*), *Bulk-drain_capacitance* (*Cbd*) and *Sidewall_bulk-drain_junction_capacitance* (*Cbdsw*)>.

A set of numbers is composed of 4 parameter values. If any parameter has the same value in every set of numbers, the parameter can be removed from every set of numbers, adding "*Parameter_name=Parameter_value*" following "*POINTS=Number_of_data_points*".

For example, if Cbd is1.2pF in every set of numbers, "CBD=1.2P" is described following "POINTS=*Number_of_data_points*". In this case, the set of numbers is composed of 3 parameter values.

Number_of_data_points is the number of sets of parameter values.

The polarities of the values for forward region of diode are such that for NMOS all the parameters are positive, but for PMOS *Vbd* and *Ibd* are negative and *Cbd* is positive.

"DATA=SOURCE" for the characteristics of DC and capacitance between source and substrate of junction diode should be followed by "POINTS=*Number_of_data_points*", < *Bulk-source_voltage_value* (*Vbs*), *Bulk-source_current_value* (*Ibs*), *Bulk-source_capacitance* (*Cbs*) and *Sidewall_bulk-source_junction_capacitance* (*Cbssw*) >.

A set of numbers is composed of 4 parameter values. If any parameter has the same value in every set of numbers, the parameter can be removed from every set of numbers, adding "*Parameter_name=Parameter_value*" following "POINTS=*Number_of_data_points*".

For example, if *Cbs* is1.2pF in every set of numbers, "CBS=1.2P" is described following "POINTS=*Number_of_data_points*". In this case, the set of numbers is composed of 3 parameter values.

Number_of_data_points is the number of sets of parameter values.

The polarities of the values for forward region of diode are that for NMOS all the parameters are positive, but for PMOS, *Vbs* and *Ibs* are negative and *Cbs* is positive.

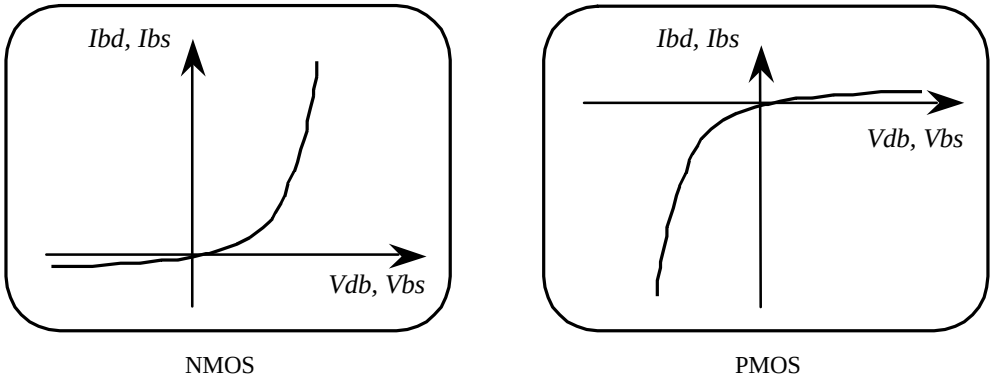


Figure 4.9 Characteristics of Junction Diode in MOS Transistor

Example

```
[DEVICE_DEF]
[SLOW]
.MODEL MODEL1 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=30U PS=30U RSH=10.2
+ DATA=CHANNEL
+  ...
+ DATA=DRAIN
+ POINTS=90
*  Vbd    Ibd      Cbd   Cbdsw
+ -2.0   0.095M   0.2P   0.01P
+  0.0   0.09M    0.3P   0.01P
+  0.6   4.0M     0.3P   0.012P
+  ...
+ DATA=SOURCE
+ POINTS=70
+ CBS=1.2P CBSSW=0.01P
*  Vbs    Ibs
+ -2.0   0.095M
+  0.0   0.09M
+  0.6   4.0M
+  ...
[END_DEVICE_DEF]
```

(iii) Bipolar Transistor Model

The Model_type should be followed by "MODEL=TABLE", "POINTS=Number_of_data_points", "RB=base_resistance_value", <Collector-emitter_voltage_value(Vce), Base-emitter_voltage_value(Vbe), Base_current_value(Ib), Collector_current_value(Ic), Collector-base_capacitance_value(Ccb), Collector-substrate_capacitance_value(Ccs), and Emitter-base_capacitance_value(Ceb).

A set of numbers is composed of 7 parameter values. If any parameter has the same value in every set of numbers, the parameter can be removed from every set of numbers, adding "*Parameter_name=Parameter_value*" following "POINTS=*Number_of_data_points*".
For example, if *Ccs* is1.2pF in every set of numbers, "CCS=1.2P" is described following "*POINTS=Number_of_data_points*". In this case, the set of numbers is composed of 6 parameter values.
Number_of_data_points is the number of sets of parameter values.
"RB=*base_resistance_value*" is optional. In default, RB=0.0.
The signs of values are as follows. In the active region of a transistor, all values are positive for NPN and *Vce*, *Vbe* and *Ic* are negative and *Ccb*, *Ccs*, and *Ceb* are positive for PNP.

Equivalent Circuit

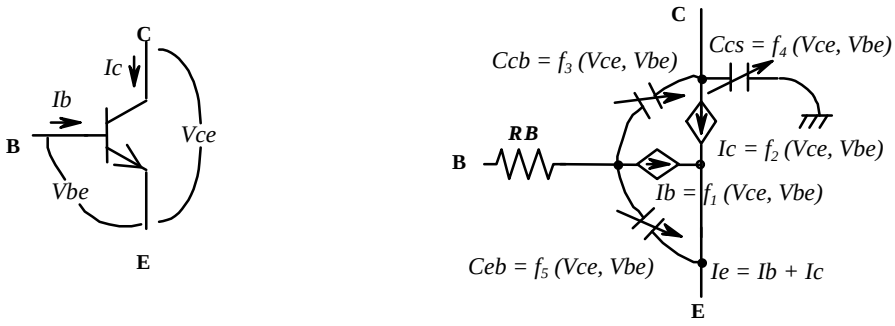


Figure 4.10 NPN Transistor Equivalent Circuit

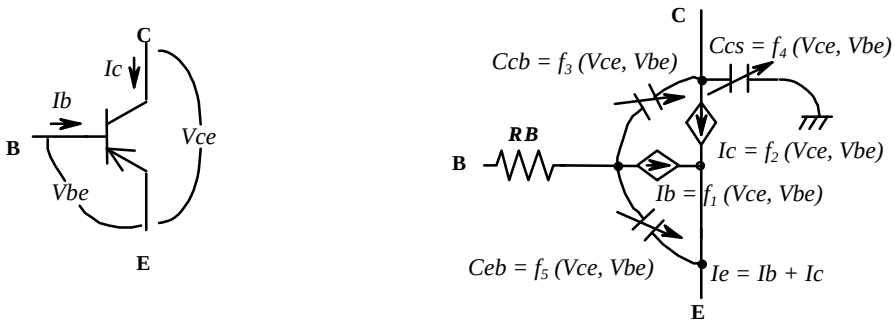


Figure 4.11 PNP Transistor Equivalent Circuit

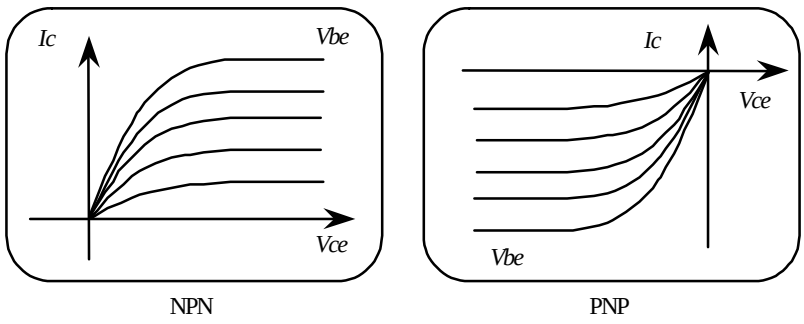


Figure 4.12 Static Characteristics of Bipolar Transistor

Example

```
[DEVICE_DEF]
[SLOW]
.MODEL MODEL1 NPN MODEL=TABLE
+ RB=10
+ POINTS=70
* Vce   Vbe    Ib     Ic       Ccb     Ccs    Ceb
+ 0.0   0.2   0.1u   0.095M   0.36P   3.8P   0.85P
+ 0.2   0.2   2.0u   0.36M    0.36P   3.8P   0.85P
+ 0.5   0.2   9.0u   0.9M     0.4P    3.8P   0.85P
+  ...
.MODEL MODEL2 NPN MODEL=TABLE
+ RB=9.4
+ POINTS=70
+ CCS=3.8P
* Vce   Vbe    Ib     Ic       Ccb     Ceb
+ 0.0   0.2   0.1U   0.095M   0.36P   0.85P
+ 0.2   0.2   2.0U   0.36P    0.36P   0.85P
+ 0.5   0.2   3.5U   0.4P     0.36P   0.85P
+  ...
[END_DEVICE_DEF]
```

(c) Example

```
[DEVICE_DEF]
[TYP]
.MODEL DIODE D MODEL=TABLE
+ RS=3.2
+ POINTS=40
*  V      I      C
+ -0.5  0.001  0.2P
+  0.0  0.095  0.2P
+  0.2  2.0    0.2P
+  0.5  3.5    0.2P
+  ...
.MODEL MODEL1 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=120
* Vgs    Vds   Vbs   Ids    Cgs    Cgd    Cgb
+ 0.0   0.095  0.2   2.0M   0.5N   0.5N   3.5N
+ 0.0   0.095  0.3   2.1M   0.7N   0.5N   4.0N
+ 0.2   2.1    0.2   2.0M   0.5N   0.5N   3.5N
```

```
+ 0.5   4.0    0.3   2.1M   0.7N   0.5N   4.0N
+  ...
+ DATA=DRAIN
+ POINTS=90
*  Vbd    Ibd   Cbd    Cbdsw
+ -2.0  0.095  0.2P   0.01P
+  0.0  0.09   0.3P   0.01P
+  0.6  4.0    0.3P   0.015P
+  ...
+ DATA=SOURCE
+ POINTS=90
+ CBS=1.2P CBSSW=0.01P
*  Vbs   Ibs
+ -2.0  0.095
+  0.0  0.09
+  0.6  4.0
+  ...
.MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=120
+ VBS=0
* Vgs    Vds   Ids    Cgs    Cgd    Cgb
+ 0.0   0.095  2.0M   0.5N   0.5N   3.5N
+ 0.0   0.095  2.1M   0.7N   0.5N   4.0N
+ 0.2   2.1    2.0M   0.5N   0.5N   3.5N
+ 0.5   4.0    2.1M   0.7N   0.5N   4.0N
+  ...
+ DATA=DRAIN
+ POINTS=90
+ CBDSW=0.01P
*  Vbd   Ibd   Cbd
+ -2.0  0.095  0.2P
+  0.0  0.09   0.3P
+  0.6  4.0    0.3P
+  ...
+ DATA=SOURCE
+ POINTS=90
+ CBS=1.2P
*  Vbs   Ibs   Cbssw
+ -2.0  0.095  0.01P
+  0.0  0.09   0.015P
```

```
+  0.6  4.0    0.02P
+  ...
[END_DEVICE_DEF]
```

(d) Data Points

Number_of_data_points is the number of sets of parameter values. It should be same as the actual number of sets of parameter values in the device model description.

If the number is different from the actual number, the smaller one is effective.

For example, if *number_of_data_points* is smaller than the actual number, *number_of_data_points* sets of parameter values should be used. if *number_of_data_points* is larger than the actual one, only whole sets of parameter values should be used.

(e) Table data structure

The Device Model is described as sets of parameters where current and capacitance are functions of terminal voltages. Terminal voltages are independent variables and current and capacitance are dependent variables. Values of each independent variable should be selected according to variations of the dependent variables considering data size and accuracy. This specification does not require that independent variables must be on regular grid. But from the simulation point of view, it is desirable that the data is on a regular grid that does not necessarily have constant pitch.

In the case where the data is on a regular grid, "GRID=YES" should appear following "POINTS=*Number_of_data_points*". In the case where the data is not on a regular grid, "GRID=NO" appears. The default is "GRID=YES".

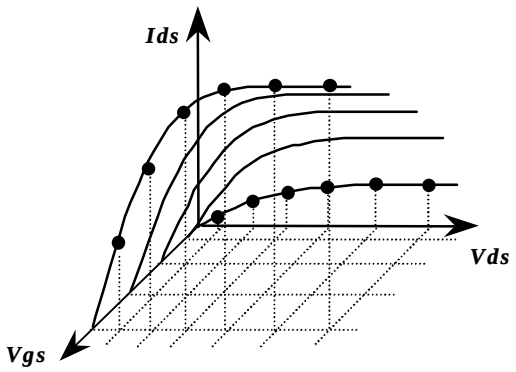


Figure 4.13 NMOS characteristics on regular grid

(f) MOS Transistor Model with Two Terminal Switch

The DC characteristics of a MOS transistor model with a two terminal switch can be considered to be the DC characteristics of *Vgs* and *Vbs* of the four terminal model for a special case. Therefore, it is considered to be the characteristic of a four terminal MOS model for the case of a fixed set of values for *Vgs* and *Vbs*. As a result, the model can be described as a one-dimensional model with only *Vds*. This table can easily represent the DC characteristics of IBIS 2.1 data.

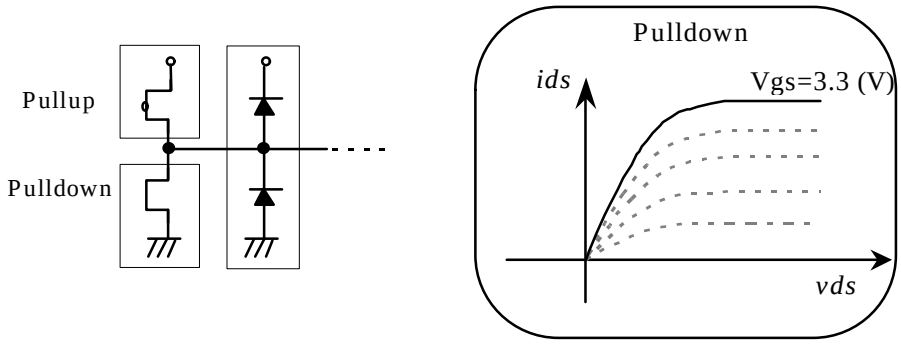


Figure 4.14 MOS Transistor Model with Two Terminal Model

Example

```
.MODEL MODEL2 NMOS MODEL=TABLE
+ L=0.8U W=10U AD=100P AS=100P PD=35U PS=35U RSH=11.5
+ DATA=CHANNEL
+ POINTS=90
+ VGS=3.3 VBS=0
*  Vds    Ids   Cgs    Cgd    Cgb
+ 0.095  2.0M   0.5N   0.5N   3.5N
+ 0.095  2.1M   0.7N   0.5N   4.0N
+ 2.1    2.0M   0.5N   0.5N   3.5N
+ 4.0    2.1M   0.7N   0.5N   4.0N
+  ...
```

(g) Dependency of L and W on Characteristics of MOS Transistor

The dependency of L and W on characteristics of a MOS transistor can be calculated by using the ratio of W/L.

The characteristics of the following MOS transistor can be calculated below.

Mxxxxxxx node1 node2 node3 node4 modelname L=*Lr* W=*Wr*

The drain current *Ids'* can be calculated by using the following equation with parameters L=*Ld*, W=*Wd* and *Ids* which are defined by .MODEL in [DEVICE_DEF], and L=*Lr* and W=*Wr* of the transistor descriptions which are defined by [CONNECTION].

$Ids' = Ids * (Wr / Wd) * (Ld / Lr)$

The gate-source capacitance *Cgs'*, the gate-drain capacitance *Cgd'* and the gate-bulk capacitance *Cgb'* can be calculated by using the following equation.

$Cgs' = Cgs * (Wr / Wd) * (Ld / Lr)$

$Cgd' = Cgd * (Wr / Wd) * (Ld / Lr)$

$Cgb' = Cgb * (Wr / Wd) * (Ld / Lr)$

(h) Dependency of AD and AS on Junction Diode Characteristics of MOS Transistor

The dependency of AD and AS on the characteristics of junction diodes in a MOS transistor can be calculated by using the ratio of AD or AS described in the circuit description, and that described in the device model.

The characteristics of the following MOS transistor can be calculated as shown below.

Mxxxxxxx node1 node2 node3 node4 modelname L=*Lr* W=*Wr* AD=*Adr* AS=*ASr* +PD=*PDr* PS=*PSr*

The bulk-drain diode current value *Ibd'* can be calculated by using the following equation with the parameters AD=*ADd* and *Ibd* which are defined by .MODEL in [DEVICE_DEF], and AD=*ADr* of the transistor descriptions which are defined by [CONNECTION].

$$Ibd' = Ibd * (ADr / ADd)$$

The bulk-source diode current value *Ibs'* can be calculated by using the following equation with the parameters AS=*ASd* and *Ibs* which are defined by .MODEL in [DEVICE_DEF], and AS=*ASr* of the transistor descriptions which are defined by [CONNECTION].

$$Ibs' = Ibs * (ASr / ASd)$$

The bulk-source diode capacitance *Cbs'* can be calculated by using the following equation with the parameters AS=*ASd*, PS=*PSd*, *Cbs* and *Cbssw* which are defined by .MODEL in [DEVICE_DEF], and AS=*ASr* and PS=*PSr* of the transistor descriptions which are defined by [CONNECTION].

$$Cbs' = Cbs * (ASr / ASd) + Cbssw * (PSr / PSd)$$

The bulk-source diode capacitance *Cbd'* can be calculated by using the following equation with the parameters AD=*ADd*, PD=*PDd*, *Cbd* and *Cbdsw* which are defined by .MODEL in [DEVICE_DEF], and AD=*ADr* and PD=*PDr* of the transistor descriptions which are defined by [CONNECTION].

$$Cbd' = Cbd * (ADr / ADd) + Cbdsw * (PDr / PDd)$$

(i) Junction Resistance of MOS Transistor

The junction resistance of MOS transistor of the following MOS transistor can be calculated as shown below.

Mxxxxxxx node1 node2 node3 node4 modelname L=*Lr* W=*Wr*
+ NRD= *NRD* NRS= *NRS*

RD, RS can be calculated by using the following equation with the parameters RSH=RSH which is defined by .MODEL in [DEVICE_DEF], and NRD=*NRD* and NRS=*NRS* of the transistor descriptions which are defined by [CONNECTION].

$$RD = NRD * RSH$$

$$RS = NRS * RSH$$

(j) Notes

The device characteristics defined by [FAST], [TYP], and [SLOW] correspond to those of the input stimulus.

Thus, a simulation for [TYP] stimulus should use the corresponding [TYP] nonlinear characteristics of the device.

4.2.9 Package Model Reference

(a) Description

```
[COMPONENT]
```

(b) Explanation

This assigns the file name and type of the package model by reference.

Parameters should be described after the keyword [COMPONENT].

This keyword has three parameters on one line: package file name, package type name, and model name to be used.

The assigned package type and model name should be described at the header of the package model.

(c) Example

```
[COMPONENT]
*FILE_NAME    PKG_NAME    MODEL_NAME
PACKAGEA.PKG  PACKAGE1    MODEL1
```

4.3 Package Model File

4.3.1 File name

The name of the model file should start with any alphabetical or numerical characters, with .PKG as an extension.

There is no limit on the number of characters in a file name.

(a) Example

```
TSSOP48.PKG
```

(b) Notes

For DOS, more than 9 characters other than extension will be ignored.

4.3.2 Start and End of Model Description

One Model description should be provided per package model.

(1) Start of package model description

(a) Description

[PACKAGE]

(b) Explanation

The contents of the model follow this keyword.

(2) End of package model description

(a) Description

[END_PACKAGE]

(b) Explanation

The description of the package model will be terminated by this keyword.

4.3.3 Header

(1) Package type

(a) Description

[NAME] Characters

(b) Explanation

Package type (Product Number/Name)

(c) Example

```
[NAME] TSSOP48
```

(2) Model version

(a) Description

[IMIC_VER] Characters

(b) Explanation

IMIC version

(c) Example

```
[IMIC_VER]  1.3
```

(3) Model level

(a) Description

`[LEVEL]` Integer

(b) Explanation

Level 1: SI (Signal Integrity) model for the analysis of signal noise.

Level 2: PI (Power Integrity) model for the analysis of power noise including signal noise.

Level 3: EMI (Electromagnetic Interference) model for the analysis of radiated emission noise.

(c) Example

```
[LEVEL]  2
```

(4) Model index

(a) Description

```
[MODEL_INDEX]
```

(b) Explanation

Package models should be listed here. After [MODEL_INDEX], package model name, upper frequency limit, and chip size in a line. Several lines of [MODEL_INDEX] entries are allowed. Frequency and chip size will be used to indicate the validity of the model for a particular application or analysis. These two parameters are optional, either may be "NA".

(c) Example

```
[MODEL_INDEX]
  * MODELNAME      FREQUENCY   CHIPSIZE
    MODEL1           50MHZ       10MM2
    MODEL2           200MHZ      10MM2
    ...
```

(5) Date

(a) Description

`[DATE]` Characters

(b) Explanation

The model release date is described using any of the following formats.

· Month / Day / Year Example : 3/3/98
· Day / Month / Year Example : 3MAR98
· Month Day, Year Example : MARCH 3, 1998

(c) Example

```
[DATE]  3/3/98
```

(6) Explanation of model

(a) Description

`[NOTES]` Characters

(b) Explanation

Any comments may appear in the lines following the keyword `[NOTES]`.

The distance from surface of PCB to reference ground should be described. 0.0mm, 0.152mm and 1.588mm are recommended as the distance.

(c) Example

```
[NOTES]
  TSOP 3 PIN PACKAGE ELECTRICAL CHARCTERISTICS MODEL
  FOR ALVCH LCR3_SELF MODEL EXCLUDE MUTUAL ELEMENTS
  HEIGHT TO REFERENCE GROUND IS 0.152mm.
```

(7) Copyright

(a) Description

`[COPYRIGHT]` Characters

(b) Explanation

Copyright holder and related terms are stated.

(c) Example

```
[COPYRIGHT] COPYRIGHT 1998, ZYX CORP., ALL RIGHTS RESERVED
```

(8) Manufacture

(a) Description

`[MANUFACTURER]` Characters

(b) Explanation

The package manufacturer is declared here.

(c) Example

```
[MANUFACTURER]   ZYX CORP.
```

4.3.4 Model Name

(a) Description

`[MODEL_NAME]` Characters

(b) Explanation

This defines the model name which is used at `[MODEL_INDEX]` and used at `[COMPONENT]` of the IC model file.

(c) Example

```
[MODEL_NAME]  MODEL1
```

4.3.5 Terminals

(1) Inner Terminals

This defines the connections between the inner terminals and the inner circuits of package.

(a) Description

```
[INNER_TERMINAL]
```

(b) Explanation

This defines the connections between the inner terminals and the inner circuits of package.

Each line should have only one inner terminal reference. The first parameter is inner terminal name and the second parameter is connected signal name of the internal circuit of the package.

(c) Example

```
[INNER_TERMINAL]
  LEAD1    NODE1
  LEAD2    NODE2
  ....
```

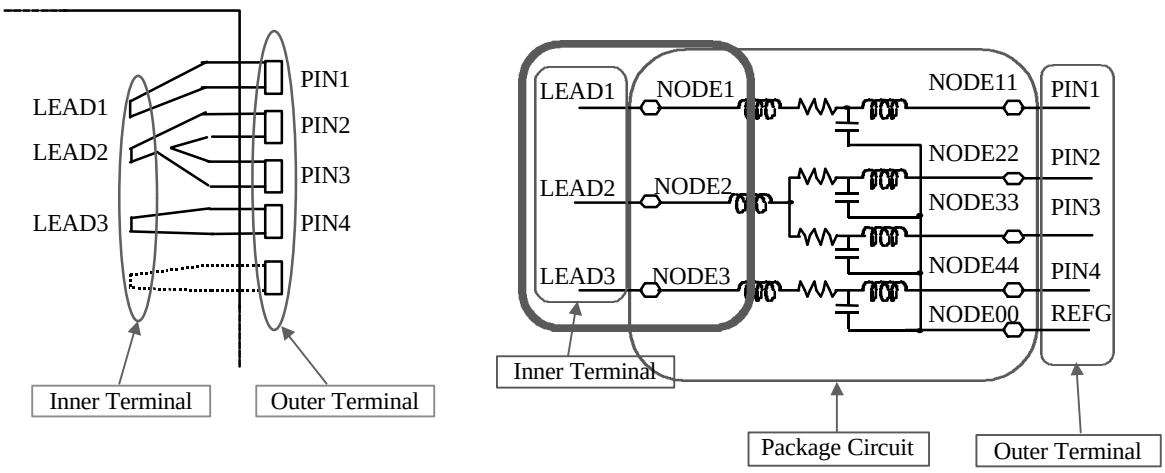


Figure 4.15 Relationship between inner terminals and internal circuit of package

(2) Outer Terminals

This defines the connections between the outer terminals and the inner circuits of package.

(a) Description

```
[OUTER_TERMINAL]
```

(b) Explanation

This defines the connections between the outer terminals and the inner circuits of the package, and the relationship between reference ground and the internal circuit of the package. Each line should have only one outer terminal reference. The first parameter is outer terminal name and the second parameter is the signal name of the internal circuit of the package, to which the outer terminal is connected.

The name of the reference ground terminal is "REFG". The reference ground is defined as a reference plane when electrical parameters of packages are measured and/or simulated. Simulation assumes this reference ground terminal to be connected to the reference ground plane of printed circuit board.

(c) Example

```
[OUTER_TERMINAL]
  PIN1  NODE11
  PIN2  NODE22
     ...
  REFG  NODE00
```

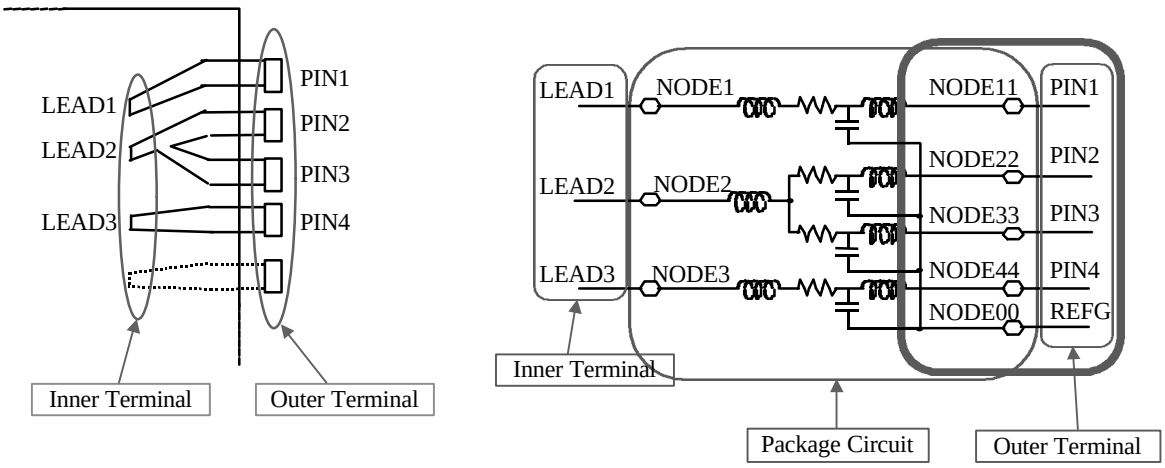


Figure 4.16 Relationship between outer terminals and internal circuit of package

4.3.6 Circuit description

This describes the elements of internal circuits and their interconnections.

(a) Description

```
[CONNECTION]
[FAST]
[TYP]
[SLOW]
[END_CONNECTION]
```

(b) Explanation

This defines the internal circuits of the package and bonding wire connections.

The format of the circuit description of the package follows the format of the IC model file.

(c) Notes

The size of the package description may be huge due to coupling etc.

If the package has symmetrical structures, the size of the model can be drastically reduced by defining the subcircuit for one portion, and then reference that subcircuit in the other portions. For example, a one-fourth model of the package or a hierarchical subcircuit of the package may reduce the size of model.

(d) Example

Example for a one-fourth model is as follows.

```
[CONNECTION]
  .SUBCKT PKG IN1 IN2 IN3 IN4 IN5 IN6 IN7 IN8 IN9 IN10 IN11
  + IN12
  + OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9 OUT10
  + OUT11 OUT12
  + IN24 IN23 IN22 IN21 IN20 IN19 IN18 IN17 IN16 IN15 IN14
  + IN13
  + OUT24 OUT23 OUT22 OUT21 OUT20 OUT19 OUT18 OUT17
  + OUT16 OUT15 OUT14 OUT13
```

```
+ IN25 IN26 IN27 IN28 IN29 IN30 IN31 IN32 IN33 IN34 IN35
+ IN36
+ OUT25 OUT26 OUT27 OUT28 OUT29 OUT30 OUT31 OUT32
+ OUT33 OUT34 OUT35 OUT36
+ IN48 IN47 IN46 IN45 IN44 IN43 IN42 IN41 IN40 IN39 IN38
+ IN37
+ OUT48 OUT47 OUT46 OUT45 OUT44 OUT43 OUT42 OUT41
+ OUT40 OUT39 OUT38 OUT37
+ REFG
XPKG_01
+ IN1 IN2 IN3 IN4 IN5 IN6 IN7 IN8 IN9 IN10 IN11 IN12
+ OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8 OUT9 OUT10
+ OUT11 OUT12  REFG  LCR
XPKG_02
+ IN24 IN23 IN22 IN21 IN20 IN19 IN18 IN17 IN16 IN15 IN14 IN13
+ OUT24 OUT23 OUT22 OUT21 OUT20 OUT19 OUT18 OUT17
+ OUT16 OUT15 OUT14 OUT13 REFG  LCR
XPKG_03
+ IN25 IN26 IN27 IN28 IN29 IN30 IN31 IN32 IN33 IN34 IN35 IN36
+ OUT25 OUT26 OUT27 OUT28 OUT29 OUT30 OUT31 OUT32
+ OUT33 OUT34 OUT35 OUT36 REFG  LCR
XPKG_04
+ IN48 IN47 IN46 IN45 IN44 IN43 IN42 IN41 IN40 IN39 IN38 IN37
+ OUT48 OUT47 OUT46 OUT45 OUT44 OUT43 OUT42 OUT41
+ OUT40 OUT39 OUT38 OUT37 REFG  LCR
.ENDS PKG
.SUBCKT LCR
+ 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
+ 23 24 25
C000 26 25 3.08467E-13
C001 27 25 1.54055E-13
C002 28 25 1.18045E-13
C003 29 25 1.04291E-13
C004 30 25 1.0002E-13
C005 31 25 9.81234E-14
C006 32 25 9.24553E-14
C007 33 25 9.26352E-14
 .......
 ......
R00m 36 61 0.000624821
L00b 12 50 5.1212E-10
L00n 24 62 5.1212E-10
```

```
R00b 37 50 0.000643131
R00n 37 62 0.000643131
.ENDS LCR
```

4.3.7 Device Model

This describes the characteristics of nonlinear devices. Variables are one-, two-, and three-dimensional data. Nonlinear devices are transistor, diode, voltage dependent capacitor and so on.

(a) Description

```
[DEVICE_DEF]
[FAST]
[TYP]
[SLOW]
[END_DEVICE_DEF]
```

(b) Explanation

This defines a device model to be used in the definition of the package.

The definition of device model should be terminated with `[END_DEVICE_DEF]`.

The format of the circuit description of the package follows the format of the IC model file.

4.3.8 Structures

The materials, positions, 3D-structures etc. of the package will be described.

This is a pending item in this standard.

4.4 Module Model File

4.4.1 File name

The name of the model file should start with any alphabetical or numerical characters, with .MDL as an extension.

There is no limit on the number of characters in the file.

(a) Example

DIMM32MB.MDL

(b) Notes

For DOS, more than 9 characters other than extension will be ignored.

4.4.2 Start and End of Model Description

One Model description should be provided per module model.

(1) Start of module model description

(a) Description

```
[MODULE]
```

(b) Explanation

The contents of the model follow this keyword.

(2) End of module model description

(a) Description

```
[END_MODULE]
```

(b) Explanation

The description of the module model will be terminated with this description.

4.4.3 Header

(1) Module type

(a) Description

[NAME] Characters

(b) Explanation

Module type identifier (Product Number/Name). This is used by simulators to locate the correct model for a module in a design.

(c) Example

```
[NAME] DIMM32MB
```

(2) Model version

(a) Description

[IMIC_VER] Characters

(b) Explanation

The IMIC specification version that the file conforms to. Currently only version 1.3 is supported. Parsers must follow appropriate syntax rules for the entire module model.

(c) Example

```
[IMIC_VER] 1.3
```

(3) Model level

(a) Description

[LEVEL] Integer

(b) Explanation

Level 1: SI (Signal Integrity) model for the analysis of signal noise.

Level 2: PI (Power Integrity) model for the analysis of power noise including signal noise.

Level 3: EMI (Electromagnetic Interference) model for the analysis of radiated emission noise.

(c) Example

```
[LEVEL] 2
```

(4) Date

(a) Description

[DATE] Characters

(b) Explanation

The model release date is described using any of the following formats.

· Month / Day / Year Example : 3/23/98

· Day / Month / Year Example : 23MAR98

· Month Day, Year Example : MARCH 23, 1998

(c) Example

```
[DATE] 3/23/98
```

(5) Explanation of model

(a) Description

[NOTES]

Arbitrary notes concerning the model. This may be used for explanations of the origin, usage, and testing of the model, for example.

(b) Explanation

Any comments may appear on the lines following the keyword [NOTES].

(c) Example

[NOTES]

MEMORY MODULE MODEL FOR 3.3V EDO x72 32MB DIMM

(6) Copyright

(a) Description

`[COPYRIGHT]` Characters

(b) Explanation

Copyright holder and related terms are stated.

(c) Example

```
[COPYRIGHT] COPYRIGHT 1998, ZYX CORP., ALL RIGHTS RESERVED
```

(7) Manufacture

(a) Description

`[MANUFACTURER]` Characters

(b) Explanation

Manufacture is declared here.

(c) Example

```
[MANUFACTURER]   ZYX CORP.
```

4.4.4 Terminals

This defines the outer terminals of the module. The outer terminals of the module are it's pins.

(a) Description

`[TERMINAL]`

(b) Explanation

This defines the external terminals of module. Description should be started with next line of keyword `[TERMINAL]`.

The signal names of the external terminals of module should be described. The keyword ".SUBCKT" is followed by the name of the module and the signal names of external terminals.

Continuous line starts with "+" in the first column.

(c) Example

```
[TERMINAL]
  .SUBCKT  DIMM32MB SIG1 SIG2 SIG3 SIG4 SIG5 SIG6 SIG7 REFG
```

4.4.5 Circuit description

This describes the elements of the internal circuit and their interconnections.

The elements are ICs, modules and other elements including elements for interconnections on the module.

(a) Description

```
[CONNECTION]
[FAST]
[TYP]
[SLOW]
```

```
[END_CONNECTION]
```

(b) Explanation

This defines the elements of the internal circuits and their interconnections.

The format of the circuit description of module follows format of the IC model file.

(c) Example

```
[CONNECTION]
[TYP]
  .SUBCKT  MODULE_TOP OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7
  XLSI-A LAA LAB LAC LAD LAE LAF ... LSI-A
  XLSI-B LBA LBB LBC LBD LBE LBF ... LSI-B
  XLSI-C LCA LCB LCC LCD LCE LCF ... LSI-C
  XMODULE-A MAA MAB MAC MAD MAE MAF MAG MODULE-A
  T1 LAA OUT1 Z0=2.3
  T2 MAC OUT2 Z0=5.3
  T3 LBA OUT3 Z0=1.3
  T4 LBF OUT7 Z0=3.1
  T5 LBF OUT7 Z0=2.1
  ...
  [END_CONNECTION]
```

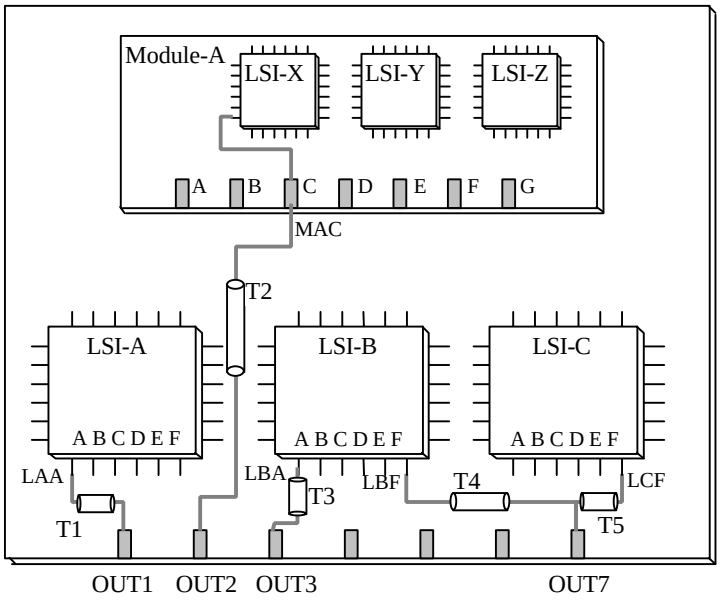


Figure 4.17 Example of module circuit

4.4.6 Signal Source

This keyword is used to define the output pins of internal IC's or modules from which signal source stimuli are described to generate the desired waveforms at the output pins of the module.

(a) Description

`[SIGNAL_SOURCE]` Output terminal name

`[SOURCE_DEF]`

(b) Explanation

This defines signal source stimuli of the internal IC's or modules that generate waveforms that will appear at the output terminals of the module. The output terminal names of the module defined next to [SIGNAL_SOURCE] must match the corresponding signal names defined as the external terminals of the module in the [TERMINAL] .SUBCKT statement..

The [SIGNAL_SOURCE] section contains one [SOURCE_DEF] subsection, specifying the internal IC's or modules and the terminals from which the signal source stimuli is desired.

[SOURCE_DEF]

The first parameter is a reference name for the internal IC or module that provides the desired signal source stimulus. This reference name should be defined in the [CONNECTION] section.

The second parameter is the external terminal name of the IC or module defined by the first parameter through which the desired signal source stimuli is output from. The external terminal name should match one of the external terminals defined in the [CONNECTION]section.

These two parameters should be described on one line.

(c) Example

```
[SIGNAL_SOURCE] OUT1
[SOURCE_DEF]
XLSI-A    LAA
[SIGNAL_SOURCE] OUT2
[SOURCE_DEF]
XMODULE-A  MAC
[SIGNAL_SOURCE] OUT3
[SOURCE_DEF]
XLSI-B    LBA
[SIGNAL_SOURCE] OUT7
[SOURCE_DEF]
XLSI-B    LBF
XLSI-C    LCF
```

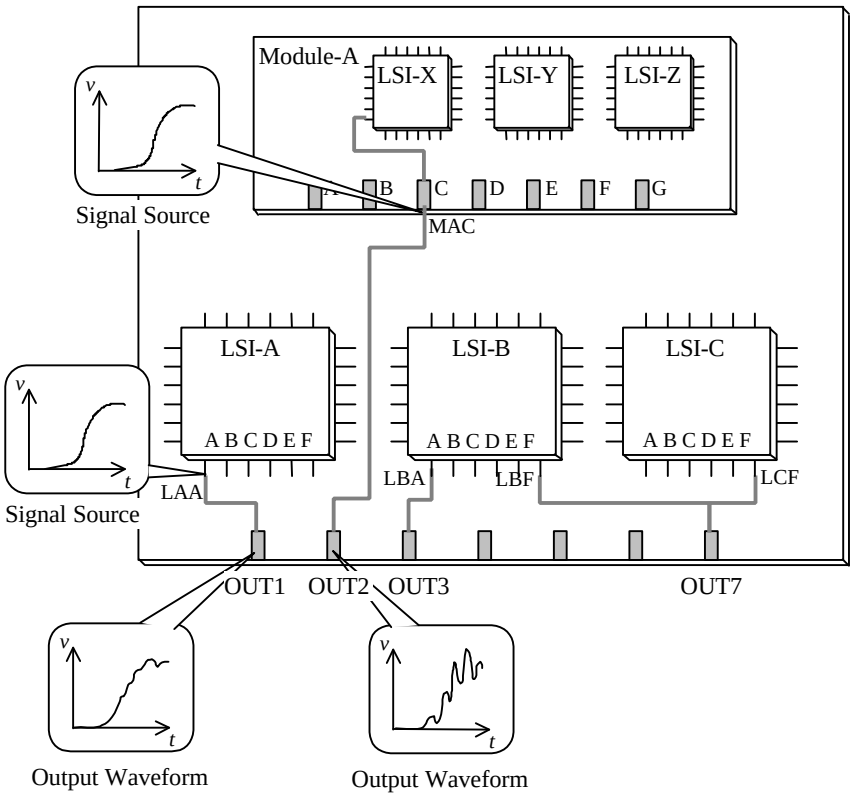


Figure 4.18 Example of signal source of module

The signal source for output terminal "OUT1" of the module is terminal "LAA" of "LSI-A".

The signal source for output terminal "OUT2" of the module is terminal "MAC" of "MODULE-A".

4.4.7 Device Model

This describes the characteristics of nonlinear devices. Variables are one-, two-, and three-dimensional data. Nonlinear devices are transistor, diode, voltage dependent capacitor and so on.

(a) Description

```
[DEVICE_DEF]
[FAST]
[TYP]
[SLOW]
[END_DEVICE_DEF]
```

(b) Explanation

This defines the device models to be used in the definition of the module.

The definition of the device model should be terminated with `[END_DEVICE_DEF]`.

The format of the circuit description of the module board must follow the same format as the IC model file.

4.4.8 Module Model Reference

This describes the relationships between the ICs and the module.

(a) Description

```
[COMPONENT]
```

(b) Explanation

This describes file and type names of the IC models to be referenced. It also describes the file and type names of the module models to be referenced.

Parameters should be described after the keyword [COMPONENT].

The first parameter is the file name of the IC model or module model. The second parameter is the model type of the IC model or module model.

These type names should be described at the header of the IC or module file.

All parameters should be described on one line.

The assigned IC type name and module type name should be described at the header of IC model file and module model file, respectively.

(c) Example

```
[COMPONENT]
  *FILE_NAME       IC_NAME
  ALVCH16244.IMC   ALVCH16244
  DRAM16MX16.MDL   DRAM16MX16
```

4.4.9 Structures

The materials, positions, 3D-structures etc. of package will be described.

This is pending item in this standard.

5. Level of Models

The level of the models are set according to the purpose of the simulation. The purpose of simulation and the elements of model which are correspondent to level of models are described in **Table 5.1** and **Table 5.2** respectivety.

Table 5.1 Level of Models

Level	Object	Simulation
1	Signal Integrity (SI)	To analyze signal waveform. - Light load to simulator
2	Power Integrity (PI)	To analyze power/ground bounce and EM emission from boards. - Large size of circuits containing many parasitic LCRs - Heavy load to simulator
3	EMI	To analyze EM emissions from the package itself. (Future Problem)

Table 5.2 Required Elements of Model for Each Level

File	Item	1	2	3
IC Model	Header	Yes	Yes	Yes
	External Terminal	Yes	Yes	Yes
	Pad Assignment	Yes	Yes	Yes
	Circuit Description Signal	Yes	Yes	Yes
	Power	No	Yes	Yes
	Input Stimulus Assignment	Yes	Yes	Yes
	Input Stimulus	Yes	Yes	Yes
	Device Model	Yes	Yes	Yes
	Package Model Reference	Yes	Yes	Yes
Package Model	Header	Yes	Yes	Yes
	Model Name	Yes	Yes	Yes
	Inner Terminals	Yes	Yes	Yes
	Outer Terminals	Yes	Yes	Yes
	Circuit Description	Yes	Yes	Yes
	Device Model	No	Yes	Yes
	Structures	No	No	Yes
Module Model	Header	Yes	Yes	Yes
	External Terminals	Yes	Yes	Yes
	Circuit Description	Yes	Yes	Yes
	Signal Source	Yes	Yes	Yes
	Device Model	Yes	Yes	Yes
	IC/Module Reference	Yes	Yes	Yes
	Structures	No	No	Yes

6 Model Delivery Flow

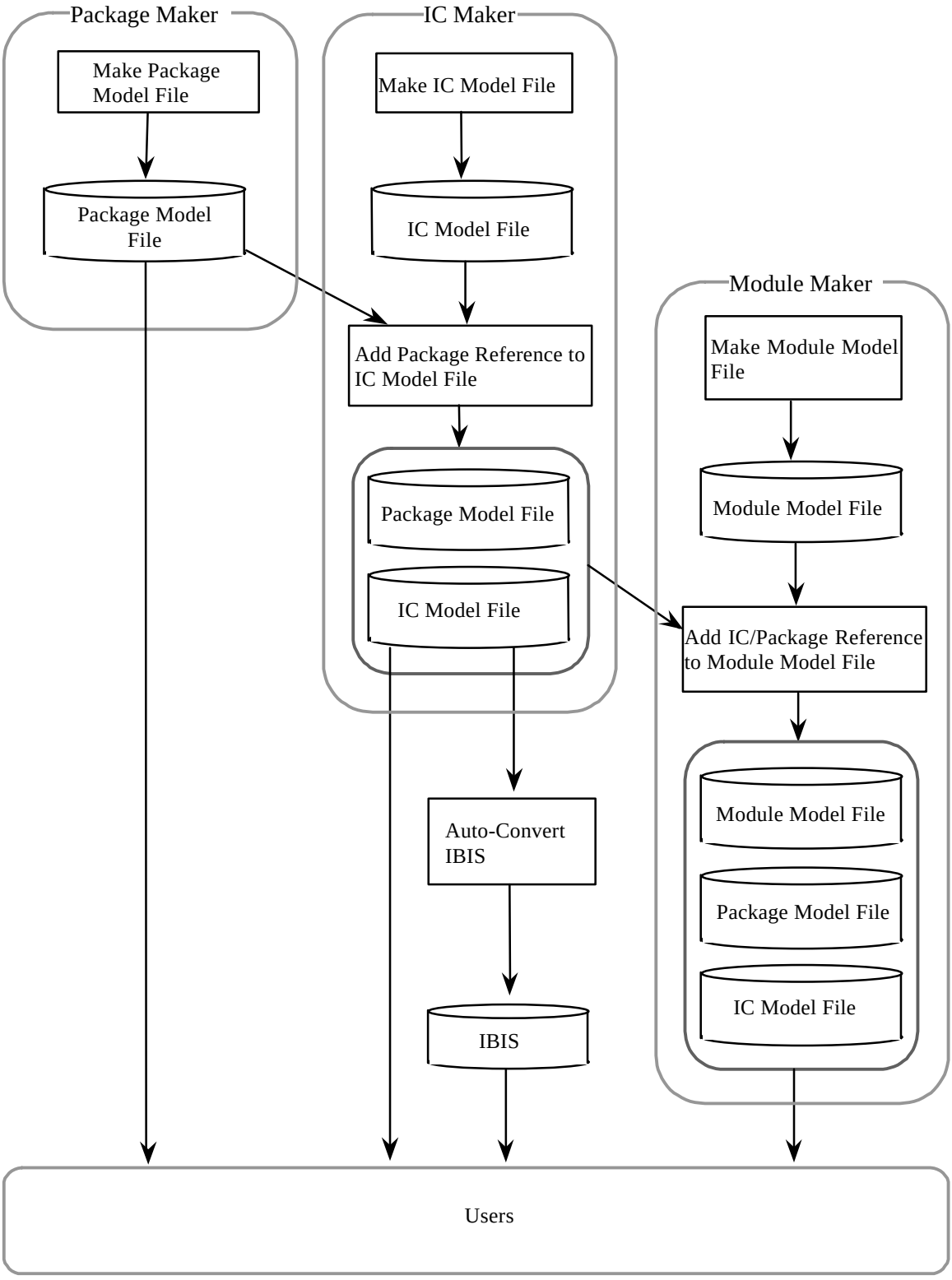


Figure 6.1 Delivery Flow of MODEL Files

7. Example

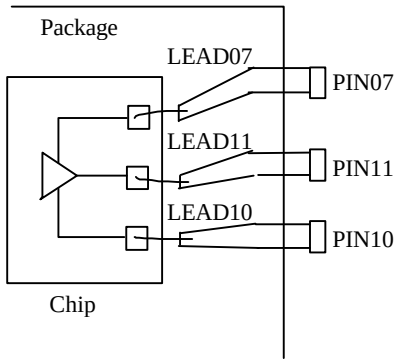


Figure 7.1 IC Structure

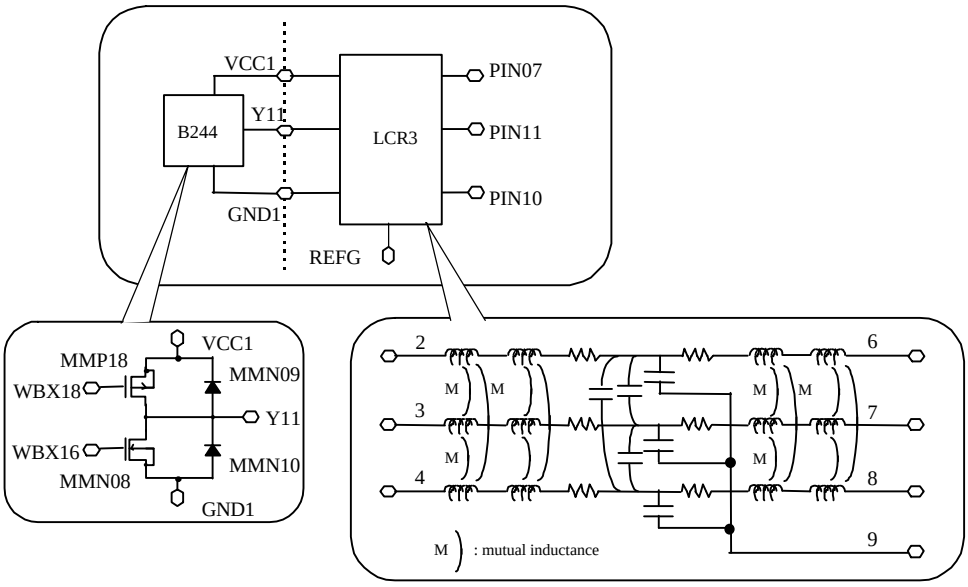


Figure 7.2 Equivalent Circuit

```
[IC]
[NAME] ALVCH16244
[IMIC_VER] 1.3
[LEVEL] 2
[DATE] AUGUST 18, 1999
[NOTES]
ELECTRICAL MODEL FOR ALVCH16244
-- 3 PIN MODEL --
[COPYRIGHT] COPYRIGHT 1999, ABC, LTD., ALL RIGHTS RESERVED.
[MANUFACTURER] ABC, LTD.

[TERMINAL]
.SUBCKT ALVCH16244 PIN11 PIN07 PIN10 REFG
```

```
[PAD_ASSIGNMENT]
XXB2442 GND1  VCC1  Y11 B244
XLCR3   VCC1  Y11 GND1  LEAD07 LEAD11  LEAD10 REFG LCR3

[CONNECTION]
.SUBCKT B244  GND1  VCC1  Y11
MMN08   Y11  WBX16  GND1  GND1  NMOS1  L=4.0E-07  W=4.0E-04
+ AD=6.596E-10 AS=6.596E-10
MMN09   VCC1 GND1   Y11   GND1  NMOS2  L=1.1E-06  W=2.0E-04
+ AD=3.296E-10 AS=3.296E-10
MMN10   Y11  GND1   GND1  GND1  NMOS2  L=1.1E-06  W=2.0E-04
+ AD=3.296E-10 AS=3.296E-10
MMP08   Y11  WBX18  VCC1  VCC1  PMOS1  L=4.0E-07  W=7.0E-04
+ AD=1.154E-9  AS=1.154E-9
.ENDS B244

[STIMULUS_ASSIGNMENT]
[TERMINAL]  LEAD11
[RISING]
XXB2442   RISING
[FALLING]
XXB2442   FALLING
[END_STIMULUS_ASSIGNMENT]

[STIMULUS]  RISING
[WAVE_DEF]
*** RISING WAVEFORM ***
VWBX16 WBX16 0 PWL
+  2.40E-11    3.30E+00    1.04E-10    3.34E+00    1.44E-10   3.38E+00
+  1.84E-10    3.36E+00    2.19E-10    3.20E+00    2.59E-10   2.78E+00
+  2.99E-10    2.12E+00    3.39E-10    1.38E+00    3.74E-10   7.47E-01
+  4.00E-10    3.69E-01    4.10E-10    2.90E-01    4.30E-10   1.65E-01
+  4.70E-10    5.12E-02    5.90E-10    3.90E-03
VWBX18 WBX18 0 PWL
+  2.40E-11    3.30E+00    1.04E-10    3.32E+00    1.44E-10   3.34E+00
+  1.84E-10    3.23E+00    1.99E-10    3.12E+00    2.19E-10   2.90E+00
+  2.59E-10    2.28E+00    2.99E-10    1.51E+00    3.39E-10   8.45E-01
+  3.74E-10    5.02E-01    4.00E-10    3.54E-01    4.70E-10   2.56E-01
+  5.50E-10    1.22E-01    6.30E-10    3.90E-02    7.10E-10   1.08E-02
+  8.30E-10    1.43E-03

[STIMULUS] FALLING
[WAVE_DEF]
```

```
*** FALLING WAVEFORM ***
VWBX16 WBX16 0 PWL
+  2.40E-11    3.33E-04    1.84E-10   -1.44E-02    2.24E-10  -3.35E-02
+  2.64E-10   -2.87E-03    3.04E-10    2.26E-01    3.44E-10   8.20E-01
+  3.84E-10    1.52E+00    4.10E-10    1.93E+00    4.70E-10   2.56E+00
+  5.10E-10    2.79E+00    5.50E-10    2.91E+00    5.85E-10   2.94E+00
+  6.65E-10    3.10E+00    7.45E-10    3.21E+00    8.25E-10   3.26E+00
+  9.05E-10    3.28E+00    1.03E-09    3.30E+00
VWBX18 WBX18 0 PWL
+  2.40E-11    5.76E-04    1.04E-10   -1.13E-03    1.44E-10  -8.22E-03
+  2.24E-10   -4.61E-02    2.64E-10   -4.95E-02    3.04E-10   2.98E-02
+  3.44E-10    2.80E-01    3.84E-10    6.90E-01    4.30E-10   1.18E+00
+  4.70E-10    1.57E+00    5.10E-10    2.01E+00    5.50E-10   2.36E+00
+  5.85E-10    2.59E+00    6.25E-10    2.88E+00    6.65E-10   3.07E+00
+  7.05E-10    3.18E+00    7.45E-10    3.24E+00    8.65E-10   3.29E+00
+  9.05E-10    3.30E+00

[DEVICE_DEF]
[TYP]
.MODEL NMOS1 NMOS MODEL=TABLE
+ W=4E-04 L=4E-07  AD=6.596E-10 AS=6.596E-10
+ DATA=CHANNEL POINTS=77 VBS=0.0
*       vgs         vds         ids         cgs         cgd         cbg
+        0.          0.          0.    48.4359f    48.4359f  182.1262f
+        0.   600.0000m     2.5255p    48.4359f    48.4359f  182.1262f
+        0.      1.2000     3.3274p    48.4359f    48.4359f  182.1262f
+        0.      1.8000     4.3064p    48.4359f    48.4359f  182.1262f
+        0.      2.4000     5.2853p    48.4359f    48.4359f  182.1262f
+        0.      3.0000     7.1084p    48.4359f    48.4359f  182.1262f
+        0.      3.6000     8.9314p    48.4359f    48.4359f  182.1262f
+        0.      4.2000    11.7951p    48.4359f    48.4359f  182.1262f
+        0.      4.8000    15.6992p    48.4359f    48.4359f  182.1262f
+        0.      5.4000    19.6034p    48.4359f    48.4359f  182.1262f
+        0.      6.0000    23.5076p    48.4359f    48.4359f  182.1262f
+    1.0000          0.          0.   306.7689f   306.7689f         0.
+    1.0000   600.0000m     6.9168m   406.9793f    97.2344f   17.3145f
+    1.0000      1.2000     7.3735m   406.9793f    97.2344f   17.3145f
+    1.0000      1.8000     7.8424m   406.9793f    97.2344f   17.3145f
+    1.0000      2.4000     8.3113m   406.9793f    97.2344f   17.3145f
+    1.0000      3.0000     8.8155m   406.9793f    97.2344f   17.3145f
+    1.0000      3.6000     9.3196m   406.9793f    97.2344f   17.3145f
+    1.0000      4.2000     9.8452m   406.9793f    97.2344f   17.3145f
```

+	1.0000	4.8000	10.3922m	406.9793f	97.2344f	17.3145f
+	1.0000	5.4000	10.9392m	406.9793f	97.2344f	17.3145f
+	1.0000	6.0000	11.4862m	406.9793f	97.2344f	17.3145f
+	2.0000	0.	0.	306.7689f	306.7689f	0.
+	2.0000	600.0000m	48.9323m	368.6421f	220.8863f	4.6129f
+	2.0000	1.2000	64.5467m	407.1945f	146.6903f	9.9828f
+	2.0000	1.8000	66.1404m	413.5093f	121.9623f	12.3870f
+	2.0000	2.4000	67.7341m	419.8241f	97.2344f	14.7912f
+	2.0000	3.0000	68.9781m	419.8241f	97.2344f	14.7912f
+	2.0000	3.6000	70.2221m	419.8241f	97.2344f	14.7912f
+	2.0000	4.2000	71.4912m	419.8241f	97.2344f	14.7912f
+	2.0000	4.8000	72.7855m	419.8241f	97.2344f	14.7912f
+	2.0000	5.4000	74.0798m	419.8241f	97.2344f	14.7912f
+	2.0000	6.0000	75.3741m	419.8241f	97.2344f	14.7912f
+	3.0000	0.	0.	306.7689f	306.7689f	0.
+	3.0000	600.0000m	75.0979m	339.2527f	274.2098f	9.040e-16
+	3.0000	1.2000	110.9732m	370.4822f	222.3031f	4.1922f
+	3.0000	1.8000	123.6722m	396.1512f	159.7688f	9.2062f
+	3.0000	2.4000	136.3713m	421.8201f	97.2344f	14.2202f
+	3.0000	3.0000	138.2381m	421.8201f	97.2344f	14.2202f
+	3.0000	3.6000	140.1050m	421.8201f	97.2344f	14.2202f
+	3.0000	4.2000	142.0038m	421.8201f	97.2344f	14.2202f
+	3.0000	4.8000	143.9346m	421.8201f	97.2344f	14.2202f
+	3.0000	5.4000	145.8655m	421.8201f	97.2344f	14.2202f
+	3.0000	6.0000	147.7963m	421.8201f	97.2344f	14.2202f
+	4.0000	0.	0.	306.7689f	306.7689f	0.
+	4.0000	600.0000m	90.1565m	328.1374f	287.2049f	3.680e-16
+	4.0000	1.2000	143.9367m	354.8098f	246.1390f	2.7429f
+	4.0000	1.8000	174.8287m	384.4827f	187.4158f	6.8692f
+	4.0000	2.4000	205.7208m	414.1555f	128.6925f	10.9954f
+	4.0000	3.0000	208.3092m	417.4761f	116.1093f	12.1873f
+	4.0000	3.6000	210.8976m	420.7966f	103.5260f	13.3793f
+	4.0000	4.2000	213.4668m	422.4569f	97.2344f	13.9752f
+	4.0000	4.8000	216.0167m	422.4569f	97.2344f	13.9752f
+	4.0000	5.4000	218.5665m	422.4569f	97.2344f	13.9752f
+	4.0000	6.0000	221.1164m	422.4569f	97.2344f	13.9752f
+	5.0000	0.	0.	306.7689f	306.7689f	0.
+	5.0000	600.0000m	99.9432m	322.5663f	292.9103f	1.973e-16
+	5.0000	1.2000	167.6002m	342.4359f	268.7011f	1.2365f
+	5.0000	1.8000	214.5414m	364.9538f	236.3058f	2.9843f
+	5.0000	2.4000	261.4827m	387.4716f	203.9105f	4.7322f
+	5.0000	3.0000	269.9993m	401.5748f	161.2401f	8.3754f

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+    5.0000      3.6000   278.5159m   415.6779f   118.5696f   12.0186f
+    5.0000      4.2000   284.3532m   422.7295f    97.2344f   13.8402f
+    5.0000      4.8000   287.5112m   422.7295f    97.2344f   13.8402f
+    5.0000      5.4000   290.6693m   422.7295f    97.2344f   13.8402f
+    5.0000      6.0000   293.8273m   422.7295f    97.2344f   13.8402f
+    6.0000          0.          0.   306.7689f   306.7689f         0.
+    6.0000   600.0000m   106.8148m   319.2583f   296.0808f  1.224e-16
+    6.0000      1.2000   184.7221m   334.6955f   279.2856f  6.979e-16
+    6.0000      1.8000   243.8294m   352.1142f   257.7719f    1.6452f
+    6.0000      2.4000   302.9367m   369.5330f   236.2582f    2.5926f
+    6.0000      3.0000   322.8342m   388.4324f   189.2582f    6.2474f
+    6.0000      3.6000   342.7316m   407.3317f   142.2582f    9.9022f
+    6.0000      4.2000   354.5032m   417.6508f   115.6834f   12.0190f
+    6.0000      4.8000   358.1487m   419.3894f   109.5337f   12.5977f
+    6.0000      5.4000   361.7943m   421.1281f   103.3841f   13.1763f
+    6.0000      6.0000   365.4399m   422.8668f    97.2344f   13.7550f
+ DATA=DRAIN POINTS=16 CBDSW=0
*       Vbd         ibd         cbd         vbd         ibd         cbd
+   -2.0000    -2.9003p   371.8970f     -1.8000    -2.6102p  380.7287f
+   -1.6000    -2.3202p   391.3235f     -1.4000    -2.0302p  403.3597f
+   -1.2000    -1.7402p   415.3959f     -1.0000    -1.4501p  427.4321f
+-800.0000m    -1.1601p   446.4778f  -600.0000m  -870.0789f  467.8601f
+-400.0000m  -580.0526f   489.2424f  -200.0000m  -290.0263f  510.6247f
+        0.     6.9045p   546.8902f   200.0000m    66.3353n  586.3105f
+ 400.0000m    68.0767u   626.7824f   600.0000m      1.8949  667.2543f
+ 800.0000m481.9861  707.7262f1.0000  116.2491k   748.1981f
+ DATA=SOURCE POINTS=16 CBSSW=0
*       Vbs         ibs         cbs         vbs         ibs         cbs
+   -2.0000    -2.9003p   371.8970f     -1.8000    -2.6102p  380.7287f
+   -1.6000    -2.3202p   391.3235f     -1.4000    -2.0302p  403.3597f
+   -1.2000    -1.7402p   415.3959f     -1.0000    -1.4501p  427.4321f
+-800.0000m    -1.1601p   446.4778f  -600.0000m  -870.0789f  467.8601f
+-400.0000m  -580.0526f   489.2424f  -200.0000m  -290.0263f  510.6247f
+        0.     6.9045p   546.8902f   200.0000m    66.3353n  586.3105f
+ 400.0000m    68.0767u   626.7824f   600.0000m      1.8949  667.2543f
+ 800.0000m    481.9861   707.7262f      1.0000   116.2491k  748.1981f
**********************************************************
.MODEL NMOS2 NMOS MODEL=TABLE
+ W=2E-04 L=1.1E-06 AD=3.296E-10 AS=3.296E-10
+ DATA=CHANNEL POINTS=44 VGS=0.0
*       Vds         vbs         ids         cgs         cgd         cbg
+        0.          0.          0.    29.9047f    29.9047f  376.2814f
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+ 400.0000m          0.   104.8585f    29.9047f    29.9047f  376.2814f
+ 800.0000m          0.   105.5168f    29.9047f    29.9047f  376.2814f
+    1.2000          0.   106.1566f    29.9047f    29.9047f  376.2814f
+    1.6000          0.   106.7964f    29.9047f    29.9047f  376.2814f
+    2.0000          0.   107.4460f    29.9047f    29.9047f  376.2814f
+    2.4000          0.   108.0955f    29.9047f    29.9047f  376.2814f
+    2.8000          0.   108.7510f    29.9047f    29.9047f  376.2814f
+    3.2000          0.   109.4125f    29.9047f    29.9047f  376.2814f
+    3.6000          0.   110.0739f    29.9047f    29.9047f  376.2814f
+    4.0000          0.   110.7353f    29.9047f    29.9047f  376.2814f
+        0.     -1.0000          0.    29.9047f    29.9047f  376.2814f
+ 400.0000m     -1.0000   104.8585f    29.9047f    29.9047f  376.2814f
+ 800.0000m     -1.0000   105.5168f    29.9047f    29.9047f  376.2814f
+    1.2000     -1.0000   106.1566f    29.9047f    29.9047f  376.2814f
+    1.6000     -1.0000   106.7964f    29.9047f    29.9047f  376.2814f
+    2.0000     -1.0000   107.4460f    29.9047f    29.9047f  376.2814f
+    2.4000     -1.0000   108.0955f    29.9047f    29.9047f  376.2814f
+    2.8000     -1.0000   108.7510f    29.9047f    29.9047f  376.2814f
+    3.2000     -1.0000   109.4125f    29.9047f    29.9047f  376.2814f
+    3.6000     -1.0000   110.0739f    29.9047f    29.9047f  376.2814f
+    4.0000     -1.0000   110.7353f    29.9047f    29.9047f  376.2814f
+        0.     -2.0000          0.    29.9047f    29.9047f  376.2814f
+ 400.0000m     -2.0000   104.8585f    29.9047f    29.9047f  376.2814f
+ 800.0000m     -2.0000   105.5168f    29.9047f    29.9047f  376.2814f
+    1.2000     -2.0000   106.1566f    29.9047f    29.9047f  376.2814f
+    1.6000     -2.0000   106.7964f    29.9047f    29.9047f  376.2814f
+    2.0000     -2.0000   107.4460f    29.9047f    29.9047f  376.2814f
+    2.4000     -2.0000   108.0955f    29.9047f    29.9047f  376.2814f
+    2.8000     -2.0000   108.7510f    29.9047f    29.9047f  376.2814f
+    3.2000     -2.0000   109.4125f    29.9047f    29.9047f  376.2814f
+    3.6000     -2.0000   110.0739f    29.9047f    29.9047f  376.2814f
+    4.0000     -2.0000   110.7353f    29.9047f    29.9047f  376.2814f
+        0.     -3.0000          0.    29.9047f    29.9047f  376.2814f
+ 400.0000m     -3.0000   104.8585f    29.9047f    29.9047f  376.2814f
+ 800.0000m     -3.0000   105.5168f    29.9047f    29.9047f  376.2814f
+    1.2000     -3.0000   106.1566f    29.9047f    29.9047f  376.2814f
+    1.6000     -3.0000   106.7964f    29.9047f    29.9047f  376.2814f
+    2.0000     -3.0000   107.4460f    29.9047f    29.9047f  376.2814f
+    2.4000     -3.0000   108.0955f    29.9047f    29.9047f  376.2814f
+    2.8000     -3.0000   108.7510f    29.9047f    29.9047f  376.2814f
+    3.2000     -3.0000   109.4125f    29.9047f    29.9047f  376.2814f
+    3.6000     -3.0000   110.0739f    29.9047f    29.9047f  376.2814f
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+    4.0000     -3.0000   110.7353f    29.9047f    29.9047f  376.2814f
+ DATA=DRAIN POINTS=16 CBDSW=0
*       vbd         ibd         cbd         vbd         ibd         cbd
+   -2.0000    -1.4493p   185.8411f     -1.8000    -1.3044p  190.2543f
+   -1.6000    -1.1594p   195.5487f     -1.4000    -1.0145p  201.5633f
+   -1.2000  -869.5761f   207.5779f     -1.0000  -724.6468f  213.5925f
+-800.0000m  -579.7174f   223.1099f  -600.0000m  -434.7881f  233.7949f
+-400.0000m  -289.8587f   244.4799f  -200.0000m  -144.9294f  255.1648f
+        0.     3.4503p   273.2871f   200.0000m    33.1485n  292.9858f
+ 400.0000m    34.0187u   313.2101f   600.0000m    13.4387m  333.4344f
+ 800.0000m    590.5343   353.6586f      1.0000    58.0909k  373.8829f
+ DATA=SOURCE POINTS=16 CBSSW=0
*       vbs         ibs         cbs         vbs         ibs         cbs
+   -2.0000    -1.4493p   185.8411f     -1.8000    -1.3044p  190.2543f
+   -1.6000    -1.1594p   195.5487f     -1.4000    -1.0145p  201.5633f
+   -1.2000  -869.5761f   207.5779f     -1.0000  -724.6468f  213.5925f
+-800.0000m  -579.7174f   223.1099f  -600.0000m  -434.7881f  233.7949f
+-400.0000m  -289.8587f   244.4799f  -200.0000m  -144.9294f  255.1648f
+        0.     3.4503p   273.2871f   200.0000m    33.1485n  292.9858f
+ 400.0000m    34.0187u   313.2101f   600.0000m    13.4387m  333.4344f
+ 800.0000m    590.5343   353.6586f      1.0000    58.0909k  373.8829f
**********************************************************
.MODEL PMOS1 PMOS MODEL=TABLE
+ W=7E-04 L=4E-07 AD=1.154E-9 AS=1.154E-9
+ DATA=CHANNEL POINTS=77 VBS=0.0
*       Vgs         vds         ids         cgs         cgd         cbg
+        0.          0.          0.    85.4335f    85.4335f  289.6904f
+        0.  -600.0000m    -6.4965p    85.4335f    85.4335f  289.6904f
+        0.     -1.2000    -9.0114p    85.4335f    85.4335f  289.6904f
+        0.     -1.8000   -12.1721p    85.4335f    85.4335f  289.6904f
+        0.     -2.4000   -15.3328p    85.4335f    85.4335f  289.6904f
+        0.     -3.0000   -21.8543p    85.4335f    85.4335f  289.6904f
+        0.     -3.6000   -28.3759p    85.4335f    85.4335f  289.6904f
+        0.     -4.2000   -39.5762p    85.4335f    85.4335f  289.6904f
+        0.     -4.8000   -55.4555p    85.4335f    85.4335f  289.6904f
+        0.     -5.4000   -71.3347p    85.4335f    85.4335f  289.6904f
+        0.     -6.0000   -87.2140p    85.4335f    85.4335f  289.6904f
+   -1.0000          0.          0.   536.8227f   536.8227f         0.
+   -1.0000  -600.0000m    -4.5084m   686.1264f   170.1530f   31.5109f
+   -1.0000     -1.2000    -4.9761m   686.1264f   170.1530f   31.5109f
+   -1.0000     -1.8000    -5.4630m   686.1264f   170.1530f   31.5109f
+   -1.0000     -2.4000    -5.9500m   686.1264f   170.1530f   31.5109f
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+   -1.0000     -3.0000    -6.5206m   686.1264f   170.1530f   31.5109f
+   -1.0000     -3.6000    -7.0912m   686.1264f   170.1530f   31.5109f
+   -1.0000     -4.2000    -7.7075m   686.1264f   170.1530f   31.5109f
+   -1.0000     -4.8000    -8.3695m   686.1264f   170.1530f   31.5109f
+   -1.0000     -5.4000    -9.0314m   686.1264f   170.1530f   31.5109f
+   -1.0000     -6.0000    -9.6934m   686.1264f   170.1530f   31.5109f
+   -2.0000          0.          0.   536.8227f   536.8227f         0.
+   -2.0000  -600.0000m   -36.0517m   623.6169f   421.6390f    5.8803f
+   -2.0000     -1.2000   -50.6744m   674.4951f   308.8774f   14.8968f
+   -2.0000     -1.8000   -53.8991m   684.8673f   239.5152f   22.4329f
+   -2.0000     -2.4000   -57.1238m   695.2395f   170.1530f   29.9691f
+   -2.0000     -3.0000   -59.5405m   695.2395f   170.1530f   29.9691f
+   -2.0000     -3.6000   -61.9571m   695.2395f   170.1530f   29.9691f
+   -2.0000     -4.2000   -64.4878m   695.2395f   170.1530f   29.9691f
+   -2.0000     -4.8000   -67.1325m   695.2395f   170.1530f   29.9691f
+   -2.0000     -5.4000   -69.7773m   695.2395f   170.1530f   29.9691f
+   -2.0000     -6.0000   -72.4221m   695.2395f   170.1530f   29.9691f
+   -3.0000          0.          0.   536.8227f   536.8227f         0.
+   -3.0000  -600.0000m   -58.2651m   585.1169f   489.2190f    1.2319f
+   -3.0000     -1.2000   -91.7005m   628.2461f   402.6441f    7.6872f
+   -3.0000     -1.8000   108.5231m   663.3161f   286.3986f   18.4950f
+   -3.0000     -2.4000   125.3456m   698.3861f   170.1530f   29.3028f
+   -3.0000     -3.0000   129.7715m   698.3861f   170.1530f   29.3028f
+   -3.0000     -3.6000   134.1974m   698.3861f   170.1530f   29.3028f
+   -3.0000     -4.2000   138.8473m   698.3861f   170.1530f   29.3028f
+   -3.0000     -4.8000   143.7214m   698.3861f   170.1530f   29.3028f
+   -3.0000     -5.4000   148.5955m   698.3861f   170.1530f   29.3028f
+   -3.0000     -6.0000   153.4697m   698.3861f   170.1530f   29.3028f
+   -4.0000          0.          0.   536.8227f   536.8227f         0.
+   -4.0000  -600.0000m   -72.3381m   569.7088f   506.9995f  5.178e-16
+   -4.0000     -1.2000   122.8842m   605.5234f   454.6861f    3.4795f
+   -4.0000     -1.8000   158.5680m   642.6790f   383.9428f    8.5352f
+   -4.0000     -2.4000   194.2517m   679.8345f   313.1995f   13.5909f
+   -4.0000     -3.0000   201.5484m   687.8281f   255.9809f   19.7290f
+   -4.0000     -3.6000   208.8451m   695.8216f   198.7623f   25.8671f
+   -4.0000     -4.2000   216.0155m   699.8184f   170.1530f   28.9362f
+   -4.0000     -4.8000   223.0596m   699.8184f   170.1530f   28.9362f
+   -4.0000     -5.4000   230.1038m   699.8184f   170.1530f   28.9362f
+   -4.0000     -6.0000   237.1479m   699.8184f   170.1530f   28.9362f
+   -5.0000          0.          0.   536.8227f   536.8227f         0.
+   -5.0000  -600.0000m   -82.0478m   561.6789f   515.1538f  2.832e-16
+   -5.0000     -1.2000   145.1179m   589.1833f   482.6673f    1.6287f
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+   -5.0000     -1.8000   195.1922m   618.3449f   441.6375f    3.8500f
+   -5.0000     -2.4000   245.2665m   647.5065f   400.6078f    6.0712f
+   -5.0000     -3.0000   262.3422m   668.7366f   308.4259f   15.1250f
+   -5.0000     -3.6000   279.4180m   689.9668f   216.2440f   24.1788f
+   -5.0000     -4.2000   292.3304m   700.5818f   170.1530f   28.7057f
+   -5.0000     -4.8000   301.0796m   700.5818f   170.1530f   28.7057f
+   -5.0000     -5.4000   309.8287m   700.5818f   170.1530f   28.7057f
+   -5.0000     -6.0000   318.5779m   700.5818f   170.1530f   28.7057f
+   -6.0000          0.          0.   536.8227f   536.8227f         0.
+   -6.0000  -600.0000m   -89.1503m   556.7781f   519.8222f  1.782e-16
+   -6.0000     -1.2000   161.5093m   578.7300f   496.4458f  9.433e-16
+   -6.0000     -1.8000   222.3355m   602.0021f   468.1484f    2.1798f
+   -6.0000     -2.4000   283.1618m   625.2741f   439.8510f    3.4163f
+   -6.0000     -3.0000   313.8994m   648.3146f   385.2116f    7.7973f
+   -6.0000     -3.6000   344.6370m   671.3551f   330.5722f   12.1783f
+   -6.0000     -4.2000   365.1282m   685.4693f   284.2383f   16.3944f
+   -6.0000     -4.8000   375.3729m   690.6572f   246.2098f   20.4455f
+   -6.0000     -5.4000   385.6175m   695.8450f   208.1814f   24.4966f
+   -6.0000     -6.0000   395.8622m   701.0329f   170.1530f   28.5478f
+ DATA=DRAIN POINTS=16 CBDSW=0
*       vbd         ibd         cbd         vbd         ibd         cbd
+    2.0000     5.0752p   825.3019f      1.8000     4.5677p  844.9008f
+    1.6000     4.0602p   868.4125f      1.4000     3.5527p  895.1228f
+    1.2000     3.0451p   921.8332f      1.0000     2.5376p  948.5435f
+ 800.0000m     2.0301p   990.8093f   600.0000m     1.5226p    1.0383p
+ 400.0000m     1.0150p     1.0857p   200.0000m   507.5244f    1.1332p
+        0.   -12.0824p     1.2136p  -200.0000m  -116.0819n    1.3011p
+-400.0000m  -119.1292u     1.3909p  -600.0000m     -3.3159    1.4807p
+-800.0000m   -843.4398     1.5706p     -1.0000  -203.4272k    1.6604p
+ DATA=SOURCE POINTS=16 CBSSW=0
*       vbs         ibs         cbs         vbs         ibs         cbs
+    2.0000     5.0752p   825.3019f      1.8000     4.5677p  844.9008f
+    1.6000     4.0602p   868.4125f      1.4000     3.5527p  895.1228f
+    1.2000     3.0451p   921.8332f      1.0000     2.5376p  948.5435f
+ 800.0000m     2.0301p   990.8093f   600.0000m     1.5226p    1.0383p
+ 400.0000m     1.0150p     1.0857p   200.0000m   507.5244f    1.1332p
+        0.   -12.0824p     1.2136p  -200.0000m  -116.0819n    1.3011p
+-400.0000m  -119.1292u     1.3909p  -600.0000m     -3.3159    1.4807p
+-800.0000m   -843.4398     1.5706p     -1.0000  -203.4272k    1.6604p
[END_DEVICE_DEF]
*
[COMPONENT]
```

```
LCR3.PKG LCR3 LCR3_MUTUAL
[END_IC]

[PACKAGE]
[NAME] LCR3
[IMIC_VER] 1.3
[LEVEL] 2

[MODEL_INDEX]
LCR3_MUTUAL

[DATE] AUGUST 18, 1999

[NOTES]
TSOP 3 PIN PACKAGE ELECTRICAL CHARACTERISTICS MODEL FOR ALVCH
LCR3_SELF MODEL EXCLUDE MUTUAL ELEMENTS
THE HIGHT TO REFERENCE GROUND IS 152 UM.

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[MANUFACTURER] ABC, LTD.

[MODEL_NAME] LCR3_MUTUAL

[INNER_TERMINAL]
LEAD07    2
LEAD10    3
LEAD11    4

[OUTER_TERMINAL]
PIN07     6
PIN10     7
PIN11     8
REFG      9

[CONNECTION]
.SUBCKT LCR3 2 3 4 6 7 8 9
C001_002 11 12 1.99788E-14
C001_003 11 13 5.45655E-15
C001 11 9 3.20735E-15
C002_003 12 13 1.0445E-13
C002 12 9 5.6009E-15
C003 13 9 5.35975E-15
L001 2 24 2.95443E-10
L001_N 16 24 2.95443E-10
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L005 6 28 2.95443E-10
L005_N 20 28 2.95443E-10
R001 11 16 0.000715901
R005 11 20 0.000715901
L002 3 25 2.67161E-10
L002_N 17 25 2.67161E-10
L006 7 29 2.67161E-10
L006_N 21 29 2.67161E-10
R002 12 17 0.000640238
R006 12 21 0.000640238
K0021001 L002 L001 0.180625
K0022001 L002_N L001_N 0.180625
K0061005 L006 L005 0.180625
K0062005 L006_N L005_N 0.180625
L003 4 26 2.6009E-10
L003_N 18 26 2.6009E-10
L007 8 30 2.6009E-10
L007_N 22 30 2.6009E-10
R003 13 18 0.000619881
R007 13 22 0.000619881
K0031001 L003 L001 0.136142
K0032001 L003_N L001_N 0.136142
K0071005 L007 L005 0.136142
K0072005 L007_N L005_N 0.136142
K0031002 L003 L002 0.424273
K0032002 L003_N L002_N 0.424273
K0071006 L007 L006 0.424273
K0072006 L007_N L006_N 0.424273
.ENDS LCR3

[END_PACKAGE]
```

Explanatory note

1. INTRODUCTION

With an increase in speed of electronic system, it becomes necessary to accurately predict electrical performance including noise in electronic systems with ICs.

Simulators have been used for this purpose. Simulators need accurate models for describing electrical properties of ICs. Semiconductor-makers are required by their customers to prepare device models for various simulation tools, some of which are not compatible with SPICE. In addition, since SPICE models contain proprietary process parameters, a Non Disclosure Agreement is typically required to obtain these from the vendor.

IBIS (I/O Buffer Interface Specification) has been proposed as a model for LSI parts. IBIS (V3.2) has the following features:

(1) Since electrical properties of I/O buffers are described in table format, disclosure of proprietary information such as process parameters is greatly reduced.

(2) It is easy to get IBIS models that are supported by many simulation tools.

(3) A public domain tool can convert SPICE models into IBIS models.

However, IBIS models seem to have the following problems:

(1) The modeling of power and ground currents is insufficient for accurate power and ground bounce analysis.

(2) Since an IBIS model has only the final stage at output and input, it is difficult to model the effect of loading on circuit boards on output and input waveforms. The fixed model taken by IBIS has little flexibility for describing other circuitry.

(3) In order to simulate EMI with accuracy, more information such as material constant and 3-D structures is needed.

Thus, the EIAJ Semiconductor Standard Committee has been pursuing improvement of I/O interface models. To address the above problems, this project group has been formed.

Electronic Industries Association of Japan (EIAJ) and The Japan Electronic Development Association (JEIDA) have marged effective November 1, 2000, The Japan Electronics and Information Technology Industries Association (JEITA).

2. Member of discussion

This standard has been discussed by the I/O Interface Model PG (Project Group) which belongs to Group on Integrated Circuits of Technical Standardization Committee on Semiconductor Devices. The member are shown as following.

<Technical Standardization Committee on Semiconductor Devices>

Chairman	Mitsutoshi Ito	NEC Corp.

<Group on Integrated Circuits>

Chairman	Shigenori Abe	Rohm Co., Ltd.

< I/O Interface Model Project Group >

Leader	Hideki Fukuda	
Sub-Leader	Tsuyoshi Watanabe	NEC corp.
	Saburo Hojo	Hitachi, Ltd.
	Tomoo Ishida	Mitsubishi Electric Corp.
Member	Shinji Tanabe	Oki Electric Industry Co., Ltd.
	Yuki Hashimoto	Oki Electric Industry Co., Ltd.
	Hidetoshi Mizutani	Sanyo Electric Co., Ltd.
	Toshikazu Tanabe	Sharp Corp.
	Tsuyoshi Horigome	Shindengen
	Fumihito Ikeda	Seiko Epson Corp.
	Takeji Tokumaru	Toshiba Corp.
	Yuichiro Yoshida	Toshiba Corp.
	Toshiyuki Kobayashi	Texas Instruments Japan Ltd.
	Naoaki Naka	Fujitsu Ltd.
	Takashi Hirata	Matsushita Electric Industries Co., Ltd.
	Nobuaki Tsuji	Yamaha Corp.
Special Member	Norio Matsui	Applied Simulation Technology
	Hiroki Oka	NTT Advanced Technology Corp.
	Toru Inoue	Oki Electric Industry Co., Ltd.
	Yutaka Takashina	Zuken Incorporated
	Ichihiko Eguchi	Hitachi, Ltd.
	Atsushi Nakamura	Hitachi, Ltd.