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EIAJ ED－5512

3.3V用スタブ直列終端型論理(SSTL_3)
標準機能仕様
(電源電圧3.3Vデジタル集積回路インタフェース標準)

Stub Series Terminated Logic for 3.3Volts (SSTL_3)
(A 3.3V Supply Voltage based Interface Standard for Digital ICs)

1996年3月制定

作　成

半導体標準化委員会

Technical Standardization Committee on Semiconductor Devices

発　行

社団法人 日本電子機械工業会

Electronic Industries Association of Japan

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Stub Series Terminated Logic for 3.3 Volts (SSTL_3)

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1. Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_3 logic switching range, nominally 0 V to 3.3V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. In many cases VDD and VDDQ will have the same voltage level. However for noise rejection reasons, the supplies may be routed separately in the system interconnect. The VDD value is not specified in this standard other than that VDDQ value may not exceed that of VDD.

1.1 Standard structure

The standard is defined in three sections:
The first section defines pertinent supply voltage requirements common to all compliant ICs.
The second section defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.
The third section specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments. The output specifications are divided into two classes, Class I and Class II, which are distinguished by drive requirements and application.

A given IC need not be equipped with both classes of output drivers, but each must support at least one to claim SSTL_3 output compliance.
The full input reference level (VREF) range specified is required on each IC in order to allow any SSTL 3, IC to receive signals from any SSTL_3 output driver.

1.2 Rationale and assumptions

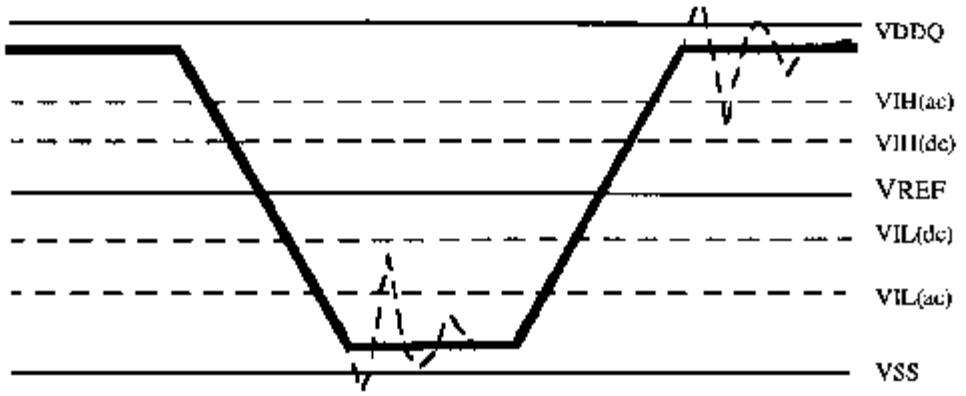
The SSTL_3 standard has been developed particularly with the objective of providing a relatively simple upgrade path from LVTTL designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage. Actual selection of the resistor values is a system design decision and beyond the scope of this standard. However in order to provide a basis, the driver characteristics will be derived in terms of a typical 50 Ohms environment.

While driver characteristics are derived from a 50 Ohm environment, this standard will work for other impedance levels. The system designer will be able to vary impedance levels, termination resistors and supply voltage and be able to calculate the effect on system voltage margins. This is accomplished precisely because drivers and receivers are specified independently of each other. The standard defines a reference voltage VREF which is used at the receivers as well as a voltage VTT to which termination resistors are connected. In typical applications VTT tracks as a ratio of VDDQ. In turn VREF will be given the value of VTT. In some standards this ratio equals 0.5. If this value were to be applied to SSTL_3, the maximum value of VTT and thus VREF would be 1.8 V (0.5* 3.6). In order to be more closely compatible with LVTTL, the nominal ratio was selected to be 0.45. This leads to a typical VTT and VREF value of about 1.5 V if VDDQ = 3.3 V. This value is close to the internal reference voltage in current LVTTL designs.

2. Supply voltage and logic input levels

The standard defines both ac and dc input signal values. Making this distinction is important for the design of high gain, differential, receivers that are required. The ac values are chosen to indicate the levels at which the receiver must meet its timing specifications. The dc values are chosen such that the final logic state is unambiguously defined, that is once the receiver input has crossed this value, the receiver will change to and maintain the new logic state. The reason for this approach is that many input waveforms will include a certain amount of "ringing". The system designer can be sure that the device will switch state a certain amount of time after the input has crossed ac threshold and not switch back as long as the input stays beyond the dc threshold. The relationship of the different levels is shown in figure 2.1 An example of ringing is illustrated in the dotted waveform.

Figure 2.1 SSTL_3 Input levels



2.1 Supply voltage levels

Table 2.1 Supply voltage levels

Symbol	Parameter	Min.	Nom	Max.	Units	Notes
VDD	Device supply voltage	VDDQ	n/a		V	1
VDDQ	Output supply voltage	3.0	3.3	3.6	V	1
VREF	Input reference voltage	1.3	1.5	1.7	V	2, 3
VTT	Termination voltage	VREF - 0.05	VREF	VREF + 0.05	V	4

Notes:

1. There is no specific device VDD supply voltage requirement for SSTL_3 compliance. However under all conditions VDDQ must be less than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.45 * VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed 2% VREF (dc).
4. VTT of transmitting device must track VREF of receiving device.

2.2 Input parametric

Table 2.2-a Input dc logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
VIH (dc)	dc input logic high	VREF + 0.20	VDDQ + 0.3	V	1
VIL (dc)	dc input logic low	- 0.30	VREF - 0.20	V	1

Notes:

1. Within this standard, it is the relationship of the VDDQ of the driving device and the VREF of the receiving device that determines noise margins. However, in the case of VIH (Max.) (i.e. input overdrive) it is the VDDQ of the receiving device that is referenced. In the case where a device is implemented that supports SSTL_3 inputs but has no SSTL_3 outputs (e.g., a translator), and therefore no VDDQ supply voltage connection, inputs must tolerate input overdrive to 3.9 V (High corner VDDQ + 300 mV).

Table 2.2-b Input ac logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
VIH (ac)	dc input logic high	VREF + 0.40		V	
VIL (ac)	dc input logic low		VREF - 0.40	V	

2.3 ac Test Conditions

The ac input test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 2 V peak to peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the ac input level. This is illustrated in figure 2.3.

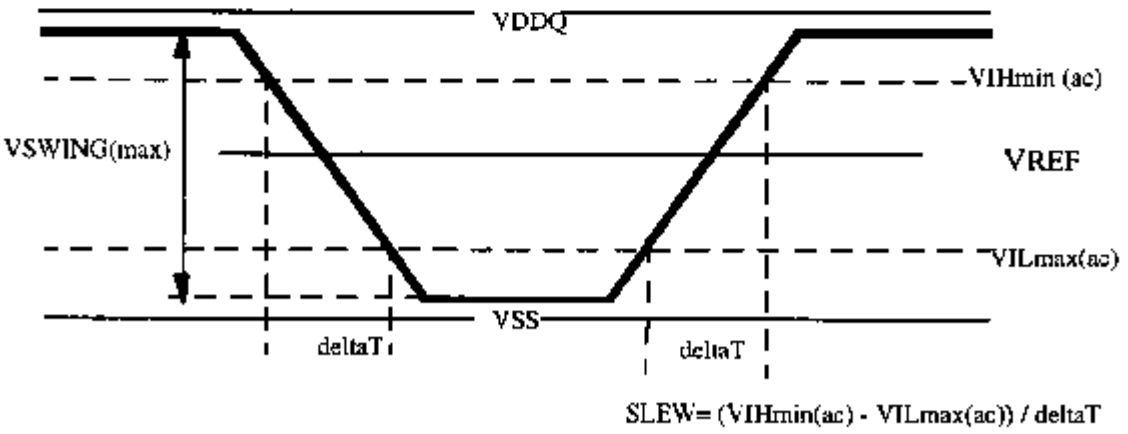
Table 2.3 ac input test conditions

Symbol	Condition	Value	Units	Notes
VREF	Input reference voltage	0.45 * VDDQ	V	1, 4
VSWINGmax	Input signal maximum peak to peak swing	2.0	V	1, 2
SLEW	Input signal minimum slew rate	1.0	V/ns	3

Notes:

1. In all cases, input waveform timing is referenced to the input signal crossing through the VREF level applied to the device under test. Table 2.1 identifies the VREF range supported in SSTL_3.
2. Compliant devices must still meet the VIH(ac) and VIL(ac) specifications under actual use conditions.
3. The 1V/ns input signal minimum slew rate is to be maintained in the VILmax (ac) to VIHmin(ac) range of the input signal swing, consistent with the ac logic specification of table 2.2-b. See alsofigure 2.3.
4. It was agreed in JEDEC discussions that ac test conditions could be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis that the device will meet its timing specifications under all supported voltage conditions.

Figure 2.3 ac Input Test Signal Waveform

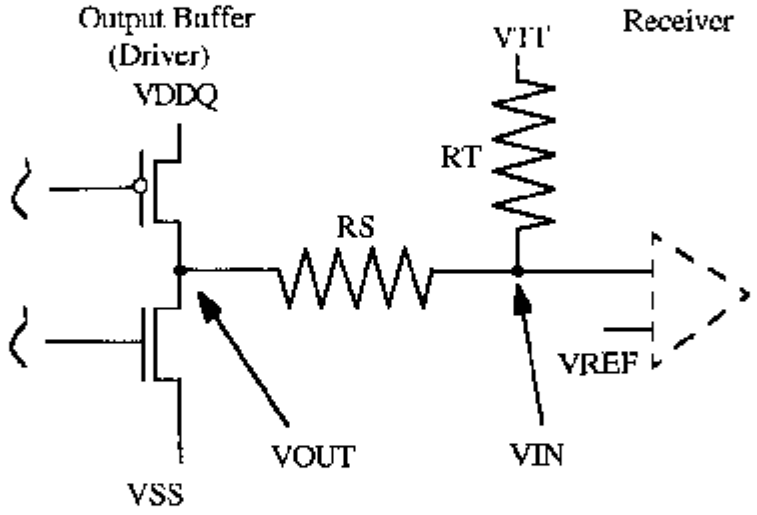


3. SSTL_3 Output Buffers

3.0 Overview

This specification sets minimum requirements for output buffers in such a way that when they are applied within the range of power supply voltages specified in SSTL_3 and are used in conjunction with SSTL_3 input receivers then the input receiver specifications can be met or exceeded. The specifications are quite different from traditional specifications, where minimum values for VOH and maximum values for VOL are set which apply to the entire supply range. In SSTL_3, the input voltage provided to the receiver depends on the driver as well as on the termination voltage and termination resistors. Figure 3.0 shows the typical dc environment that the output buffer is presented with.

Figure 3.0 Typical Output Buffer (Driver) environment



Of particular interest here are the values VOUT and VIN. These values depend not only on the current drive capabilities of the buffer, but also on the values of VDDQ and VTT (VREF is equal to VTT). The important condition is that VIN be at least 400mV above or below VREF as a result of VOUT attaining its maximum low or it's minimum high value. As will be seen later, the two cases of interest for SSTL_3 are where the series resistor RS equals 25 Ohms and the termination resistor RT equals 50 Ohms (for Class I) or 25 Ohms (for Class II). VTT is specified as being equal to 0.45 * VDDQ.

In order to meet the 400mV minimum requirement for Vin, a minimum of 8mA must be developed across RT if RT equals 50 Ohms (Class I) or 16mA in case RT equals 25 Ohms (Class II). The driver specification now must guarantee that these values of VIN are obtained in the worst case conditions specified by this standard.

Table 3.0 Spread sheet showing SSTL_3 circuit voltages depending on VDDQ.
(For reference only)

Conditions	Units	Class I	Class I	Class I	Class II	Class II	Class II
VDDQ	V	3.0	3.3	3.6	3.0	3.3	3.6
VTT	V	1.3	1.5	1.7	1.3	1.5	1.7
VREF	V	1.3	1.5	1.7	1.3	1.5	1.7
Termination Resistor. RT	Ohms	50	50	50	25	25	25
Series Resistor, RS	Ohms	25	25	25	25	25	25
Delta VIN	V	0.4	0.4	0.4	0.4	0.4	0.4
Output High Driver							
Voltage at VIN	V	1.7	1.9	2.1	1.7	1.9	2.1
Voltage at VOUT	V	1.9	2.1	2.3	2.1	2.3	2.5
Pull-up Source-Drain Voltage	V	1.1	1.2	1.3	0.9	1.0	1.1
Output Current	A	-0.008	-0.008	-0.008	-0.016	-0.016	-0.016
On resistance	Ohms	137.50	150.00	162.50	56.25	62.50	68.75
Output Low Driver							
Voltage at VIN	V	0.9	1.1	1.3	0.9	1.1	1.3
Voltage at VOUT	V	0.70	0.9	1.1	0.5	0.7	0.9
Output Current	A	0.008	0.008	0.008	0.016	0.016	0.016
On resistance	Ohms	87.50	112.50	137.50	31.25	43.75	56.25

As can be seen from Table 3.0 the most stringent requirements will result where VDDQ=3.0V, since for that case the output driver transistors must have the lowest "on" resistance. If the driver outputs are sized for this condition, then for all other VDDQ voltage applications, the resulting input signal will be larger than the minimum required 400mV.

3.1 SSTL_3 Class I output buffers

3.1.1 Push-pull output buffer for symmetrically single parallel terminated loads with series resistor. (VTT=0.45*VDDQ)

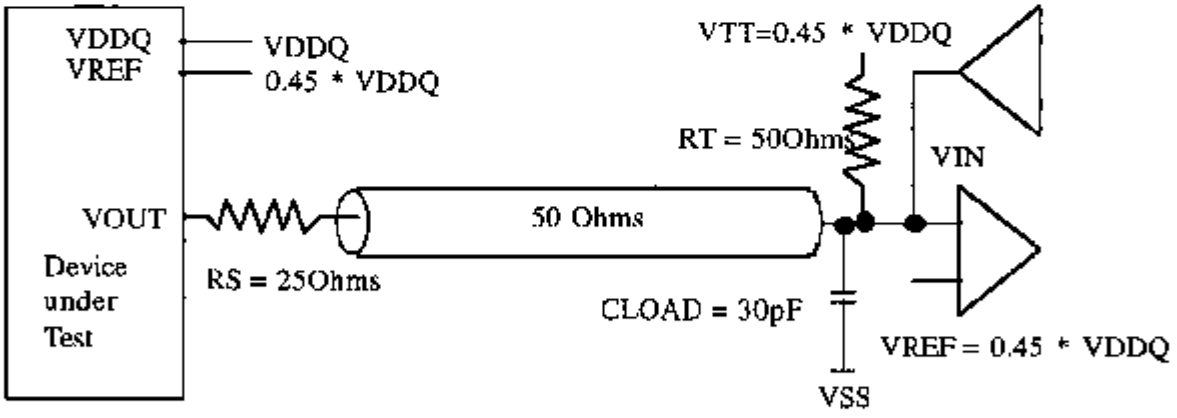
Table 3.1-a Output dc current drives

Symbol	Parameter	Min.	Max.	Units	Notes
IOH (dc)	Output minimum source dc current	-8		mA	1, 3, 4
IOL (dc)	Output minimum sink dc current	8		mA	2, 3, 4

Notes:

1. VDDQ = 3.0 V; VOUT = VDDQ - 1.1 V
2. VDDQ = 3.0 V; VOUT = 0.7 V.
3. The dc value of VREF applied to the receiving device is expected to be set to VTT.
4. The values of IOH(dc) and IOL(dc) are based on VDDQ = 3.0 V and VTT = 1.3V. They are used to test device current drive capability which ultimately delivers acceptable noise margin for an SSTL_3 receiver. Under these conditions VOH is 1.9V and VOL is 0.7V. Under other conditions for VDDQ and VTT the typical output levels are discussed in Section 3.0 (Overview).

Figure 3.1 An example of SSTL_3, Class I, symmetrically single parallel terminated output load, and series resistor



3.1.2 SSTL_3 Class I output ac test conditions

This testing regimen is used to verify SSTL_3 Class I type output buffers (push-pull output buffers designed for symmetrically single parallel terminated loads with series resistor).

This section is added to set the conditions under which the driver ac specifications can be tested. The test circuit is assumed to be similar to the circuit shown in figure 3.1. It was agreed in JEDEC discussions that ac test conditions could be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis, that the device will meet its timing specifications under all supported voltage conditions. Table 3.1 assumes that +/- 0.4 V must be developed across the 50 Ohm termination resistor at VIN. With a series resistor of 25 Ohms this translates into a minimum requirement of 0.6 volt swing relative to VTT, at the output of the device.

Table 3.1-b ac test conditions

Symbol	Condition	Value	Units	Notes
VOH	Minimum required output pull-up under ac test load	VTT + 0.6	V	
VOL	Maximum required output pull-down under ac test load	VTT - 0.6	V	
VOTR	Output timing measurement reference level	0.45 * VDDQ	V	1

Notes:
1. The VDDQ of the device under test is referenced.

3.2 SSTL_3 Class II output buffers

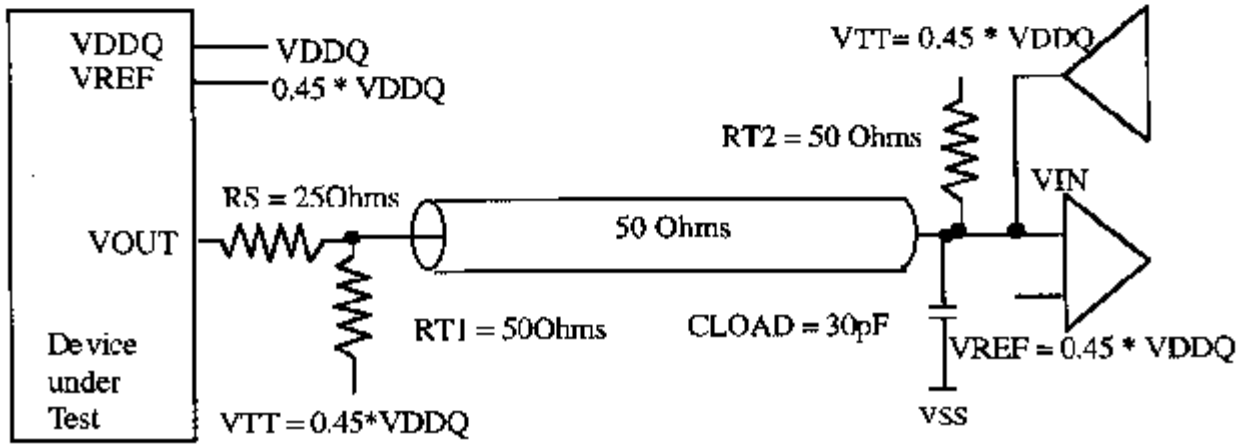
3.2.1 Push-pull output buffer for symmetrically double parallel terminated loads with series resistor (VTT = 0.45 * VDDQ)

Table 3.2-a Output dc current drive

Symbol	Parameter	Min.	Max.	Units	Notes
IOH (dc)	Output minimum source dc current	-16		mA	1, 3, 4
IOL (dc)	Output minimum sink dc current	16		mA	2, 3, 4

Notes
1. VDDQ = 3.0 V; VOUT = VDDQ - 0.9 V
2. VDDQ = 3.0 V; VOUT = 0.6 V.
3. The dc value of VREF applied to the receiving device is expected to be set to VTT.
4. The values of IOH(dc) and VOL(dc) are based on VDDQ = 3.0V and VTT = 1.3. They are used to test device current drive capability which ultimately delivers acceptable noise margin for an SSTL_3 receiver. Under these conditions VOH is 2.1 V and VOL is 0.5 V. Under other conditions for VDDQ and VTT the typical output levels are discussed in Section 3.0(Overview).

Figure 3.2 An example of SSTL_3, Class II, symmetrically double parallel terminated output load with series resistor



3.2.2 SSTL_3 Class II output ac test conditions

This testing regimen is used to verify SSTL_3 Class II type output buffers (push-pull output buffers designed for symmetrically double parallel terminated loads with series resistor).

This section is added to set the conditions under which the driver ac specifications can be tested. The test circuit is assumed to be similar to the circuit shown in figure 3.2. It was agreed in JEDEC discussions that ac test conditions could be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis, that the device will meet its timing specifications under all supported voltage conditions. Table 3.2-b assumes that +/- 0.4 V must be developed across the effectively 25 Ohm termination resistor at VIN . With a series resistor of 25 Ohms this translates into a minimum requirement of 0.8 volt swing relative to VTT, at the output of the device.

Table 3.2-b ac test conditions

Symbol	Condition	Value	Units	Notes
VOH	Minimum required output pull-up under ac test load	VTT + 0.8		
VOL	Maximum required output pull-down under ac test load	VTT - 0.8	V	
VOTR	Output timing measurement reference level	0.45 * VDDQ	V	1

Notes:

1. The VDDQ of the device under test is referenced.

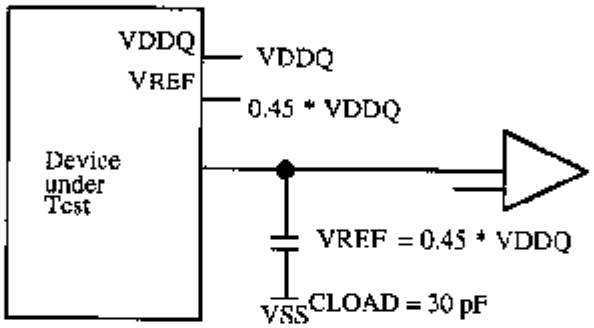
4. Other Application (For reference only)

The specifications for Class I and II were based on an environment comprising both series and parallel terminating resistors. In this nonbinding section we will show some derived applications. Clearly it is not the intention to show all possible variations in this standard.

4.1 Push-pull output buffer for unterminated loads

In many applications where interconnections are short, there is no need for any termination at all. An example of this is shown in figure 3.3.1. This application can be served by a Class I or Class II type buffer and an SSTL_3 type receiver. Noise margins and possibly speed will be improved over LVTTL

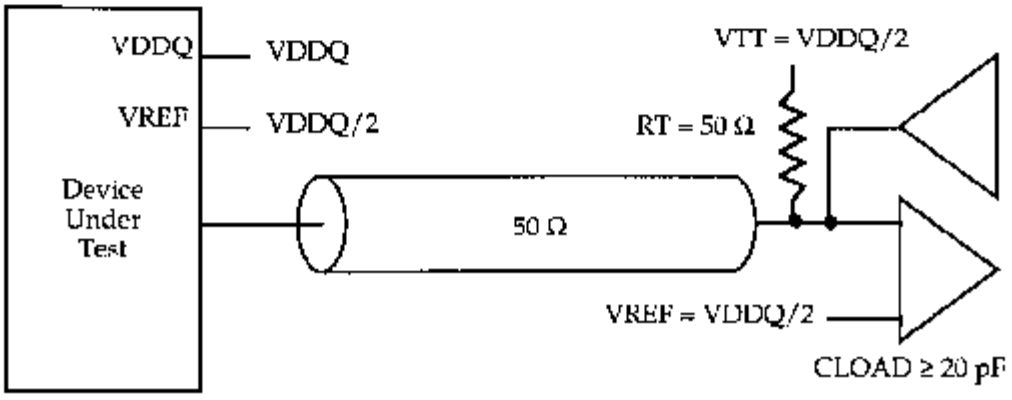
Figure 4.1 An example of SSTL_3 unterminated output load



4.2 Push-pull output buffer for symmetrically single parallel terminated loads (VTT = 0.45* VDDQ)

Sometimes the system application requires longer transmission lines that will only be terminated at one end. An example of this may be address drivers on a memory board. This application can also be served with a Class I or Class II type buffer and an SSTL_3 receiver. An example is shown in figure 3.3.2.

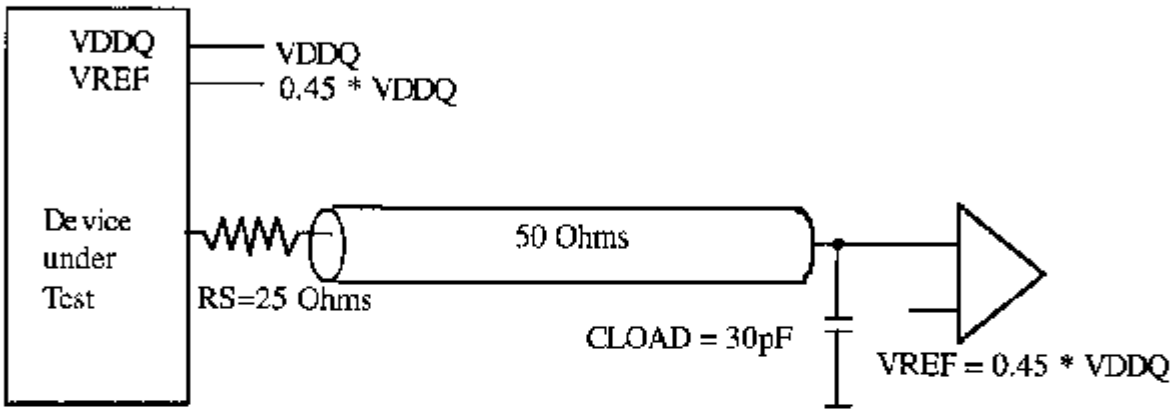
Figure 4.2 An example of SSTL_3. Class I or Class II, buffer with symmetrically single parallel terminated output loads.



4.3 **Push-pull output buffer for externally source series terminated loads**

In other applications the system designer may wish to terminate at the signal source rather than at the end of the transmission line. One advantage of this approach is that there is no need for a VTT power supply. This application may again be served with a Class I or Class II type buffer and SSTL_3 receiver. An example is shown in figure 3.3.3. In this example a Class II type buffer might be preferred since it comes closer, in conjunction with the series resistor, to match the characteristic impedance of the the transmission line.

Figure 4.3 An example of SSTL_3, Class I or Class II, Externally Source Series terminated output load



4.4 **Push-pull output buffer for symmetrically double parallel terminated loads (VTT = 0.45 * VDDQ)**

Finally, the system designer may require a bus system which must be terminated at both sides. However, the drivers are connected directly onto the bus so there are no stubs present. In that case, the designer may decide to eliminate the series resistors entirely. This application can be implemented using a Class I or Class II driver and SSTL 3 receiver. However a Class II buffer would dissipate more power due to its larger current drive and thus might require special cooling.

Figure 4.4 An example of SSTL_3, Class I, buffer with symmetrically double parallel terminated output load