Standard of Electronic Industries Association of Japan

EIAJ ED-5513

Stub Series Terminated Logic for 2.5 Volts (SSTL_2)

(A 2.5V Supply Voltage based Interface Standard for Digital ICs)

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(A 2.5V Supply Voltage based Interface Standard for Digital ICs)

1. Scope

This standard defines the input, output specifications and AC test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0V to 2.5V. The standard may be applied to ICs operating with separate V_{DD} and V_{DDQ} supply voltages. In many cases V_{DD} and V_{DDQ} will have the same voltage level. The V_{DD} value is not specified in this standard other than that V_{DDQ} value may not exceed that of V_{DD}.

1.1 Standard structure

The standard is defined in three sections;

The first section defines pertinent supply voltage requirements common to all compliant ICs.

The second section defines the minimum DC and AC input parametric requirements and AC test conditions for inputs on compliant devices.

The third section specifies the minimum required output characteristics of, and AC test conditions for, compliant outputs targeted for various application environments. The output specifications are divided into two classes, Class I and Class II, which are distinguished by drive requirements and application.

A given IC need not be equipped with both classes of output drivers, but each must support at least one to claim SSTL_2 output compliance.

The full input reference level (V_{REF}) range specified is required on each IC in order to allow any SSTL_2 IC to receive signals from any SSTL_2 output driver.

1.2 Rationale and assumptions

The SSTL_2 standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage.

Actual selection of the resistor values is a system design decision and beyond the scope of this standard. However in order to provide a basis, the driver characteristics will be derived in terms of a typical 50Ω environment.

While driver characteristics are derived from a 50Ω environment, this standard will work for other impedance levels. The system designer will be able to vary impedance levels, termination resistors and supply voltage and be able to calculate the effect on system voltage margins. This is accomplished precisely because drivers and receivers are specified independently of each other. The standard defines a reference voltage V_{REF} which is used at the receivers as well as a voltage V_{TT} to which termination resistors are connected. In typical applications V_{TT} tracks as a ratio of V_{DDQ}. In turn V_{REF} will be given the value of V_{TT}. In some standards this ratio equals 0.5.

2 Supply Voltage and Logic Input Levels

The standard defines both AC and DC input signal values. Making this distinction is important for the design of high gain, differential, receivers that are required. The AC values are chosen to indicate the levels at which the receiver must meet its timing specifications. The DC values are chosen such that the final logic state is unambiguously defined, that is once the receiver input has crossed this value, the receiver will change to and maintain the new logic state. The reason for this approach is that many input wave-forms will include a certain amount of "ringing". The system designer can be sure that the device will switch state a certain amount of time after the input has crossed AC threshold and not switch back as long as the input stays beyond the DC threshold. The relationship of the different levels is shown in Figure 2.1. An example of ringing is illustrated in the dotted wave-form.

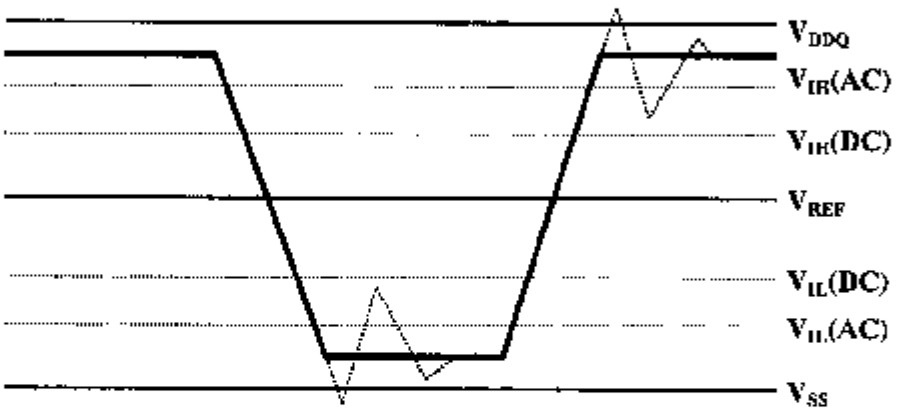

Figure 2.1 SSTL_2 Input voltage levels

2.1 Supply voltage levels

Table 2.1 Supply voltage levels

Symbol	Parameter	Min.	Nom	Max.	Units	Notes
V_{DD}	Device supply voltage	V_{DDQ}		n/a	V	1
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	V	1
V_{REF}	Input reference voltage	1.15	1.25	1.35	V	2, 3
V_{TT}	Termination voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	4

<Notes>

1. There is no specific device V_{DD} supply voltage requirement for SSTL_2 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
3. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF} (DC).
4. V_{TT} of transmitting device must track V_{REF} of receiving device.

2.2 Input parametric

Table 2.2-a Input DC logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (DC)	DC input logic high	V_{REF} + 0.18	V_{DDQ} + 0.3	V	1
V_{IL} (DC)	DC input logic low	- 0.3	V_{REF} - 0.18	V	1

<Note>

Within this standard, it is the relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device that determines noise margins. However, in the case of V_{IH} (Max.) (I.e. input overdrive) it is the V_{DD} of the receiving device that is referenced. In the case where a device is implemented that supports SSTL_2 inputs but has no SSTL_2 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

Table 2.2-b Input AC logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH} (AC)	AC input logic high	V_{REF} + 0.35		V	
V_{IL} (AC)	AC input logic low		V_{REF} - 0.35	V	

2.3 AC test conditions

The AC input test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.5 V peak to peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the AC input level. This is illustrated in Figure 2.3.

Table 2.3 AC input test conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 × V_{DDQ}	V	1,4
V_{SWING} (max)	Input signal maximum peak to peak swing	1.5	V	1,2
SLEW	Input signal minimum slew rate	1.0	V/ns	3

<Notes>

1. In all cases, input wave-form timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test. Table 2.1 identifies the V_{REF} range supported in SSTL_2.
2. Compliant devices must still meet the V_{IH}(AC) and V_{IL}(AC) specifications under actual use conditions.
3. The 1V/ns input signal minimum slew rate is to be maintained in the V_{IL}max (AC) to V_{IH} min(AC) range of the input signal swing, consistent with the AC logic specification of table 2.2-b. See also Figure 2.3.
4. It was agreed in JEDEC discussions that AC test conditions could be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis that the device will meet its timing specifications under all supported voltage conditions.

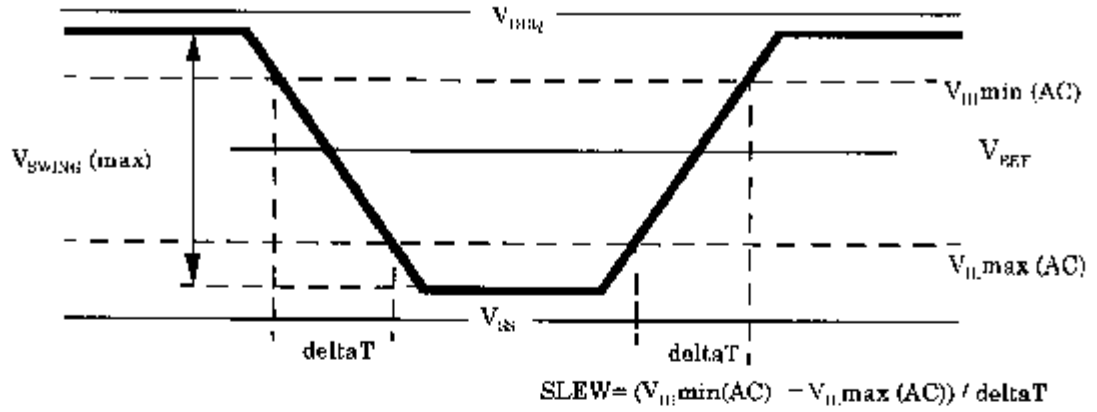

Figure 2.3 AC Input Test Signal Wave Form

3 SSTL_2 Output Buffers

3.0 Overview

This specification sets minimum requirements for output buffers in such a way that when they are applied within the range of power supply voltages specified in SSTL_2 and are used in conjunction with SSTL_2 input receivers then the input receiver specifications can be met or exceeded. The specifications are quite different from traditional specifications, where minimum values for V_{OH} and maximum values for V_{OL} are set which apply to the entire supply range. In SSTL_2, the input voltage provided to the receiver depends on the driver as well as on the termination voltage and termination resistors. Figure 3.0 shows the typical DC environment that the output buffer is presented with.

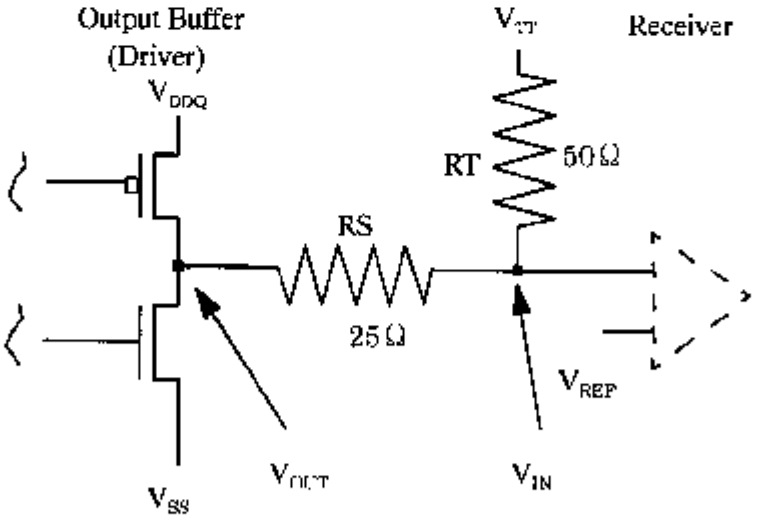

Figure 3.0 Typical Output Buffer (Driver) environment

Of particular interest here are the values V_{OUT} and V_{IN}. These values depend not only on the current drive capabilities of the buffer, but also on the values of V_{DDQ} and V_{TT} (V_{REF} is equal to V_{TT}). The important condition is that V_{IN} be at least 380mV above or below V_{REF} as a result of V_{OUT} attaining its maximum low or it's minimum high value. As will be seen later, the two cases of interest for SSTL_2 are where the series resistor RS equals 25Ω and the termination resistor RT equals 50Ω (for Class I) or 25Ω (for Class II). V_{TT} is specified as being equal to $0.5 \times V_{DDQ}$.

In order to meet the 380mV minimum requirement for Vin, a minimum of 7.6mA must be developed across RT if RT equals 50Ω (Class I) or 15.2mA in case RT equals 25Ω (Class II). The driver specification now must guarantee that these values of V_{IN} are obtained in the worst case conditions specified by this standard.

Table 3.0 Spread sheet showing how the limits of SSTL_2 circuit voltages depending on V_{DDQ}.

(For reference only)

Paramater	Units	Class I	Class I	Class I	Class II	Class II	Class II
V_{DDQ}	V	2.3	2.5	2.7	2.3	2.5	2.7
V_{TT}min	V	1.11	1.25	1.31	1.11	1.25	1.31
V_{TT}max	V	1.19	1.25	1.39	1.19	1.25	1.39
V_{REF}	V	1.15	1.25	1.35	1.15	1.25	1.35
RT	Ω	50	50	50	25	25	25
RS	Ω	25	25	25	25	25	25
Delta V_{IN}	V	0.35	0.35	0.35	0.35	0.35	0.35
Delta $V_{OUT}1$	V	0.38	0.38	0.38	0.38	0.38	0.38
Delta $V_{OUT}2$	V	0.57	0.57	0.57	0.76	0.76	0.76
Output High Drive							
Minimum Voltage at V_{IN}	V	1.57	1.63	1.77	1.57	1.63	1.77
Minimum Voltage at V_{OUT}	V	1.76	1.82	1.96	1.95	2.01	2.15
Minimum Output Current	mA	-7.6	-7.6	-7.6	-15.2	-15.2	-15.2
Maximum On Resistance	Ω	71.1	89.5	97.4	23.0	32.2	36.2
Output Low Drive							
Maximum Voltage at V_{IN}	V	0.73	0.87	0.93	0.73	0.87	0.93
Maximum Voltage at V_{OUT}	V	0.54	0.68	0.74	0.35	0.49	0.55
Minimum Output Current	mA	7.6	7.6	7.6	15.2	15.2	15.2
Maximum On Resistance	Ω	71.1	89.5	97.4	23.0	32.2	36.2

Delta $V_{OUT}1$ ($dV_{OUT}1$) is voltage across RT in Figure 3.0

Delta $V_{OUT}2$ ($dV_{OUT}2$) is total voltage across RS and RT in Figure 3.0

These values follow from an analysis of Figure 3.0 with fixed driver current. Thus, for output low voltage, $V_{IN}=V_{TT} - I \times RT$; $V_{OUT}=V_{TT} - I \times (RT+RS)$; On Resistance = $V_{TT}/I - (RT+RS)$.

As can be seen from Table 3.0 the most stringent requirements will result where V_{DDQ}= 2.3 V, since for that case the output driver transistors must have the lowest "on" resistance. If the driver outputs are sized for this condition, then for all other V_{DDQ} voltage applications, the resulting input signal will be larger than the minimum required 380mV.

3.1 SSTL_2 Class I output buffers

3.1.1 Push-pull output buffer for symmetrically single parallel terminated loads with series resistor. (V_{TT}=0.5×V_{DDQ})

Table 3.1-a Output DC current drives

Symbol	Parameter	Min.	Max.	Units	Notes
IOH (DC)	Output minimum source DC current	-7.6		mA	1,3,4
IOL (DC)	Output minimum sink DC current	7.6		mA	2,3,4

<Notes>

1. V_{DDQ} = 2.3 V; V_{OUT} = V_{DDQ} - 0.62 V
2. V_{DDQ} = 2.3 V; V_{OUT} = 0.54V.
3. The DC value of V_{REF} applied to the receiving device is expected to be set to V_{TT}.
4. The values of IOH(DC) and IOL(DC) are based on V_{DDQ} = 2.3V and V_{TT} = 1.11V. They are used to test device current drive capability which ultimately delivers acceptable noise margin for an SSTL_2 receiver. Under these conditions V_{OH} is 1.68V and V_{OL} is 0.54V. Under other conditions for V_{DDQ} and V_{TT} the typical output levels are discussed in Section 3.0 (Overview).

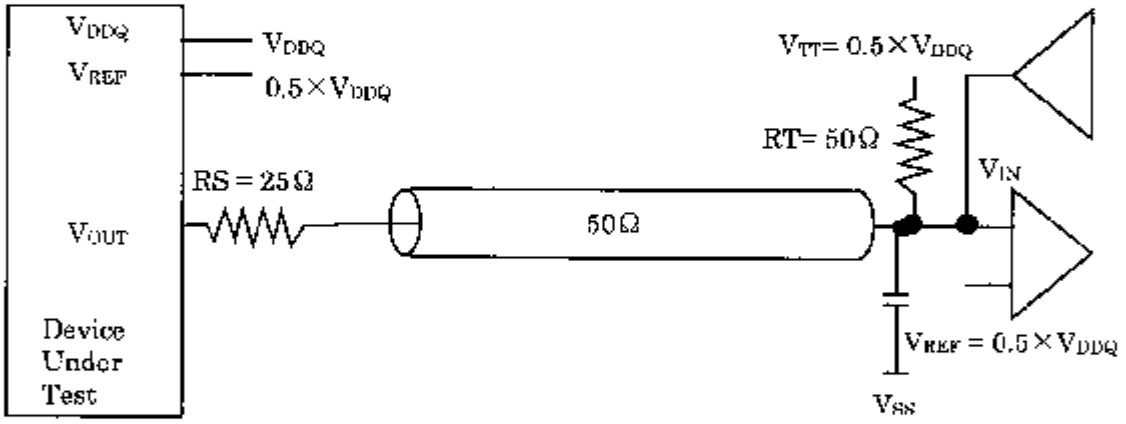

Figure 3.1 An example of SSTL_2, Class I, symmetrically single parallel terminated output load, and series resistor

3.1.2 SSTL_2 Class I output AC test conditions

This testing regimen is used to verify SSTL_2 Class I type output buffers (push-pull output buffers designed for symmetrically single parallel terminated loads with series resistor).

This section is added to set the conditions under which the driver AC specifications can be tested. The test circuit is assumed to be similar to the circuit shown in Figure 3.1. It was agreed in JEDEC discussions that AC test conditions could be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis, that the device will meet its timing specifications under all supported voltage conditions. Table 3.1-b assumes that +/- 0.38V must be developed across the 50 Ω termination resistor at V_{IN}. With a series resistor of 25Ω this translates into a minimum requirement of 0.57Volt swing relative to V_{TT}, at the output of the device.

Table 3.1-b AC test conditions

Symbol	Condition	Value	Units	Notes
V_{OH}	Minimum required output pull-up under AC test load	$V_{TT}+0.57$	V	
V_{OL}	Maximum required output pull-down under AC test load	$V_{TT}-0.57$	V	
V_{OTR}	Output timing measurement reference level	$0.5\times V_{DDQ}$	V	1

<Note>

The V_{DDQ} of the device under test is referenced.

3.2 SSTL_2 Class II output buffers

3.2.1 Push-pull output buffer for symmetrically double parallel terminated loads with series resistor ($V_{TT} = 0.5\times V_{DDQ}$)

Table 3.2-a Output DC current drive

Symbol	Parameter	Min.	Max.	Units	Notes
IOH (DC)	Output minimum source DC current	-15.2		mA	1,3,4
IOL (DC)	Output minimum sink DC current	15.2		mA	2,3,4

<Notes>

1. $V_{DDQ} = 2.3$ V; $V_{OUT} = V_{DDQ} - 0.43$V
2. $V_{DDQ} = 2.3$ V; $V_{OUT} = 0.35$V.
3. The DC value of V_{REF} applied to the receiving device is expected to be set to V_{TT}.
4. The values of IOH(DC) and V_{OL}(DC) are based on $V_{DDQ} = 2.3$V and $V_{TT} = 1.11$V. They are used to test device current drive capability which ultimately delivers acceptable noise margin for an SSTL_2 receiver. Under these conditions V_{OH} is 1.87V and V_{OL} is 0.35V. Under other conditions for V_{DDQ} and V_{TT} the typical output levels are discussed in Section 3.0 (Overview).

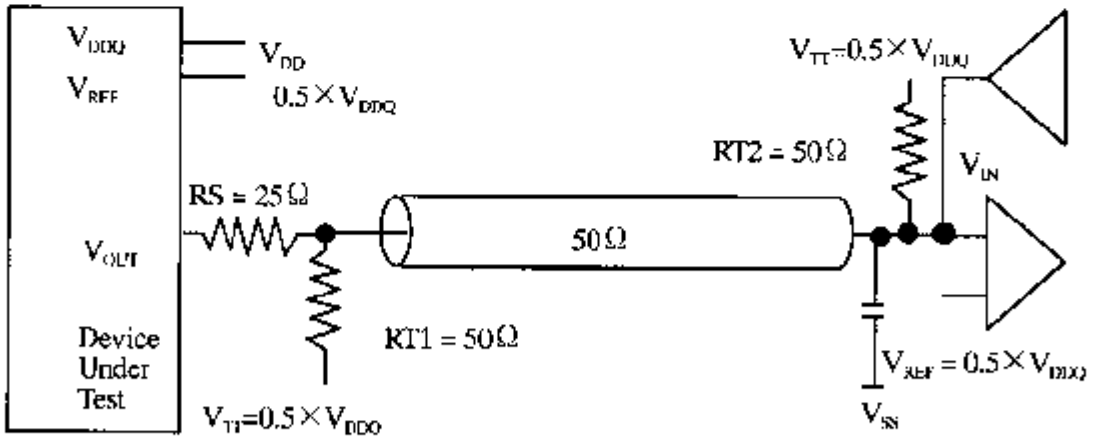

Figure 3.2 An example of SSTL_2, Class II, symmetrically double parallel terminated output load with series resistor

3.2.2 SSTL_2 Class II output AC test conditions

This testing regimen is used to verify SSTL_2 Class II type output buffers (push-pull output buffers designed for symmetrically double parallel terminated loads with series resistor).

This section is added to set the conditions under which the driver AC specifications can be tested. The test circuit is assumed to be similar to the circuit shown in Figure 3.2. It was agreed in JEDEC discussions that AC test conditions could be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis, that the device will meet its timing specifications under all supported voltage conditions. Table 3.2-b assumes that +/- 0.38V must be developed across the effectively 25Ω termination resistor at V_{IN}. With a series resistor of 25Ω this translates into a minimum requirement of 0.76Volt swing relative to V_{TT}, at the output of the device.

Table 3.2-b AC test conditions

Symbol	Condition	Value	Units	Notes
V_{OH}	Minimum required output pull-up under AC test load	V_{TT} + 0.76	V	
V_{OL}	Maximum required output pull-down under AC test load	V_{TT} - 0.76	V	
V_{OTR}	Output timing measurement reference level	$0.5 \times V_{DDQ}$	V	1

<Note>

The V_{DDQ} of the device under test is referenced.

4. Other Application (For reference only)

The specifications for Class I and II were based on an environment comprising both series and parallel terminating resistors. In this non binding section we will show some derived applications. Clearly it is not the intention to show all possible variations in this standard.

4.1 Push-pull output buffer for unterminated loads

In many applications where interconnections are short, there is no need for any termination at all. An example of this is shown in Figure 4.1 This application can be served by a Class I or Class II type buffer and an SSTL_2 type receiver.

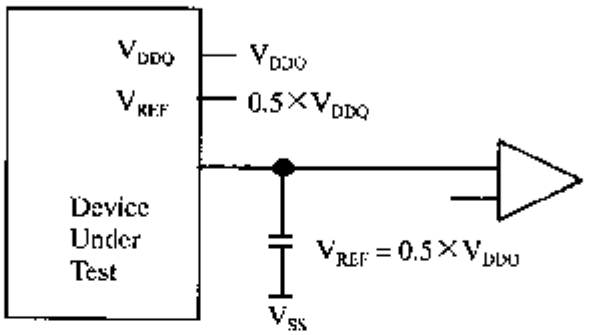

Figure 4.1 An example of SSTL_2 un-terminated output load

4.2 Push-pull output buffer for symmetrically single parallel terminated loads ($V_{TT} = 0.5\times V_{DDQ}$)

Sometimes the system application requires longer transmission lines that will only be terminated at one end. An example of this may be address drivers on a memory board. This application can also be served with a Class I or Class II type buffer and an SSTL_2 receiver. An example is shown in Figure 4.2.

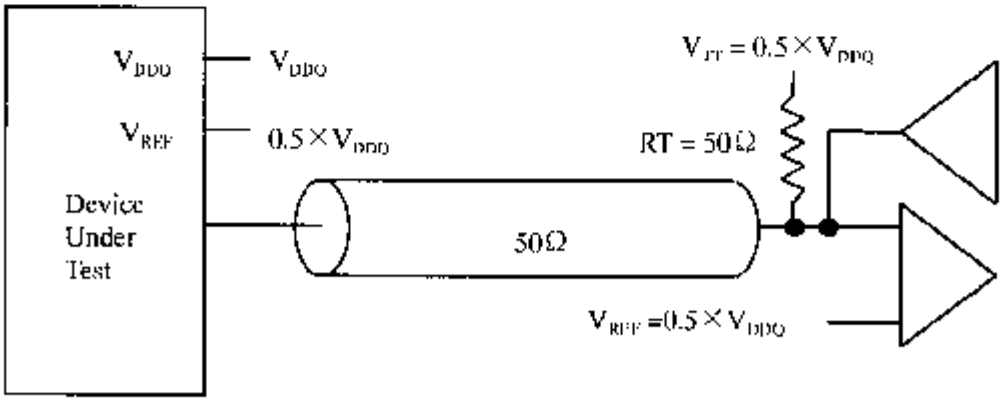

Figure 4.2 An example of SSTL_2, Class I or Class II, buffer with symmetrically single parallel terminated output loads.

4.3 Push-pull output buffer for externally source series terminated loads

In other applications the system designer may wish to terminate at the signal source rather than at the end of the transmission line. One advantage of this approach is that there is no need for a V_{TT} power supply. This application may again be served with a Class I or Class II type buffer and SSTL_2 receiver. An example is shown in Figure 4.3. In this example a Class II type buffer might be preferred since it comes closer, in conjunction with the series resistor, to match the characteristic impedance of the transmission line.

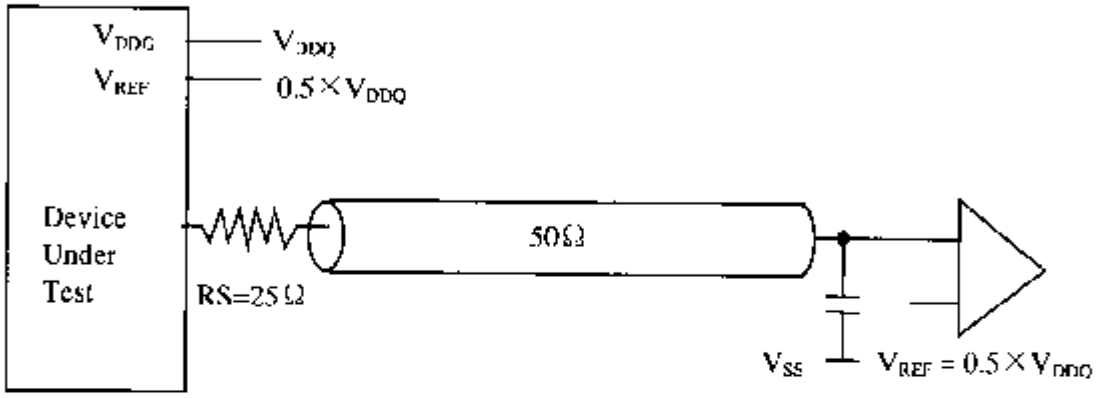

Figure 4.3 An example of SSTL_2, Class I or Class II, Externally Source Series terminated output load

4.4 Push-pull output buffer for symmetrically double parallel terminated loads ($V_{TT} = 0.5 \times V_{DDQ}$)

Finally, the system designer may require a bus system which must be terminated at both sides. However, the drivers are connected directly onto the bus so there are no stubs present. In that case, the designer may decide to eliminate the series resistors entirely. This application can be implemented using a Class I or Class II driver and SSTL_2 receiver. However a Class II buffer would dissipate more power due to its larger current drive and thus might require special cooling. An example is shown in Figure 4.4.

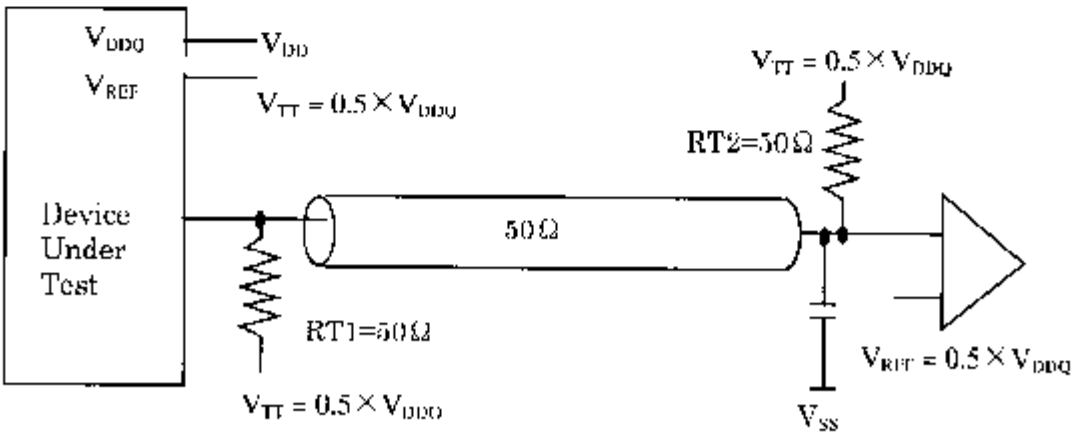

Figure 4.4 An example of SSTL_2, Class I, buffer with symmetrically double parallel terminated output load

EXPLANATORY NOTES

1. Objectives of Establishment

This standard has been established as a related standard derived from "Stub Series Terminated Logic for 3.3V (SSTL_3)" established in March, 1996, aiming to separate bus from moderately long stub through the external serial resistance at the 2.5V memory module, memory board, etc., perform the small signal amplitude operation by connecting to terminated voltage through the parallel resistance, and adjust impedance to establish noise margin and perform the low-power and high-speed operation. This standard defining each provision for the output driver and the input receiver, is established as the 100 – 200MHz high-speed interface standard along with the faster MPU.

2. Process of Discussion

When "Stub Series Terminated Logic for 3.3V (SSTL_3)" was established in March, 1996, the development to shift the system power supply voltage from 3.3V to 2.5V has already started along with process technologies development for faster memory devices.

At the time, this standard was proposed as the voltage scaling of SSTL_3 as the related standard derived from SSTL_3 interface, and submitted to the JEDEC JC-16 Low Voltage Operation and Interface Committee ("JEDEC" hereafter), the sub-organization of the Electronic Industries Association in U.S. in September, 1996.

While the JEDEC discussion continued, it was proceeded to standardize the interface specifications used for faster memories such as DDR SDRAM, SLDRAM, etc. devices, and review the interface performance through simulations in cooperation with JEDEC. The final standard draft was agreed with EIAJ and JEDEC, submitted to JEDEC in September, 1997, and passed the JEDEC JC-16 Committee in December. SSTL_2 standard is the collaborated standard of EIAJ and JEDEC.

3. Members of Committee

This standard was discussed mainly by Memory Subcommittee and IC Low Voltage operation subcommittee on Semiconductor Standardization Committee/Integrated Circuit G (group). The members are as shown below.

<Semiconductor Standardization Committee>

Chairman	Mitsutoshi Ito	NEC Corp.

<Semiconductor Standardization Committee/Integrated Circuit G>

Chief Examiner	Motoo Nakano	Fujitsu Ltd.

<Memory Subcommittee>

Chief Examiner	Yoshiharu Nishiwaki	Oki Electric Industry Co., Ltd.
Vice-Chief Examiner	Mitsuo Higuchi	Fujitsu Ltd.
Member	Young Jun Roh	LG Japan, Inc.
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	Seijin Kim	Samson Japan Corp.
	Soichiro Kamei	Texas Instruments Japan Ltd.
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	Kazutami Arimoto	Mitsubishi Electric Corp.
	Hideki Hayashi	ROHM Ltd.
Special Member	Mitsuo Yasuhira	Matsushita Electronics Corp.
	Miwa Menma	NEC Corp.
	Yoshitomo Asakura	NEC Corp.

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Member	Terunori Tajima	Oki Electric Industry Co., Ltd.
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