Standard of Electronic Industries Association of Japan

EIAJ ED-5514

Processor Enhanced Memory Module (PEMM)

Standard for Processor Enhanced Memory Module Functional Specifications

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Basava Technology

1 Scope

This document defines the standard of operation of the PEMM (Processor Enhanced Memory Module).

The target for this standard is all DIMMs, including 144 pin SO-DIMMs and 168 pin DIMMs, containing either EDO or SDRAM(Refer to JEDEC Standard JESD21-C 4.5.1, 4.5.3~7).

Future proposals may include but may not be limited to DDR-SDRAM.

This document suggests changes to the supporting memory controller, motherboard, and the DIMM itself. This document assumes that the system has at least two DIMM sockets, and two physical banks of memory can reside on a single DIMM.

2 Architectural Overview

This architecture (Basava Technology*) is a new computer architecture and system concept that enables an end user to easily enhance a system's performance and add new functions by just plugging in a memory expansion module. For example, a user can transform his/her PC or Notebook computer into a high-performance multimedia computer capable of executing the fastest fax/modem, high polyphony CD-quality music synthesis, DVD decoding, and user interface functions like speech-recognition and Text-to-Speech by just plugging in a memory expansion module with one or more processors embedded in it. The hardware memory-expansion module is referred to as the PEMM.

Technically, this architecture addresses parallel processing in the memory space of a Central Processing Unit (CPU). The CPU, also referred to as the Main Processing Unit (MPU) is the main processor in the system. For example, in the case of PCs it would be an Intel CPU, in the case of Sun workstations it would be a SPARC RISC, and so on. Parallel processing is obtained by adding one or more processors such as Digital Signal Processors (DSPs) but could also be an additional CPU. The processor(s) embedded on the memory module is referred to as a Memory Module Processing Unit (MMPU).

* This technology includes hardware and software architectures for the PEMM.

2.1 Benefits

This architecture offers several significant benefits:

(a) It offers the ability to Plug & Play since adding the parallel processor is as easy as expanding the memory of a CPU. It relies on standardized interfaces which are often standardized by organizations like IEEE, JEDEC etc.

(b) It offers the highest possible bandwidth between the CPU and coprocessor at any given time and technology.

(c) It offers a bus-independent, and therefore a host-independent solution for PCs, PDAs, workstations and other computer systems.

(d) It reduces system cost by sharing system memory.

(e) It provides a framework for easily scaling up the processing power of the system; an existing uniprocessor system can be transformed into a scalable, multiprocessing system

(f) Customers do not have to change their product platforms in order to get/offer new, value-added functions.

2.2 Motivation

(a) Bandwidth between CPU and Coprocessor is a key parameter that Multimedia applications appear to quickly consume

(b) Multimedia applications are limited by computational-speed , memory-size and bandwidth

(c) Hardware Upgrade: no simple or standard way of scaling up computing power

(d) Many co-processing applications are memory-intensive, well-structured and amenable to partitioning. Small operations or routines applied to a large set of data e.g. search techniques

(e) Transparent upgrade of system performance:
- Backward compatible with existing architecture

(f) Differentiation via type of module added

2.3 Rationale for this standard

This standard allows DIMMs not only to contain standard memory, but also enables a simple memory-mapped co-processing interface.

In this standard, we are requesting two new DIMM card-edge interface signals, /MWAIT and /MIRQ. Since the memory on the module is shared between the MMPU and the host CPU, arbitration is required. This is accomplished by the logic on the module. The /MWAIT signal allows the shared memory to be given back to the CPU transparently when it accesses the module. Instead of dual-ported memories, this signal /MWAIT enables the use of standard, single-port DRAMs.

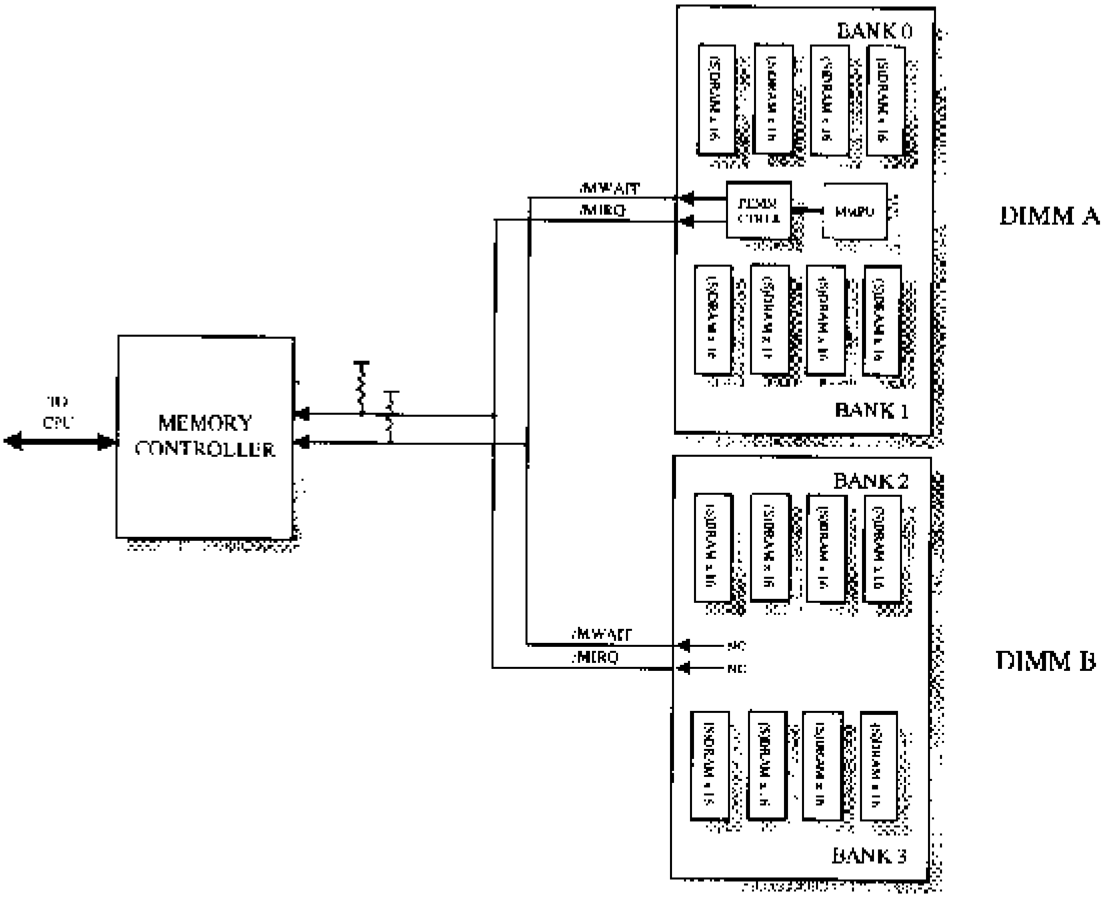
In a typical mode of operation, the MMPU needs to signal the CPU after completing the task it was asked to execute. With an interrupt signal, /MIRQ supported at the DIMM interface, this becomes possible.

Detection of the PEMM is required and shall be achieved through supplements to the existing SPD (Serial Presence Detect) data.

Figures in sections 2.4 and 2.5 show a system level and a PEMM bank-level block diagram, respectively.

Section 4 describes in detail the information required for standardization, /MWAIT and /MIRQ pin definitions and functions, and the SPD table enhancements.

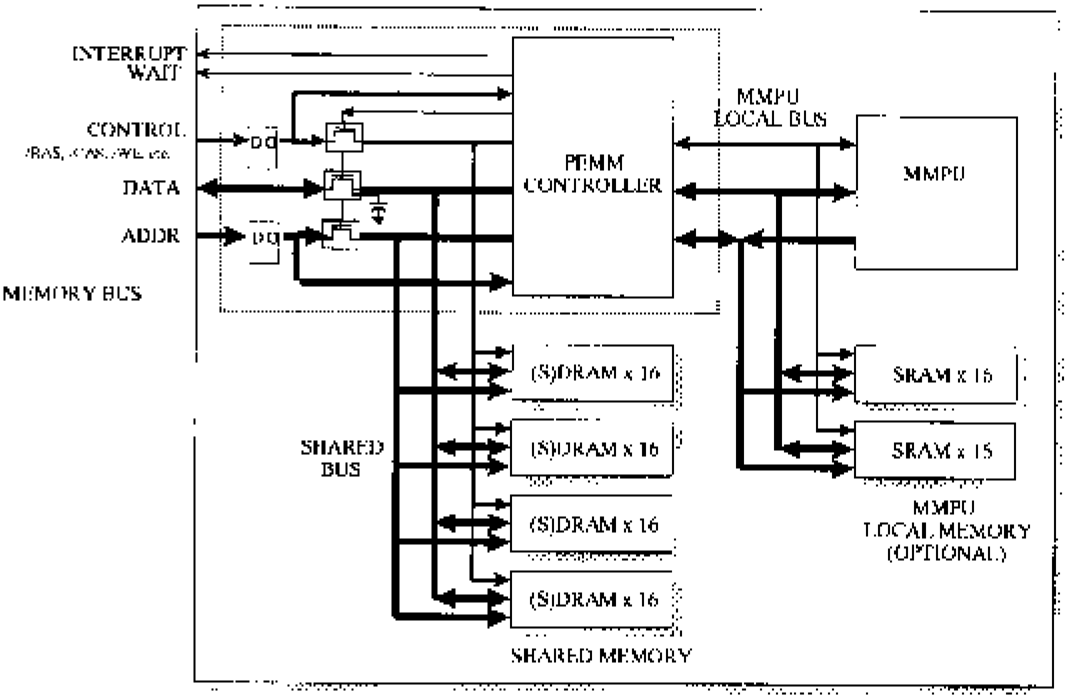
2.4 Memory system block diagram (DIMM: a PEMM)



The figure above shows a typical block diagram for a 2-DIMM system using a PEMM. In this figure, DIMM A is a PEMM, and DIMM B is a standard memory module. As can be seen, the /MWAIT and /MIRQ signals shall be driven by the PEMM Controller(s) and wire ORed on the motherboard before being received by the Memory Controller.

Systems may contain any number of PEMMs mixed with standard DIMMs. The interface for /MWAIT and /MIRQ are backward compatible, thus functioning properly with today's DIMMs that do not drive these signals.

2.5 PEMM block diagram



The PEMM shall contain the following components:

(a) A bank of shared memory, either EDO DRAM or SDRAM

(b) An MMPU with its own local SRAM (optional)

(c) A PEMM Controller ASIC which has the option of containing crossbar switches and or registers for the memory bus I/O signals.

The PEMM Controller has the following duties:

(a) Generate /MWAIT and /MIRQ signals

(b) Control switching of bus traffic to (S)DRAM from MMPU and CPU

(c) Provide address mapping from MMPU linear address to a DRAM type Row/Column address

(d) Contain setup registers for operation of PEMM

Generally, MMPUs shall be added to DIMMs on a bank-by-bank basis. In other words, memory bank 0, controlled by /RAS0 or /S0 may contain an MMPU while the memory bank controlled by /RAS1 or /S1 may remain unchanged. This allows for easy segmentation of the hardware, and allows the user to expand incrementally if desired.

Along with the shared bank, the PEMM may also contain a 2nd bank of memory, which is not shared. A single DIMM of this type would add one standard bank of DRAM and one Processor Enhanced bank with the hardware described above.

The memory I/O signals on the module shall be switched "in" or "out" depending on which processor, (the CPU or the MMPU) currently owns the bus. The CPU will always maintain highest priority, thus necessitating the /MWAIT signal to allow the MMPU time to relinquish the memory bus back to the CPU when requested.

When the CPU is disconnected from a memory bank containing an MMPU, "dummy loads" shall be switched on to the data lines to keep the loading constant from the CPU's point of view.

3 PEMM Modes of Operation

The PEMM shall operate in three basic modes:

(a) Standard Mode

(b) Configuration Mode

(c) Smart Mode.

3.1 Standard mode

Standard Mode is the default power-up mode of the module. In this mode, the module's smart functions are disabled and the module appears only as standard memory to the CPU.

3.2 Configuration mode

The Configuration Mode is entered when the CPU writes a specific pattern to a pre-determined memory address on the PEMM. This address is defined by the SPD ROM and the data pattern is hard-coded into the PEMM Controller. The PEMM Controller shall snoop the bus, monitoring accesses to this specific location. If the PEMM Controller detects that through several consecutive accesses that the proper data or "signature" was written, then the Configuration mode is immediately entered.

Once the Configuration Mode is active, a portion of the PEMM's memory space is replaced with setup registers which can be read from or written to by the main CPU. These registers provide an interface to the control of the PEMM, status monitoring of the PEMM, and data/program upload/download to the PEMM. Once configuration is complete, the CPU can switch the PEMM into the Smart Mode via access to one of the control registers.

Specific details of the Configuration Mode, as well as all necessary software/driver controlled memory-mapped setup registers for the PEMM are beyond the scope of document.

3.3 Smart mode

After the Smart Mode is entered, the MMPU on the PEMM begins execution. The configuration registers are still mapped into the main memory space allowing the CPU and the MMPU to communicate after execution begins. The MMPU also has the ability to interrupt the main CPU when the Smart Mode is active. This interrupt may be used to alert the CPU when a specific PEMM task is complete.

The Smart Mode and/or Configuration Mode can be exited (i.e. entering Standard Mode) at any time at the main CPU's command.

4 Hardware Structure

This section describes PEMM hardware structure information necessary for standardization. This standard has the following impact on JEDEC STANDARD DIMM modules:

(a) Two new output signals shall be added to the DIMM, /MWAIT and /MIRQ.

(b) The DIMM shall contain (S)DRAM, MMPU, and the PEMM Controller and similar logic.

(c) The SPD data must be appended to provide PEMM specific information

4.1 New signal function

Function	Description
WAIT	This function allows the PEMM to indicate to the memory controller that the DRAM in the specific bank is currently busy. Once the memory controller requests a memory access of this bank, this signal will only be asserted for the amount of time required for the PEMM to relinquish the shared memory back to the controller. Further accesses to the same page of this bank will incur no further delays.
INTERRUPT	This function allows the PEMM to indicate to the memory controller that a specific task is complete, and that the main CPU should be alerted.

4.2 New signal description

Signal	144-Pin SO-DIMM Pin #	168 Pin DIMM Pin #	Type	Description
/MWAIT	77	61	O/Z LVTTL/TTL	**Memory WAIT flag.** This is an active-low signal driven by the *currently* accessed module indicating that the accessed bank of DRAM is temporarily busy. PEMMs that are not being accessed shall hold this signal in the high-Z state. For compatibility with modules that do not drive this signal, it shall be pulled up on the motherboard or in the memory controller. See further description and timing diagrams below.
/MIRQ	78	145	O (Open Drain) LVTTL/TTL	**Memory Interrupt ReQuest.** This is a signal indicating that a MMPU on this PEMM is requesting an interrupt of the main CPU. A low level on this signal indicates that an interrupt request is in progress. Since this signal is open-drain, several PEMMs may be connected to and drive this signal at the same time. For compatibility with modules that do not drive this signal, it shall be pulled up on the motherboard or in the memory controller. See further description and timing diagrams below.

4.3 Serial presence detect table entries

4.3.1 Table of superset memory types

Superset Mem. Type	Fundamental memory type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	See
Reserved		0	0	0	0	0	0	0	0	N/A
ESDRAM	Sync DRAM	0	0	0	0	0	0	0	1	Appendix #
TBD	TBD	0	0	0	0	0	0	1	0	Appendix #
Processor Enhanced Memory—Basava Technology	FDO DRAM	0	0	0	0	0	0	1	1	Appendix #
Processor Enhanced Memory—Basava Technology	Sync DRAM	0	0	0	0	0	1	0	0	Appendix #
TBD		0	0	0	0	0	1	0	1	TBD
TBD		0	0	0	0	0	1	1	0	TBD
.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.
TBD		1	1	1	1	1	1	0	1	TBD
TBD		1	1	1	1	1	1	1	0	TBD
TBD		1	1	1	1	1	1	1	1	TBD

<Note> Appendix # will be assigned by JEDEC JC-42.5 committee.

4.3.2 Specific PD's for superset type processor enhanced memory

4.3.2.1 Address map

The following is the SPD address map for the Processor Enhanced Memory superset type. It describes where the individual LUT-Entrics/bytes will be held in the serial EEPROM:

Byte Number	Function Described	Notes
60-59	Processor Bus Controller; Generic Part Number (JEDEC managed Look Up Table)	
58	Processor Bus Controller: Rev code (for information purposes only – system should disregard)	
57-54	Processor Bus Controller: Power-up address location	
53-52	Processor 1: Generic Part Number (JEDEC managed Look Up Table)	
51	Processor 1: Rev code (for information purposes only – system should disregard)	
50-49	Processor 1: Actual Clock Cycle time	
48	Processor 1: Local Memory Size	
47	Processor 1: Bank Location	
46-45	Processor 2: Generic Part Number (JEDEC managed Look Up Table)	
44	Processor 2. Rev code (for information purposes only – system should disregard)	
43-42	Processor 2: Actual Clock Cycle time	
41	Processor 2: Local Memory Size	
40	Processor 2: Bank Location	

4.3.2.2 Bytes 60-59

Processor Bus Controller Generic Part Number: This field describes the part number for the Bus Controller device on the Processor Enhanced Memory Module. Since there is limited SPD space in the superset range (bytes 36-60), this data shall not follow the same format as bytes 73-90, but will be on a Look Up Table basis. This SPD spec will not attempt to present a decode table for device part numbers, instead JEDEC will administer and manage the Look Up Table entries for this field.

4.3.2.3 Byte 58

Processor Bus Controller Rev. Code: This refers to the Bus Controller revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte. This field is intended for manufacturer's information only, thus the system should disregard the contents of this byte.

4.3.2.4Bytes 57-54

Processor Bus Controller Power-Up Address Location: These four bytes represent the decode values for the starting location of the Bus Controller's "Smart Registers" upon power-up. The format for these bytes is as follows:

Incoming Row/Column address	Byte 57	Byte 56	Byte 55	Byte 54

Row = 0000(h),
Column = 0000(h)
	00h	00h	00h	00h

Row = 0000(h),
Column = 0001(h)
	00h	00h	00h	01h

:	:	:	:	:

Row = ABCD(h),
Column = 1234(h)
	ABh	CDh	12h	34h

:	:	:	:	:

Row = FFFF(h),
Column = FFFF(h)
	FFh	FFh	FFh	FFh

4.3.2.5Bytes 53-52

Processor 1 Generic Part Number: This field describes the part number for the first processing device on the Processor Enhanced Memory Module. Since there is limited SPD space in the superset range (bytes 36-60), this data shall not follow the same format as bytes 73-90, but will be on a Look Up Table basis. This SPD spec will not attempt to present a decode table for device part numbers, instead JEDEC will administer and manage the Look Up Table entries for this field.

4.3.2.6Byte 51

Processor 1 Rev. Code: This refers to the revision code for the first processing device. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte. This field is intended for manufacturer's information only, thus the system should disregard the contents of this byte.

4.3.2.7Bytes 50-49

Processor 1 Actual Clock Cycle Time: These bytes indicate the actual clock cycle time for the first processing device. Each digit for the cycle time "ABC.D ns" is coded in BCD format:

Example Cycle Time	A: Byte 50 high nibble	B: Byte 50 low nibble	C: Byte 49 high nibble	D: Byte 49 low nibble
5.0 ns	0000b	0000b	0101b	0000b
10.5 ns	0000b	0001b	0000b	0101b
33.4 ns	0000b	0011b	0011b	0100b
100.2 ns	0001b	0000b	0000b	0010b
:				:

4.3.2.8Byte 48

Processor 1 Local Memory Size: This field describes the size of the local memory available to the first processing device. The format of this byte is governed by the following equation:

Memory Size = 2 exp (Byte 48), except when (Byte 48) = 0. See table below:

Memory Size	Byte 48
0 bytes	00h
:	:
1K Bytes	0Ah
2K Bytes	0Bh
4K Bytes	0Ch
8K Bytes	0Dh
16K Bytes	0Eh
32K Bytes	0Fh
64K Bytes	10h
128K Bytes	11h
256K Bytes	12h
512K Bytes	13h
1M Byte	14h
2M Byte	15h
:	:

4.3.2.9Byte 47

Processor 1 Bank Location: This field indicates the module bank location for the first processor at power-up time. The format for this byte is shown below:

Bank Location	Byte 47
Bank 0	00h
Bank 1	01h
:	:

4.3.2.10 Bytes 46-45

Processor 2 Generic Part Number: This field describes the part number for the second processing device on the Processor Enhanced Memory Module. Since there is limited SPD space in the superset range (bytes 36-60), this data shall not follow the same format as bytes 73-90, but will be on a Look Up Table basis. This SPD spec will not attempt to present a decode table for device part numbers, instead JEDEC will administer and manage the Look Up Table entries for this field.

4.3.2.11 Byte 44

Processor 2 Rev. Code: This refers to the revision code for the second processing device. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte. This field is intended for manufacturer's information only, thus the system should disregard the contents of this byte.

4.3.2.12 Bytes 43-42

Processor 2 Actual Clock Cycle Time: These bytes indicate the actual clock cycle time for the second processing device. Each digit for the cycle time "ABC.D ns" is coded in BCD format:

Example Cycle Time	A: Byte 43 high nibble	B: Byte 43 low nibble	C: Byte 42 high nibble	D Byte 42 low nibble
5.0 ns	0000b	0000b	0101b	0000b
10.5 ns	0000b	0001b	0000b	0101b
33.4 ns	0000b	0011b	0011b	0100b
100.2 ns	0001b	0000b	0000b	0010b
:	:	:	:	:

4.3.2.13 Byte 41

Processor 2 Local Memory Size: This field describes the size of the local memory available to the second processing device. The format of this byte is governed by the following equation:

Memory Size = 2 exp (Byte 41), except when (Byte 41) = 0. See table below:

Memory Size	Byte 41
0 bytes	00h
:	:
1K Bytes	0Ah
2K Bytes	0Bh
4K Bytes	0Ch
8K Bytes	0Dh
16K Bytes	0Eh
32K Bytes	0Fh
64K Bytes	10h
128K Bytes	11h
256K Bytes	12h
512K Bytes	13h
1M Byte	14h
2M Byte	15h
:	:

4.3.2.14 Byte 40

Processor 2 Bank Location: This field indicates the module bank location for the second processor at power-up time. The format for this byte is shown below:

Bank Location	Byte 40
Bank 0	00h
Bank 1	01h
:	:

4.4 Supplemental information

This section describes supplemental information for the hardware structure of the PEMM and is not currently a part of the proposed standard. Items in this section should be viewed only as design suggestions for PEMM providers. PEMM providers are free to add innovation to this concept, however PEMM providers must be responsible for proper end-product operation and full DIMM standard compliance.

4.4.1 PEMM differences from a standard DIMM (reference only)

A typical PEMM would differ from a standard DIMM in the following ways:

(a) The PEMM will contain an MMPU

(b) The MMPU may have on-board local memory

(c) The PEMM will contain at least one bank of shared memory

(d) The PEMM will contain a PEMM Controller or similar logic to handle the arbitration of memory access traffic from the CPU and the MMPU

Additions to this list, or specific details of how each of these components are implemented are left up to each individual PEMM provider.

4.4.2 Power-on reset (reference only)

Because the memory bus contains no power-on reset signal, the PEMM will include necessary devices to generate an on-board power-on reset signal.

4.4.3 Clock generation (reference only)

The PEMM will include an onboard crystal for the MMPU when no clock source is available. A PLL will be used with either the onboard crystal or the CPU clock to generate all desired onboard clocks. The PLL will be software controllable, and configured by the PEMM Controller. This will allow one standard PEMM to work efficiently in several different systems running at different speeds.

4.4.4 Bus switching (reference only)

Switching will be done with "zero delay" crossbar switches, also using registers if needed. These crossbars (and registers) may be placed exterior or interior to the PEMM Controller.

When only crossbars are used, the memory access time, tAC, will be slightly increased due to the propagation delay of the crossbar switches. PEMM designers must consider these delays and their effect on memory data setup and hold times.

4.4.5 Capacitance (reference only)

The addition of the PEMM Controller will add capacitance to the memory bus. As seen in the figure in section 2.5, if the PEMM Controller contains the bus switches (crossbars), then the capacitance can be controlled much more accurately than if the crossbar switches reside exterior to the PEMM Controller. In either case, however, dummy loads must be implemented on the data lines when the CPU is "cut off" from the memory. This will balance the load, keeping the exterior bus loading fairly constant.

If it is assumed that the PEMM Controller WILL NOT contain the necessary switching logic, then the following signals will not exceed the following increases in loading:

Signal	CPU Disconnected (Switch off) "C_{OFF}"	CPU Connected (Switch on) "C_{ON}"
DQ signals[3]	C_{DUMMY}[1] + 3.5pF	C_{MEMORY}[2] + 10.5pF
/RAS(n), /CAS(n), /Sn, Addr. Signals, /WE, CKEn, DQMn[4]	8.5Pf	C_{MEMORY}[2] + 13.5pF
One CKn line[5]	C_{MEMORY}[2] + 5pF	C_{MEMORY}[2] + 5pF
Serial PD lines[6]	Unchanged	unchanged

<Note>

1 Dummy load will be sized for each signal so that COFF = CON.

2 Memory load corresponds to standard DRAM CIN or CIO value. CIN typ. is 5pF. CIO typ. is 7pF.

3 DQ signals will experience crossbar loading (3.5pF) at all times + PEMM Controller loading (7pF) when connected.

4 These signals are "snooped", thus always connected to PEMM Controller (5pF) and always connected to crossbar (3.5pF). When the switch is "on", a 2nd PEMM Controller load will add 5pF.

5 The PEMM Controller will add one load to one input clock line (5pF).

6 Serial PD lines are not connected to Processor Enhanced Logic.

4.4.6 Power consumption (reference only)

It must be noted that MMPU supply current can vary with clock speed, usage, and device technology. Maximum PEMM supply current must not exceed specifications for end system environment or rated maximum of DIMM connector.

4.4.7 Impact to memory controller (reference only)

(a) Two new signals will be added, /MWAIT and /MIRQ.

(b) The memory controller will include the necessary logic to comprehend the added signals above.

(c) The memory controller will include PEMM setup registers. See section 5.1.1.

4.4.8 Impact to motherboard (reference only)

(a) Pull-up resistors will be included (if not pulled-up in memory controller) for /MWAIT and /MIRQ signals.

(b) Two new signal etch runs will be added, /MWAIT and /MIRQ.

(c) These signals will be connected to the Memory Controller and WIRE-ORed to all DIMM sockets.

5 Electrical Interface

5.1 Wait protocol

The protocol described in the following sections must be followed by the memory controller when the currently accessed bank of memory has been placed in the "Smart" (shared) Mode. Standard DIMMs or banks that are not in the Smart Mode need not abide by this protocol.

5.1.1 Memory controller setup registers

The Memory Controller shall be aware of which memory banks are in the Smart Mode by the contents of the Memory Controller setup registers. These registers shall be IO memory mapped and updated in real time by the hardware driver for the PEMM. Memory banks that are in the Standard Mode need not follow any special protocol, and may be treated as standard memory.

For the SDRAM case, the memory controller must also be aware of, and agree with the PEMM Controller for the starting point of MMPU eligibility to access the shared memory. Setup registers shall be included in the memory controller for this purpose. See section 5.1.3.1 for further details.

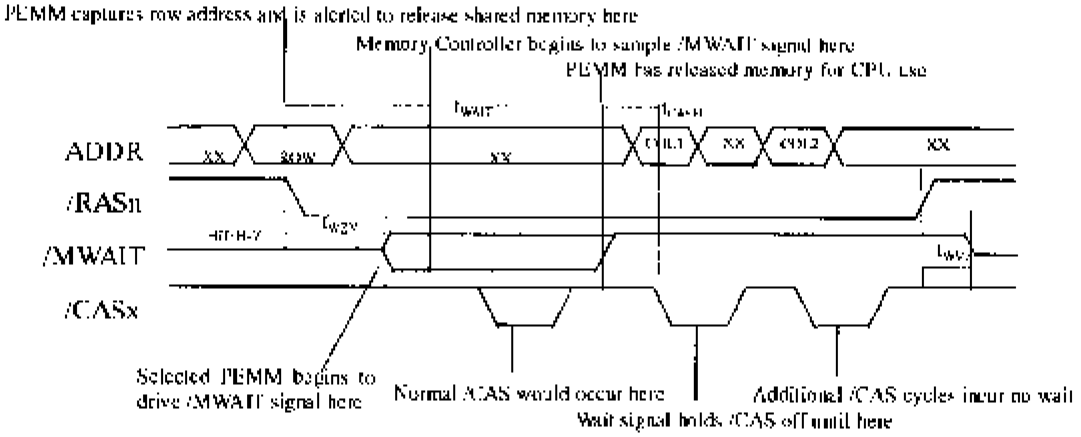
5.1.2 Wait protocol-EDO DRAM

For the EDO DRAM case, the memory controller must begin to sample the /MWAIT signal directly after each falling edge of /RASn to determine if bank "n" currently accessed is busy. If the currently accessed bank is busy, then the memory controller must wait a short amount of time until this flag is driven back high indicating that the PEMM has relinquished the shared memory back to the controller. At this point, the controller may assert /CAS. The MMPU may only begin to use bank "n" of shared memory when /RASn is high, thus further memory controller accesses to the same page of this bank will incur no wait. If all /RASn inputs to the PEMM are high, then the PEMM shall hold the /MWAIT signal in the High-Z state.

<Note>

In systems with multiple PEMMs, contention on the /MWAIT signal must be avoided by assuring that the memory controller drive its /RASn signals low to only one PEMM at a time. Thus, /RAS only refreshes must be staggered on a module-by-module basis. Staggering need not be done for CBR refreshes, as the PEMM will hold the /MWAIT signal in the High-Z state during a CBR refresh.

5.1.2.1Wait timing - READ or WRITE (EDO DRAM)


PEMM captures row address and is alerted to release shared memory here
Memory Controller begins to sample /MWAIT signal here
PEMM has released memory for CPU use
tWAIT
tRASH
ADDR
XX
ROW
XX
COL1
XX
COL2
XX
/RASn
tWZV
HI-Z
/MWAIT
tWVZ
/CASx
Selected PEMM begins to drive /MWAIT signal here
Normal /CAS would occur here
Wait signal holds /CAS off until here
Additional /CAS cycles incur no wait

5.1.2.2Timing data for figure 5.1.2.1 (reference only)

Parameter	Description	MIN	TYP	MAX
t_{WAIT}[1]	/RASn low to /MWAIT high	T_{WAV}(min)	-	t_{RL2RL2}
t_{WZV}	/RASn low to /MWAIT driven	TBD[2]	TBD[2]	7 ns
t_{WVZ}	/RASn high to /MWAIT High-Z	TBD[2]	TBD[2]	7 ns
t_{CASH}	Required /CAS high time after /MWAIT high			0 ns

<Note>

1 This parameter is dependent upon the speed of the DRAM in this bank. JEDEC Symbol t_{RL2RL2} is the DRAM read or write cycle time. The PEMM Controller shall be programmable to control/accept a variety of memory speeds.

2 This value is dependent upon the PEMM Controller. MIN and TYP times are TBD but the MAX time is a design requirement.

5.1.3 Wait protocol - SDRAM;

For the SDRAM case, /MWAIT is synchronous with the memory bus clock. The PEMM will drive the /MWAIT signal high or low for each cycle following a NOP command cycle. If /MWAIT is sampled as low, then after further NOP commands, /MWAIT will be driven high indicating that the PEMM has relinquished the shared memory back to the controller. At this point, the controller may begin (or continue) a memory cycle and suffer no further delay. A bank "n" of SDRAM may only become busy when it is "eligible" for MMPU access. A NOP command will always end the period of eligibility, requesting main CPU access of the memory. See the "eligibility" section and timing diagrams below. If no NOP commands are being applied to the PEMM, then the PEMM shall hold the /MWAIT signal in the High-Z state.

To avoid contention on the /MWAIT signal, the memory controller must only issue NOP commands to one PEMM at a time. Since the DSEL command is interpreted the same as a NOP command by all SDRAMs, this stipulation should not be a problem for the design of the memory controller.

5.1.3.1Memory eligibility for MMPU access (SDRAM only)

Unlike conventional DRAMs, synchronous DRAMS have 2 or 4 internal banks. Because of this feature, the memory controller has the ability to open 2 or 4 pages at a time and instantly switch between them for read and write access. This feature makes the eligibility of MMPU access to the memory slightly more complicated than with conventional DRAMs. A set of rules for eligibility must be defined.

The shared memory shall be eligible for MMPU access regardless of the state (open or closed) of each SDRAM internal bank. This allows the MMPU to break memory controller pages that are open, accessing the memory whenever the memory controller is not currently busy with a memory transaction. The "Region of Eligibility" will begin, making the memory eligible for MMPU access, only when ALL of the following conditions are met:

(a) All CPU burst read or write cycles are complete (either by self-completion or by the issuing of a Burst-Stop (BST) command)

(b) All CPU precharge cycles are complete

(c) All CPU refresh commands are complete

(d) t_{E}, the required number of DSEL cycles has occurred

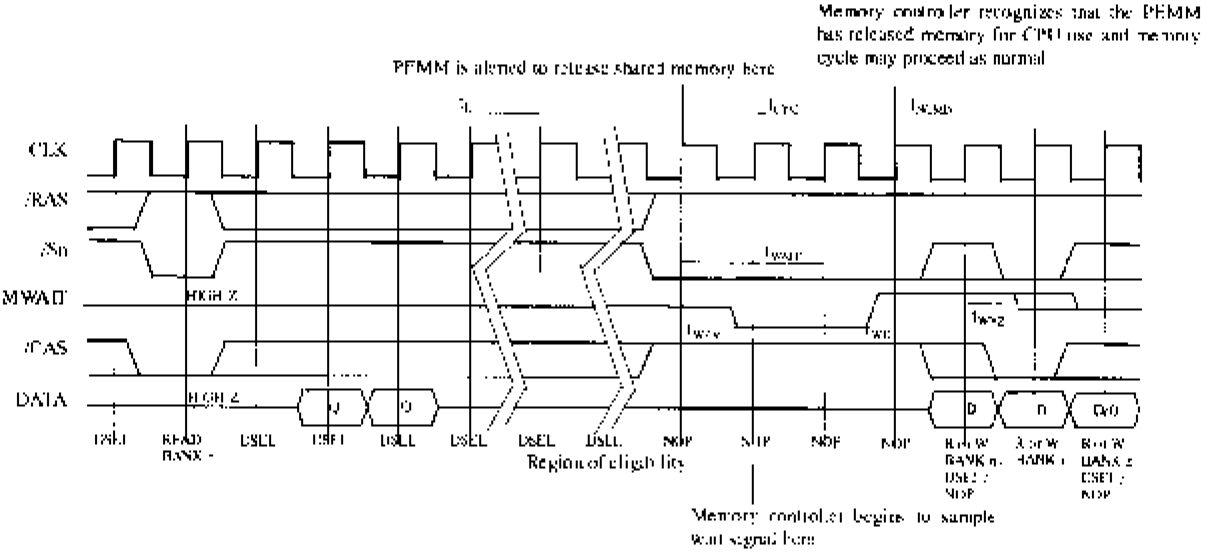
Since eligibility can not begin until after all bursts are complete, the PEMM Controller must be aware of the programmed SDRAM burst length value. The PEMM Controller shall "snoop" the memory bus during an SDRAM Mode Register Set (MRS) command to determine the value of the SDRAM setup register.

The MMPU, after gaining access to the memory shall be responsible for issuing a precharge for all banks that it wishes to access via a PALL or one or more PRE command(s). After precharging is complete, the MMPU may issue an ACTV command for its desired row. The MMPU may sustain uninterrupted access to the memory until the memory controller issues a NOP command, indicating that the main CPU wishes to access the shared memory. When the MMPU is finished accessing memory, or if the main CPU requests access, the MMPU will be responsible for closing all of its open pages, and re-opening all broken CPU pages. This method of operation takes the burden off of the memory controller, allowing memory cycles to continue as normal without having to re-open broken pages. The PEMM Controller on the PEMM must "snoop" the memory bus at all times, however, to keep track of which CPU pages are open.

After the point of memory eligibility has occurred, the memory controller must always issue a NOP command and monitor the wait signal before issuing any new commands. If /MWAIT is sampled to be low, then the controller must wait until /MWAIT is driven high to continue access. Access may continue with no further wait from this point until the conditions occur to produce the next point of memory eligibility.

The starting point of eligibility shall be programmable (see table in section 5.1.3.7) and must be agreed upon by the memory controller and the PEMM Controller.

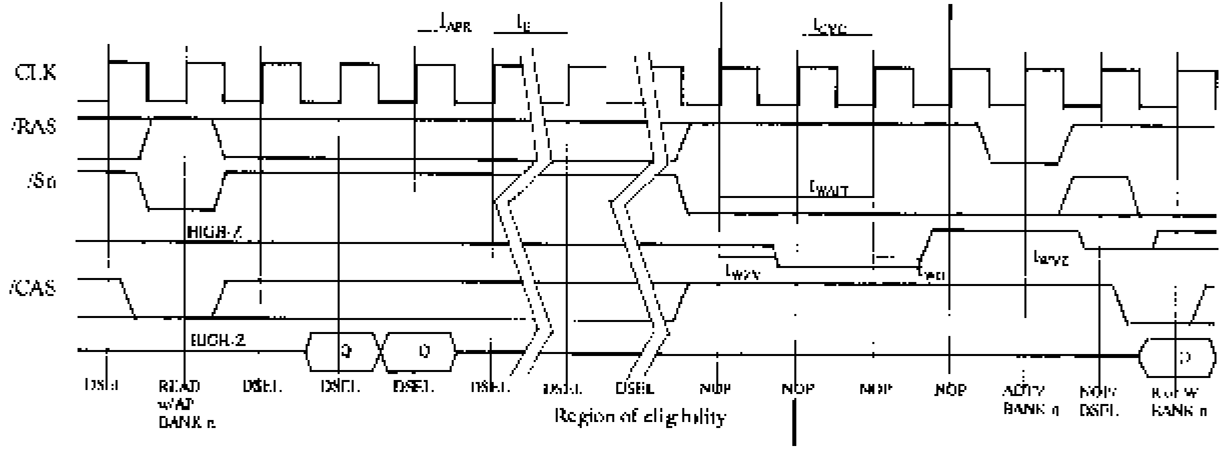
5.1.3.2Wait timing - CPU burst read followed by CPU access to same row, same bank (SDRAM BL=2, CL=2)


Memory controller recognizes that the PEMM has released memory for CPU use and memory cycle may proceed as normal
PEMM is alerted to release shared memory here
tWCE
tWSAS
CLK
/RAS
/Sn
/MWAIT
/CAS
DATA
HIGH Z
HIGH Z
tWAIT
tWZV
tWE
tWHZ
D
D
D
D
D
DSEL
READ BANK x
DSEL
DSEL
DSEL
DSEL
DSEL
DSEL
NOP
NOP
NOP
NOP
R or W BANK n, DSEL / NOP
R or W BANK x
R or W BANK z DSEL / NOP
Region of eligibility
Memory controller begins to sample wait signal here

5.1.3.3Wait timing - CPU read with auto precharge followed by CPU access to different row, same bank (SDRAM BL=2, CL=2, I_{APR}=1)

Memory controller recognizes that the PEMM has released memory for CPU use and memory cycle may proceed as normal

PEMM is alerted to release shared memory here.

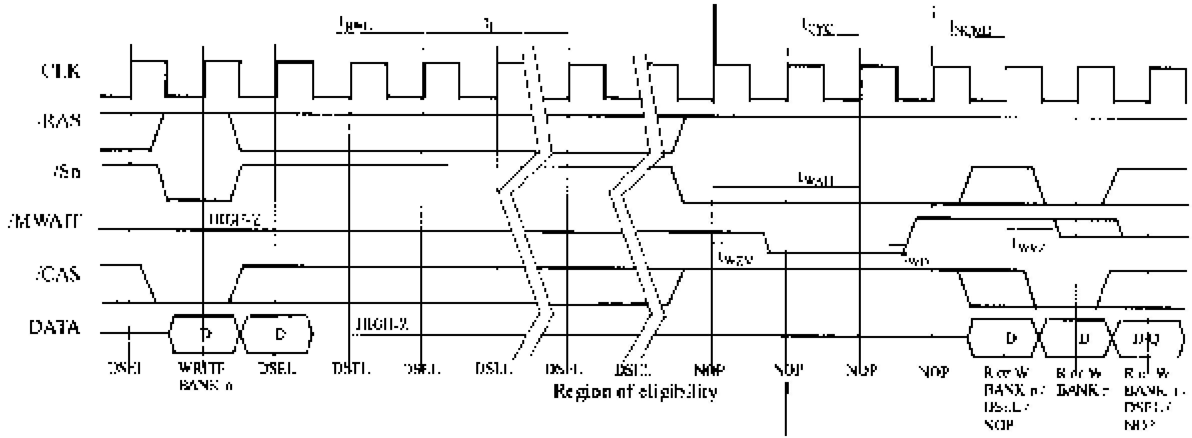


Memory controller begins to sample wait signal here

5.1.3.4Wait timing - CPU burst write followed by CPU access to same row, same bank (SDRAM BL=2, CL=2, t_{RWL}=2)

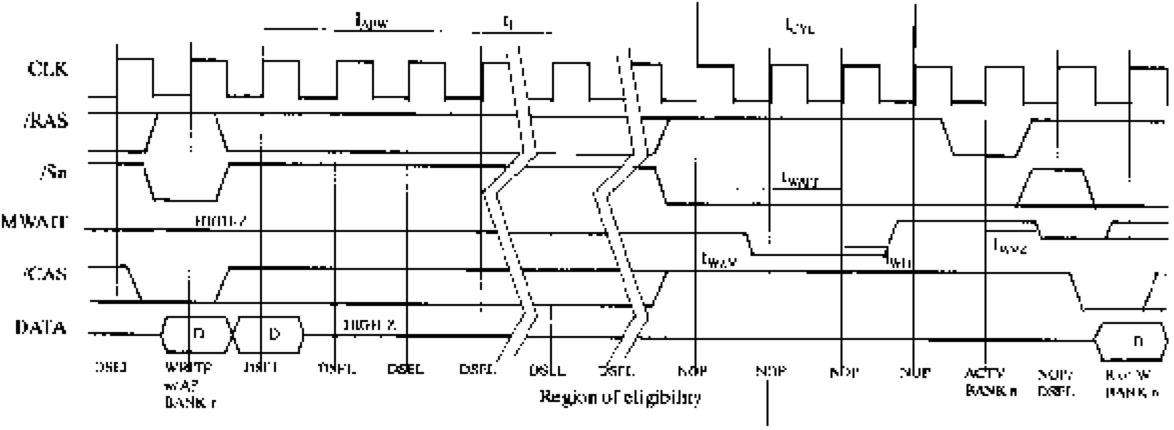
Memory controller recognizes that the PEMM has released memory for CPU use and memory cycle may proceed as normal

PEMM is alerted to release shared memory here.



Memory controller begins to sample wait signal here

5.1.3.5Wait timing – CPU write with auto precharge followed by CPU access to different row, same bank (SDRAM BL=2, CL=2, l_{APW}=3)

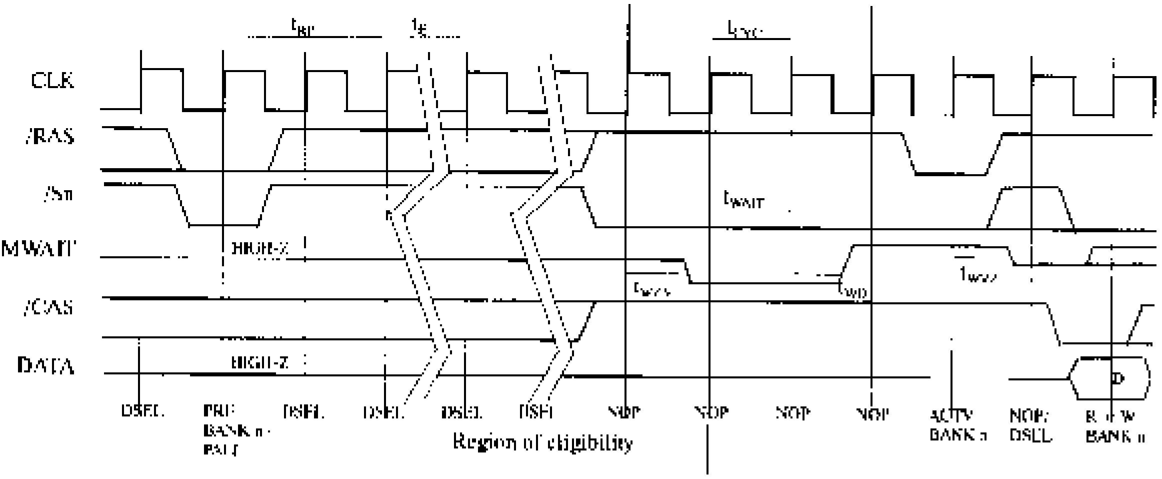


PEMM is alerted to release shared memory here.

Memory controller recognizes that the PEMM has released memory for CPU use and memory cycle may proceed as normal

Memory controller begins to sample wait signal here

5.1.3.6Wait timing – CPU precharge/precharge all followed by CPU access to different row, same bank using PALL or PRE (SDRAM t_{RP}=2)



PEMM is alerted to release shared memory here.

Memory controller recognizes that the PEMM has released memory for CPU use and memory cycle may proceed as normal

Memory controller begins to sample wait signal here

5.1.3.7Timing data for figures 5.1.3.2-5.1.3.6 (reference only)

Parameter	Description	MIN	TYP	MAX
t_{CYC}	Clock rate		-	100 MHz
t_{WAIT}[1]	/MWAIT low cycle length - MMPU accessing different row of any CPU opened bank	0 cycles	-	t_{RC} + t_{RCD} + 1 cycle
	/MWAIT low cycle length - MMPU accessing same row of any CPU opened bank	0 cycles	-	1 cycle
	/MWAIT low cycle length - MMPU accessing any closed bank	0 cycles	-	t_{RC} + 1 cycle
t_{WZV}	NOP command to /MWAIT driven	TBD[3]	TBD[3]	6 ns
t_{WD}	Delay, /MWAIT state change after CLK	2 ns	TBD[3]	6 ns
t_{WVZ}	Not NOP command to /MWAIT High-Z	2 ns	TBD[3]	TBD[3]
t_E[2]	Burst/Precharge/Refresh complete, /Sn sustained high (DSEL) to point of eligibility	5 cycles	10 cycles	15 cycles
t_{NCMD}	Required no command (DSEL or NOP) period after /MWAIT sampled as high			0 cycles

<Note>

1 This parameter is dependent upon the speed of the SDRAM in this bank. The symbol tRC is the SDRAM read or write cycle time. The symbol tRCD is the SDRAM RAS to CAS delay time. The PEMM Controller shall be programmable to control/accept a variety of memory speeds.

2 This parameter shall be programmable in the PEMM Controller.

3 This value is dependent upon the PEMM Controller. Specified MIN and MAX timing are design requirements.

5.2 Interrupt protocol

For both the EDO and SDRAM cases, the /MIRQ need not be synchronous. This output from the PEMM shall be open drain. /MIRQ shall be wire ORed on the motherboard and connected to the input of the memory controller.

If any MMPU on any module wishes to interrupt the main CPU, the corresponding PEMM Controller will drive the /MIRQ line low. The CPU, after receiving the interrupt, must then query all PEMMs in the system to determine the source of the interrupt. This shall be done by reading memory-mapped status registers in each PEMM Controller. Once the CPU acknowledges the interrupt by writing to the corresponding PEMM Controller, the /MIRQ line will be released.

If two (or more) PEMMs are requesting an interrupt at the same time, both PEMMs will be driving /MIRQ low. The CPU must acknowledge all PEMM generated interrupts before /MIRQ will be released.

5.3 Refresh handling

In order to avoid duplication of hardware, the CPU shall always be in charge of refresh timing for the shared memory. CBR or /RAS only refresh shall be accepted by the PEMM regardless of the current operating mode.

If the memory controller issues a refresh command when the PEMM is in the Standard Mode, the memory shall be refreshed as normal.

If the memory controller issues a refresh command when the PEMM is in the Smart Mode, the wait protocol need not be followed. Through snooping of the memory bus, the PEMM Controller shall detect a refresh command and execute it at the next possible memory idle time. If the MMPU is not currently executing a memory access when a refresh command is received, the memory shall be refreshed instantly.

5.3.1 Refresh handling - EDO DRAM case

Refresh commands from the CPU have high priority, thus if the MMPU is accessing the memory when a refresh command is received, the MMPU will be forced to immediately complete its access. After the MMPU's access is complete, and the required precharge time has expired, the memory controller will "echo" the CPU's refresh command (either /RAS only with a valid address or CBR refresh) to the memory. The first CPU access to memory (/RAS going low) after a CPU refresh command will experience a maximum t_{WAIT} time of t_{RL2RL2}.

5.3.2 Refresh handling - SDRAM case

Refresh commands (REF) from the CPU have high priority, thus, if the MMPU is accessing the memory when a refresh command is received, the period of memory eligibility will immediately end. The PEMM Controller will then precharge all banks with a PALL command and then execute the REF command.

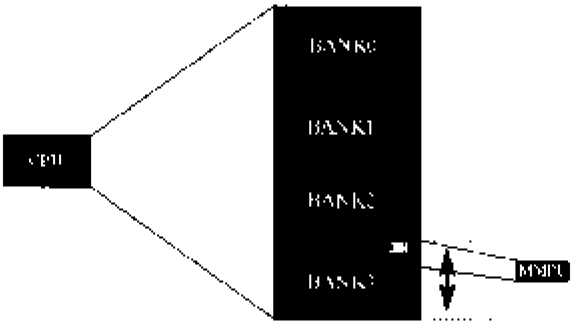
If the memory was eligible for MMPU access before the CPU REF command was issued, then the first ACTV command after the refresh command must follow the wait protocol and be preceded by a NOP command. The maximum t_{WAIT} delay experienced for this first ACTV command will be equal to t_{RC}.

5.4 Special commands

Special commands for SDRAM, such as Clock Suspend, Self Refresh (SELF), and power down shall be supported by the PEMM.

6 Architecture concept (reference only)

Basava Architecture Concept

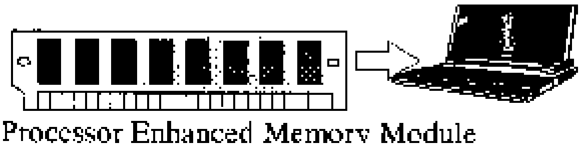


A New Computer Architecture and System Concept that:

- Enables an end user to easily enhance his system performance and add new functions
- By just plugging in a memory expansion module with one or more processors embedded in the module.
- Supporting Downloadable, Multiple Functions with Application Software Developed by Third Parties.

Benefits:

- Ease - Plug & Play MMPU
- Provides Highest Bandwidth
- Shares System Memory for Reduced Cost.
- Scaleable, Multiprocessing Solution.
- Customers can easily add value without changing platform.
- Bus Independent Solution for PCs, PDAs, Workstations, etc. Standardized interface



Processor Enhanced Memory Module

EXPLANATORY NOTES

1. Objectives of Establishment

This standard aims to define the interface and operation functional specification for DIMM based on JEDEC standard (see JESD21-C4.5.1 and 4.5.3 – 7.) that assumes that two memory banks are physically placed in 1 DIMM out of 144-pin SO-DIMM, 168-pin DIMM, etc. equipped with the EDO, SDRAM, or other formats, in order to equip processors such as microcomputer and DSP and to enhance the system function and performance.

2. Process of Discussion

In May, 1997, a company participating in the Memory Subcommitte suggested to standardize the interface and operation functional specification to equip processors such as microcomputer and DSP with DIMM such as 144-pin SO-DIMM, 168-pin DIMM, etc. used for personal computers, and to enhance the system function and performance. Therefore, EIAJ started the discussion about this standardization. Since this processor enhanced memory module ("PEMM" hereafter) responds only to the specific demands unlike general memory modules, it was considered that the EIAJ-original standard does not influence the market as commodity products, and the discussion was proceeded. However, since the memory industry regards JEDEC JC-42 Memory Standardization Committee ("JEDEC" hereafter), the sub-organization of the Electronic Industries Association (EIA) as a standardization organization for Worldwide memory market in terms of commodity memories, it was decided to approve PEMM and standardize the overview parts of its function in JEDEC. The standard was actually proposed in September, 1997, and agreed and established in June, 1998. This standard is the operation functional specification of the PEMM standard including more details and timings.

This standard has been already used by some users, and it is estimated that more users make its full use.

The following chapters are proposed to JEDEC JC-42.5 (Memory Standardization Committee), and under discussion for the moment. Therefore, only the following chapters may become JEDEC standards.

2.5 PEMM block diagram

3 PEMM operation mode

4.1 New signal definition

4.2 New sginal description

4.3 Serial presence detect table entries

3. Members of Committee

This standard was discussed mainly by Memory on Semiconductor Standardization Committee/Integrated Circuit G (group). The members are as shown below.

<Semiconductor Standardization Committee>

Chairman	Mitsutoshi Ito	NEC Corp.

<Semiconductor Standardization Committee/Integrated Circuit G>

Chief Examiner	Motoo Nakano	Fujitsu Ltd.

<Memory Subcommittee>

Chief Examiner	Yoshiharu Nishiwaki	Oki Electric Industry Co., Ltd.
Vice-Chief Examiner	Mitsuo Higuchi	Fujitsu Ltd.
Member	Young Jun Roh	LG Japan, Inc.
	Shinya Takahashi	Oki Electric Industry Co., Ltd.
	Yeong-Il Kim	Hyundai Electronic Industry Japan, Inc.
	Kenichi Kuramochi	Sanyo Electric Co., Inc.
	Yukichi Murakami	Sharp Corp.
	Yasuhiko Takahashi	Shin Nippon Steel Co.
	Akira Uematsu	Seiko Epson Co.
	Hitoshi Taniguchi	Sony Corp.
	Toshio Kimura	Toshiba Corp.
	Seijin Kim	Samsung Japan Corp.
	Soichiro Kamei	Texas Instruments Japan Ltd.
	Masaharu Yajima	NEC Corp.
	Yasuhiro Suenaga	Nippon Motorola Ltd.
	Atsushi Hiraishi	Hitachi, Ltd.
	Masao Ikushima	Matsushita Electric Industrial Co., Ltd.
	Kazutami Arimoto	Mitsubishi Electric Corp.
	Hidenori Hayashi	Rohm Ltd.
Special Member	Mitsuo Yasuhira	Matsushita Electronics Corp.
	Miwa Monma	NEC Corp.
	Yoshitomo Asakura	NEC Corp.