Standard of Electronic Industries Association of Japan

EIAJ ED-5515

Stub Series Terminated Logic for 2.5Volts (SSTL_2) Differential Input Signal Specifications

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Stub Series Terminated Logic for 2.5 Volts (SSTL_2) Differential Input Signal Specifications

1. Scope

This standard defines the differential input signal specifications for high frequency operation of Stub Series Terminated Logic for 2.5V (SSTL_2), previously standardized as EIAJ standard (EIAJ ED-5513).

Thus, the standard conforms to SSTL_2 standard and additionally defines differential input signal specification for high frequency operation devices.

2. Standard Structure

The standard is defined in three sections;

The first section defines values of input signal parameters which is used to test differential input signal specifications. The second section defines test conditions to perform differential AC input test.

Further more, in the third section describes, as reference only information, typical example of SSTL_2 class I differential input circuit, and SSTL_2 clock input circuit using direct termination resister. Also, for the SSTL_2 clock input circuit using direct termination resister, offset voltage parameter Viso and Viso deviation parameter △Viso are mentioned as reference only parameters.

1.0 Differential input parameters

Table 1.0-a Differential input DC logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IN} (DC)	DC input signal voltage	−0.30	V_{DDQ}+0.30	V	1
V_{SWING} (DC)	DC differential input voltage	0.36	V_{DDQ}+0.60	V	2

<Notes>

1. V_{IN} (DC) specifies the allowable DC execution of each differential input.
2. V_{SWING} (DC) specifies the input differential voltage $|V_{TR}-V_{CP}|$ required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complementary" input level.

Table 1.0-b Differential input AC logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
V_{SWING} (AC)	AC differential input voltage	0.70	V_{DDQ}−0.6	V	1
V_X (AC)	AC differential cross point voltage	$0.5\times V_{DDQ}$ −200mV	$0.5\times V_{DDQ}$ +200mV	V	2

<Notes>

1. V_{SWING} (AC) specifies the input differential voltage $|V_{TR}-V_{CP}|$ required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal.
2. The typical value of V_X (AC) is expected to be about $0.5\times V_{DDQ}$ of the transmitting device and V_X (AC) is expected to track variations in V_{DDQ}. Vx (AC) indicates the voltage at which differential input signals must be crossing.

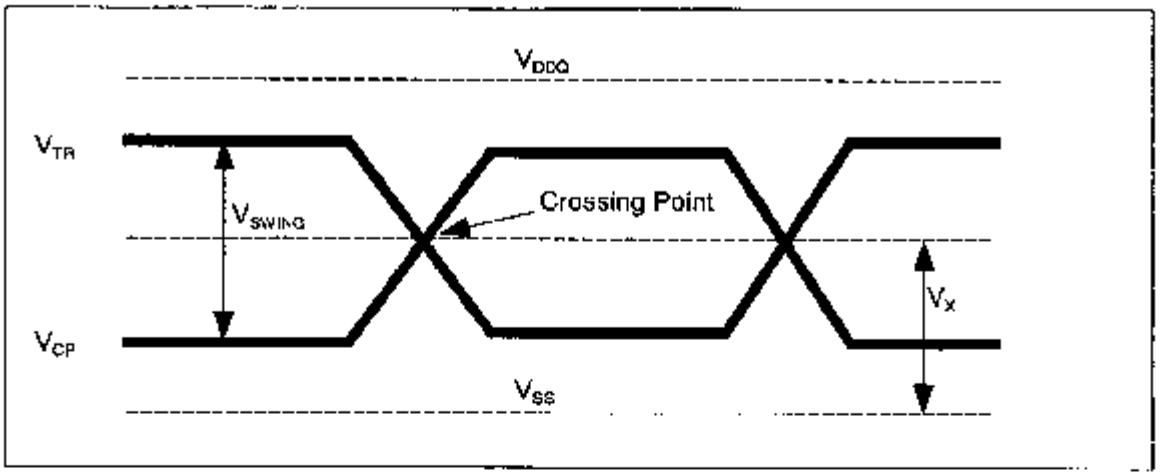

Figure 1.0 SSTL_2 differential input levels

2.0 Differential input AC test conditions

The differential AC test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.5V peak to peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the differential AC input level. This is illustrated in Figure 2.0

Table 2.0 Differential Input AC test conditions

Symbol	Parameter	Min.	Max.	Units	Notes
Vr	Input timing measurement reference level	V_X (cross point)		V	1
V_{SWING}	Input signal peak to peak swing voltage	—	1.5	V	2
SLEW	Input signal slew rate	1.0	—	V/ns	3
t_{CKD}	Clock duty cycle	45	55	%	4

<Notes>

1. In all cases, input waveform timing is referenced to two input signals (V_{TR} and V_{CP}) crossing point level (V_X) applied to the device under test, where V_{TR} is "true" input signal and V_{CP} is the "complementary" input signal. Table 1.0-b identifies the V_X (AC) range supported in SSTL_2 differential input.
2. A 1.5V input pulse level is specified to allow consistent, repeatable test results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{SWING} (AC) specification under actual use conditions. See Table 1.0-b.
3. The 1V/ns input signal minimum slew rate is to be maintained the V_{IL}max (AC) to V_{IH}min (AC) range of the input signal swing, consistent with Table 2.2-b and Figure 2.3 of SSTL_2 standard (EIAJ ED-5513).
4. For periodic clock inputs, the duty cycle (t_{CKD}) is defined to the t_{CH} (or t_{CL}) divided by t_{CK} time when "true" input signal and "complementary" input signal are crossing each other.
   See Figure 2.0-a.
   This can be expressed by equation-1 or equation-2.
   $t_{CKD}=t_{CH} / t_{CK}$ (1)
   $t_{CKD}=t_{CL} / t_{CK}$ (2)

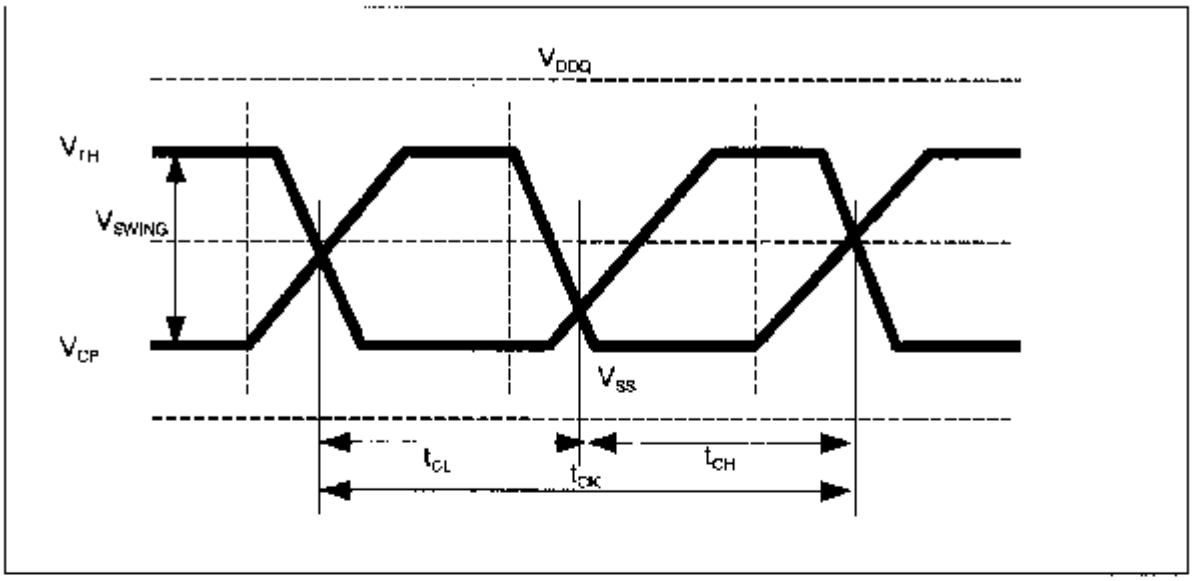

Figure 2.0 Differential AC input test signal wave form

3.0 An example of SSTL_2 Class I differential signals (Reference only)

For reference only example, Figure 3.0 show the differential clocks are independently terminated by a 50Ω resistor. The value of I_{OH} (DC) and I_{OL} (DC) has to be abide by class-I specification.

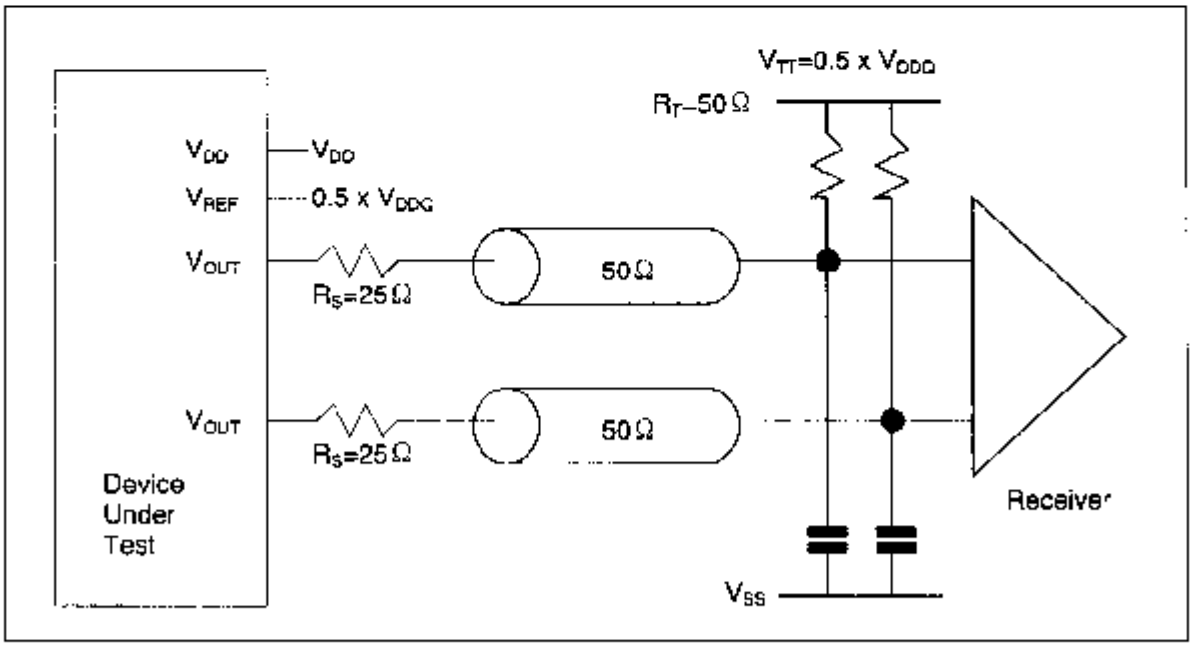

Figure 3.0 An example of SSTL_2 class I, differential signal using single load, and series resistor. (Reference only)

Table 3.0 Viso specifications (Reference only)

Symbol	Parameter	Min.	Max.	Units	Notes
Viso	Input clock signal offset voltage	$0.5\times V_{DDO}$		V	1
△Viso	Viso variation	−	+200	mV	1

<Notes>

1. For only reference, the value of Viso is expected to be $(|V_{TR}+V_{CP}|)/2$ in case of each clock directly terminated by a 100Ω resistor, where V_{TR} is the "true" input signal voltage and V_{CP} is the "complementary" input signal voltage respectively.
   See Figure 3.1-b.

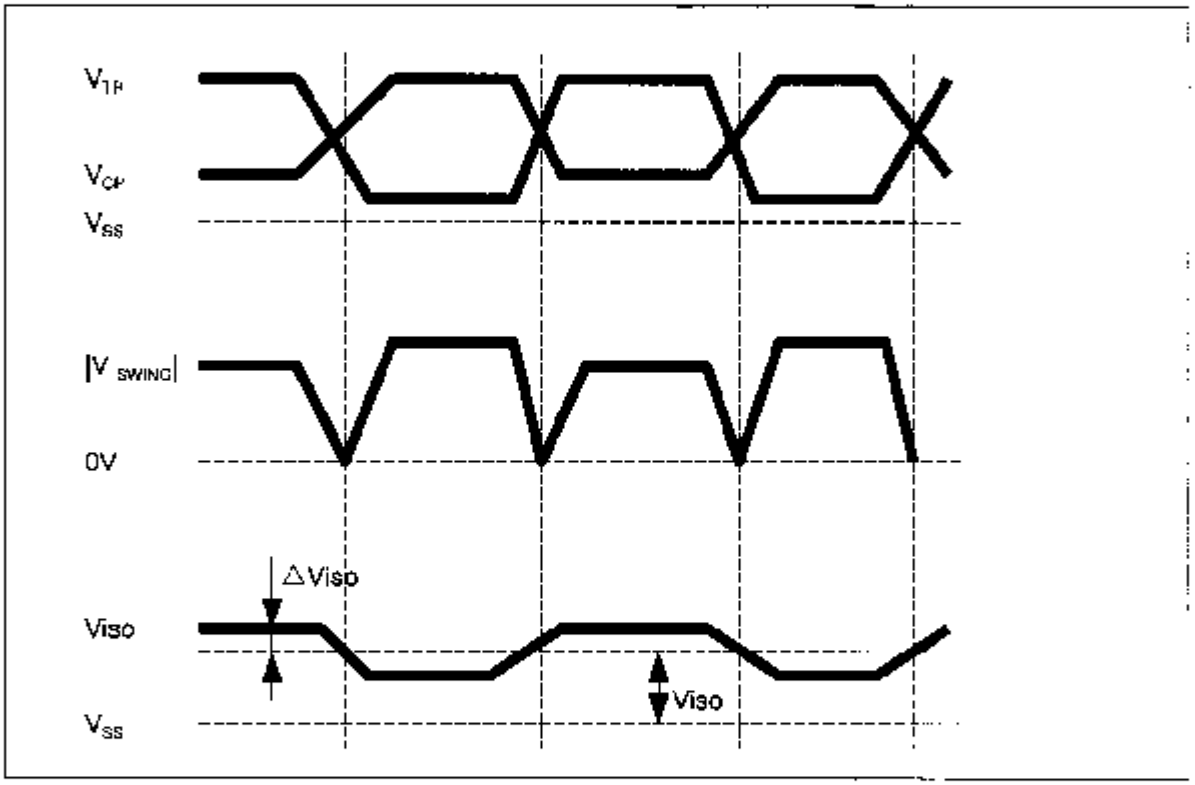

Figure 3.1-b Input clock signal offset voltage (Reference only)

3.1 For reference only example of SSTL_2 Class I differential clock signals

For reference only example, Figure 3.1-a show the differential clocks are directly terminated by a 100Ω resistor. The value of I_{OH} (DC), I_{OL} (DC) and Table-2.0 parameters have to be abide by class-I specification.

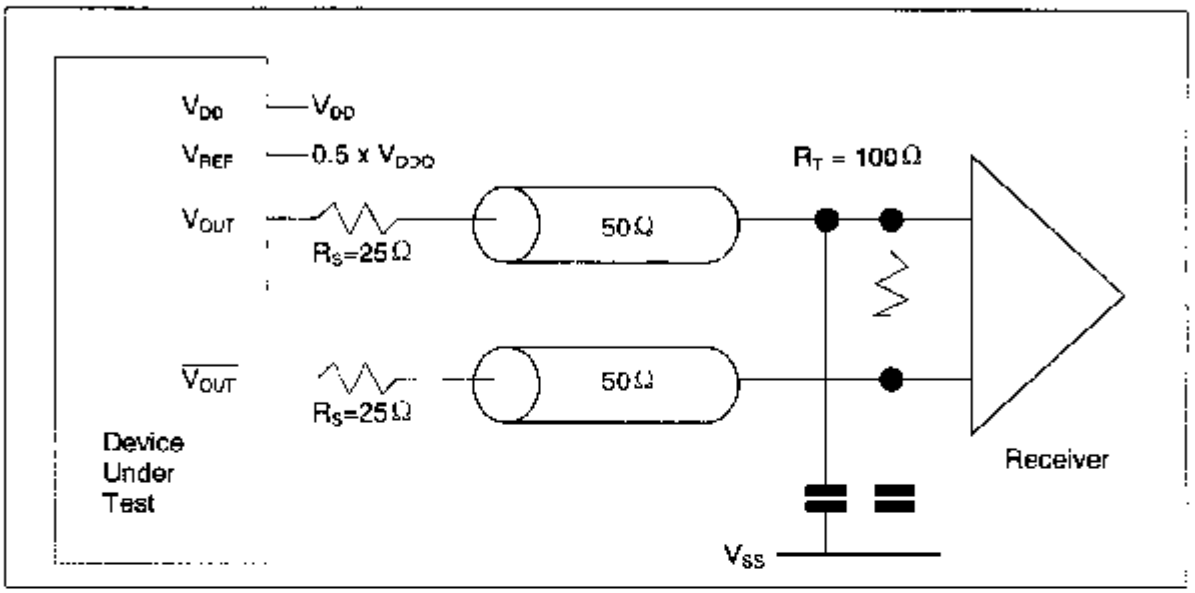

Figure 3.1-a An example of SSTL_2 class I, differential signal using direct termination resistor, and series resistor. (Reference only)

EXPLANATORY NOTES

1. Objectives of Establishment

This standard defines differential input signal specification of SSTL_2 (Stub Series Terminated Logic for 2.5V, hereafter "SSTL_2") which was previously established as EIAJ standard in August 1998. Using differential input signals, the standard aims to establish enough and superior noise margin for signal input signals to achieve devices on signal buses high frequency operation (More than 100–125MHz).

2. Process of Discussion

In Memory Subcommittee (hereafter "the subcommittee"), there is an agreement between the subcommittee and JEDEC JC-16 committee (hereafter "JEDEC") that the subcommittee submits standard proposals to JEDEC when the subcommittee wants to establish EIAJ standard which may become a worldwide common standard. And after establishing a standard in JEDEC, the subcommittee standardizes it as EIAJ-JEDEC common standard.

Based on the agreement, SSTL_2 proposal of EIAJ passed at JEDEC in December 1997. However, during more than 1 year long discussion about achieving high speed operation of devices, especially memory devices, were taken place in the industry. And, the industry considered superiority of differential input signal in discussion about interface for high frequency DRAMs such as DDR-SDRAM, SLDRAM.

To correspond to the consideration, the subcommittee started discussion about this standard in November 1997, and made first presentation at JEDEC meeting in December 1997. The proposal passed the JEDEC committee in June 1998. Then, the subcommittee made this standard as EIAJ standard.

This is an EIAJ and JEDEC joint standard.

3. Members of Committee

This standard was discussed mainly by Memory Subcommittee on Semiconductor Standardization Committee/Integrated Circuit Group. The members are as shown below.

<Semiconductor Standardization Committee>

Chairman	Mitsutoshi Ito	NEC Corp.

<Semiconductor Standardization Committee/Integrated Circuit Group>

Chief Examiner	Motoo Nakano	Fujitsu Ltd.

<Memory Subcommittee>

Chief Examiner	Yoshiharu Nishiwaki	Oki Electric Industry Co., Ltd.
Vice-Chief Examiner	Mitsuo Higuchi	Fujitsu Ltd.
Member	Young Jun Roh	LG Japan, Inc.
	Shinya Takahashi	Oki Electric Industry Co., Ltd.
	Yeong-Il Kim	Hyundai Electronic Industry Japan, Inc.
	Kenichi Kuramochi	Sanyo Electric Co., Inc.
	Yukichi Murakami	Sharp Corp.
	Yasuhiko Takahashi	Nippon-Steel Semiconductor Inc.
	Akira Uematsu	Seiko Epson Co.
	Hitoshi Taniguchi	Sony Corp.
	Toshio Kimura	Toshiba Corp.
	Seijin Kim	Samsung Japan Ltd.
	Soichiro Kamei	Texas Instruments Japan Ltd.
	Masaharu Yajima	NEC corp.
	Yasuhiro Suenaga	Nippon Motorola Ltd.
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	Kazutami Arimoto	Mitsubishi Electric Corp.
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Special Member	Mitsuo Yasuhira	Matsushita Electronics Corp.
	Miwa Monma	NEC Corp.
	Yoshitomo Asakura	NEC Corp.