Standard of Electronic Industries Association of Japan

EIAJ ED-5515

Stub Series Terminated Logic for 2.5Volts (SSTL_2)
Differential Input Signal Specifications

Established in September, 1998

Prepared by
Technical Standardization Committee on Semiconductor Devices

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Standard of Electronic Industries Association of Japan

**Stub Series Terminated Logic for 2.5 Volts (SSTL_2)**

**Differential Input Signal Specifications**

1. **Scope**

This standard defines the differential input signal specifications for high frequency operation of Stub Series Terminated Logic for 2.5V (SSTL_2), previously standardized as EIAJ standard (EIAJ ED-5513).

Thus, the standard conforms to SSTL_2 standard and additionally defines differential input signal specification for high frequency operation devices.

2. **Standard Structure**

The standard is defined in three sections:

The first section defines values of input signal parameters which is used to test differential input signal specifications. The second section defines test conditions to perform differential AC input test.

Furthermore, the third section describes, as reference only information, typical example of SSTL_2 class I differential input circuit, and SSTL_2 clock input circuit using direct termination resister. Also, for the SSTL_2 clock input circuit using direct termination resister, offset voltage parameter $V_{iso}$ and $V_{iso}$ deviation parameter $\Delta V_{iso}$ are mentioned as reference only parameters.

1.0 **Differential input parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ (DC)</td>
<td>-0.30</td>
<td>$V_{DDQ} + 0.30$</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>$V_{SWING}$ (DC)</td>
<td>0.35</td>
<td>$V_{DDQ} + 0.60$</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

**Table 1.0-a Differential Input DC logic levels**

1. $V_{IN}$ (DC) specifies the allowable DC execution of each differential input.

2. $V_{SWING}$ (DC) specifies the input differential voltage $|V_{IN} - V_{TR}|$ required for switching, where $V_{TR}$ is the "true" input level and $V_{CP}$ is the "complementary" input level.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{SWING}$ (AC)</td>
<td>-0.70</td>
<td>$V_{DDQ} + 0.6$</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>$V_{X}$ (AC)</td>
<td>$0.5 \times V_{DDQ} - 200 \text{mV}$</td>
<td>$0.5 \times V_{DDQ} + 200 \text{mV}$</td>
<td>V</td>
<td>2</td>
</tr>
</tbody>
</table>

**Table 1.0-b Differential Input AC logic levels**

1. $V_{SWING}$ (AC) specifies the input differential voltage $|V_{IN} - V_{TR}|$ required for switching, where $V_{TR}$ is the "true" input signal and $V_{CP}$ is the "complementary" input signal.

2. The typical value of $V_{X}$ (AC) is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and $V_{X}$ (AC) is expected to track variations in $V_{DDQ}$. $V_{X}$ (AC) indicates the voltage at which differential input signals must be crossing.
2.0 Differential Input AC test conditions

The differential AC test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.5V peak to peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the differential AC input level. This is illustrated in Figure 2.0.

Table 2.0 Differential Input AC test conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vr</td>
<td>Input timing measurement reference level</td>
<td>Vx</td>
<td>V</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>VsWING</td>
<td>Input signal peak to peak swing voltage</td>
<td>–</td>
<td>1.5</td>
<td>V</td>
<td>2</td>
</tr>
<tr>
<td>SLPW</td>
<td>Input signal slew rate</td>
<td>1.0</td>
<td>–</td>
<td>VPS</td>
<td>3</td>
</tr>
<tr>
<td>tCKD</td>
<td>Clock duty cycle</td>
<td>45</td>
<td>55</td>
<td>%</td>
<td>4</td>
</tr>
</tbody>
</table>

<Notes>

1. In all cases, input waveform timing is referenced to two input signals (VTR and VCP) crossing point level (Vx) applied to the device under test, where VTR is "true" input signal and VLP is the "complementary" input signal. Table 1.0-b identifies the Vx (AC) range supported in SSTL_2 differential input.

2. A 1.5V input pulse level is specified to allow consistent, repeatable test results in an automatic test equipment (ATE) environment. Compliant devices must meet the VsWING (AC) specification under actual use conditions. See Table 1.0-b.

3. The 1V/ns input signal minimum slew rate is to be maintained the VHmax (AC) to VHmin (AC) range of the input signal swing, consistent with Table 2.2-b and Figure 2.3 of SSTL_2 standard (EIAJ ED-5515).

4. For periodic clock inputs, the duty cycle (tCKD) is defined to the tCH (or tCL) divided by tCK time when "true" input signal and "complementary" input signal are crossing each other. See Figure 2.0-a.

This can be expressed by equation-1 or equation-2.

\[ t_{CKD} = t_{CH} / t_{CK} \]  \hspace{1cm} (1)  
\[ t_{CKD} = t_{CL} / t_{CK} \]  \hspace{1cm} (2)
3.0 An example of SSTL_2 Class I differential signals (Reference only)

For reference only example, Figure 3.0 show the differential clocks are independently terminated by a 50Ω resistor. The value of I_H (DC) and I_L (DC) has to be abide by class-I specification.

Figure 3.0 An example of SSTL_2 class I, differential signal using single load, and series resistor. (Reference only)
Table 3.0  Viso specifications (Reference only)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viso</td>
<td>Input clock signal offset voltage</td>
<td>$0.5 \times V_{DD}$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta V_{iso}$</td>
<td>Viso variation</td>
<td>-</td>
<td>+200 mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<Notes>

1. For only reference, the value of Viso is expected to be $(V_{TH} + V_{TP})/2$ in case of each clock directly terminated by a 100$\Omega$ resistor, where $V_{TH}$ is the “true” input signal voltage and $V_{TP}$ is the “complementary” input signal voltage respectively.

See Figure 3.1-b.

![Figure 3.1-b](image)

**Figure 3.1-b  Input clock signal offset voltage (Reference only)**
3.1 For reference only example of SSTL_2 Class I differential clock signals

For reference only example, Figure 3.1-a show the differential clocks are directly terminated by a 100Ω resistor. The value of I_{OH} (DC), I_{OL} (DC) and Table 2.0 parameters have to be abide by class-I specification.

![Diagram of SSTL_2 Class I differential clock signals]

Figure 3.1-a An example of SSTL_2 class I, differential signal using direct termination resistor, and series resistor. (Reference only)
EXPLANATORY NOTES

1. Objectives of Establishment
This standard defines differential input signal specification of SSTL_2 (Stub Series Terminated Logic for 2.5V, hereafter “SSTL_2”) which was previously established as EIAJ standard in August 1998. Using differential input signals, the standard aims to establish enough and superior noise margin for signal input signals to achieve devices on signal buses high frequency operation (More than 100~125MHz).

2. Process of Discussion
In Memory Subcommittee (hereafter “the subcommittee”), there is an agreement between the subcommittee and JEDEC JC-16 committee (hereafter “JEDEC”) that the subcommittee submits standard proposals to JEDEC when the subcommittee wants to establish EIAJ standard which may become a worldwide common standard. And after establishing a standard in JEDEC, the subcommittee standardizes it as EIAJ-JEDEC common standard.

Based on the agreement, SSTL_2 proposal of EIAJ passed at JEDEC in December 1997. However, during more than 1 year long discussion about achieving high speed operation of devices, especially memory devices, were taken place in the industry. And, the industry considered superiority of differential input signal in discussion about interface for high frequency DRAMs such as DDR-SDRAM, SLDRAM.

To correspond to the consideration, the subcommittee started discussion about this standard in November 1997, and made first presentation at JEDEC meeting in December 1997. The proposal passed the JFDEC committee in June 1998. Then, the subcommittee made this standard as EIAJ standard.

This is an EIAJ and JEDEC joint standard.
EIAJ ED-5515

3. Members of Committee

This standard was discussed mainly by Memory Subcommittee on Semiconductor Standardization Committee/Integrated Circuit Group. The members are as shown below.

{Semiconductor Standardization Committee}
Chairman Mitsutoshi Ito NEC Corp.

{Semiconductor Standardization Committee/Integrated Circuit Group}
Chief Examiner Motoo Nakano Fujitsu Ltd.

{Memory Subcommittee}
Chief Examiner Yoshinari Nishiwaki Oki Electric Industry Co., Ltd.
Vice-Chief Examiner Mitsuo Higuchi Fujitsu Ltd.
Member Young-Jun Roh LG Japan, Inc.
Shinya Takahashi Oki Electric Industry Co., Ltd.
Yeong-II Kim Hyundai Electronic Industry Japan, Inc.
Kenichi Kuramoto Sanyo Electric Co., Inc.
Yukichi Murakami Sharp Corp.
Yasuhiko Takahashi Nippon-Steel Semiconductor Inc.
Akira Uematsu Seiko Epson Co.
Hitoshi Taniguchi Sony Corp.
Toshio Kimura Toshiba Corp.
Seijin Kim Samsung Japan Ltd.
Sosuke Kamei Texas Instruments Japan Ltd.
Masaharu Yajima NEC corp.
Yasuhiko Suenaga Nippon Motorola Ltd.
Atsushi Hiraishi Hitachi Ltd.
Masao Ikushima Matsushita Electric Industrial Co., Ltd.
Kazumaru Arimoto Mitsubishi Electric Corp.
Hiidenori Hayashi Rohm Ltd.
Mitsuo Yasuhira Matsushita Electronics Corp.
Miwa Monna NEC Corp.
Yoshitomo Asakura NEC Corp.