JEITA

Standard of Japan Electronics and Information Technology Industries Association

JEITA ED－7301A

Manual for preparation of indivisual standards of integrated circuits packages

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Manual for preparation of individual standards of integrated circuits packages

Foreword

This standard was prepared by the Subcommittee on General Rules and Common, Technical Standardization Committee (TSC) on Semiconductor Device Packages, Japan Electronics and Information Technology Industries Association (**JEITA**).

This standard was prepared in compliance with the "Rules for the drafting and presentation of **JEITA** Standards", **TSC-16**, based on the normative references that were established with the intention of harmonizing with international standards.

This standard, the revision of the **EIAJ** specification **ED-7301** published on Dec. 1996, was approved on Mar. 2007 by the TSC on Semiconductor Device Packages.

1. Scope

This standard stipulates the requirements for drafting individual standards of integrated circuit packages (hereafter referred to as individual standard).

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document applies.

a) **JEITA TSC-16**, Rules for the drafting and presentation of **JEITA** Standards

b) **JEITA ED-7300A**, General rules for preparation of standards of integrated circuit packages

c) **JEITA ED-7302A**, Manual for preparation of design guides of integrated circuit packages

d) **JEITA ED-7303C**, Name and code for integrated circuit packages

3. Terms and definitions

Definitions of the terms used in this standard follow **JEITA TSC-16**, **JEITA ED-7300A**, **JEITA ED-7302A** and **JEITA ED-7303C**, other than defined below.

3.1 Individual standard

Document specifying dimensions of a particular package or a small group of packages with the aim of providing users compatibility of the package outlines.

3.2 Terms

Definitions of the terms used in this standard follow **JEITA TSC-16**, **JEITA ED-7300A**, **JEITA ED-7302A**, and **JEITA ED-7303C**.

4. Structure

The Individual standard is composed of the following components in addition to the elements specified in Clause **5.**, "Structure of the specification", in **JEITA TSC-16**.

a) Drawing

1) Package drawing (See **Figure 2**)

2) Pattern of terminal position areas (See **Figure 3**)

b) Dimension table

1) Group 1 and Group 2 (See **Table 4**)

Note: The "Group" is defined in **JEITA ED-7300A**.

5. Details of the individual standard

5.1 Master form

Master form of the individual standard is shown in **Figure 1**.

5.1.1 Structure of the master form

The master form of the individual standard consists of:

a) Third-angle projection symbols

b) Title of the **JEITA** standard (JEITA STANDARD PACKAGE OUTLINE DRAWING)

c) Registration date (DATE)

d) Sheet number (SHEET)

e) Package name (PACKAGE NAME); derivative package name specified in **JEITA ED-7303C**

f) Resistration number (JEITA REGISTRATION NO.)

5.2 Drawing

5.2.1 Components of Drawing

The package drawing and the pattern of terminal position areas are the drawings of the individual standard.

5.2.2 Outline drawing and symbols

The outline drawing and symbols are pursuant to **JEITA ED-7302A** and **JEITA ED-7300A**.

An example of the package drawing is shown in **Figure 2**, and an example of the pattern of terminal position areas is shown in **Figure 3**.

5.3 Dimension table of the individual standard

5.3.1 Group

All dimensions in the drawings are classified into Group 1 or Group 2 for tabulation.

5.3.2 Group classification

The definition of the group classification complies with **JEITA ED-7300A**.

5.3.3 Indispensable dimensions

The indispensable dimensions for the dimension table are specified by the corresponding design guide of the integrated circuit package. In case the corresponding design guide does not exist, the indispensable dimensions will be specified independently.

5.3.4 Example

An example of the dimension table is shown in **Table 4**.

6. Registration and establishment

The registration number is given to the draft of the individual standard as specified in **6.1**, and it is published as the individual standard of the integrated circuit package (**JEITA ED-7311 series**) as needed.

6.1 Designation system of the registration number (JEITA REGISTRATION NO.)

The registration number, categorized by package type, is composed of the following **a)**, **b)**, and **c)**.

The right lower column of the drawing, entitled "JEITA REGISTRATION NO", is the place wherer the number is shown.

a) "IC" denoting integrated circuits

b) Package type code

c) Serial number

1) "IC" denoting integrated circuits

Two capital letters "IC" that indicate the individual standard of integrated circuits are prefixed to the registration number.

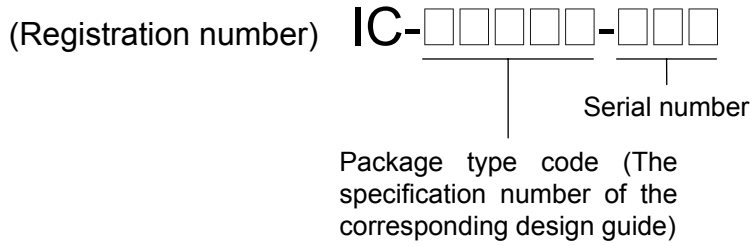
2) Package type code

The package type code shall include the specification number of the corresponding design guide, such as "*****" of **JEITA EDR-***** in four or five digits.

If the corresponding design guide to the individual standard is nowhere to be found, the design guide number of the similar package may substitute for it, only in case in which TSC on Semiconductor Device Packages approves it. If there is no such design guide, the code of "0000" is given to the individual standard.

3) Serial number

Serial number indicates the order of the registration in each package type code, starting from "001".



6.2 Reference letters (REFERENCE LETTERS)

When plural of packages with the same package name are registered simultaneously, these packages are distinguished by reference letters which are composed of two or three capital letters. The reference letters are shown in the top row of the dimension table. (See **Table 2**, **3**, and **4**)

The letters I, O, and Q shall not be used.

7. Package type

Package types are categorized pursuant to **JEITA ED-7303C**.

8. Tabulating plural of package variations

Individual standard is composed of the elements listed in Clause **4.**, and each variation is described basically in a separate sheet. But one sheet may contain up to two variations in the case of **a)**, **b)**, or **c)**.

- **a)** Package variations have the same derivative package name that is specified in **JEITA ED-7303C**.
- **b)** TSC on semiconductor device package has approved the case.
- **c)** Package variations belong to the same design guide.

9. Preparation of the registration table

The individual standard is categorized by package type or small package group and created in the order of registration number. The registration table is also prepared for each package type or each package group for the convenience of searching. (See **Table 1**, **2**, and **3**)

10. Others

Refer to **JEITA ED-7300A**, **JEITA ED-7302A**, and **JEITA TSC-16** for some other issues.

Explanation

This part of the document is not a specification but the explanation of the normative elements, appendix, informative description, and related issues.

1. Purpose of establishment

This manual, established as the guidelines for drafting the individual standard of the integrated circuit packages, specifies the indispensable items and contents for the standard.

2. History of deliberation

After the establishment of the “Administrative Rules of the TSC on Semiconductor Device Packages” (PKG-OP-001) on Dec. 1995, the Subcommittee on General Rules and Common decided to create the manual for preparation of the individual standards of integrated circuit packages. The Administrative Rules aims at the smooth processing of the proposals to **IEC** standards in response to the diversification of the integrated circuit packages. The manual was established on Dec. 1996. After that, the contents were reviewed and revised in compliance with **JEITA TSC-16** on Mar. 2007.

3. Contents of the individual standard

3.1 Relation to other standards

The layout and items in the master form of the individual standard were determined with reference to **IEC** standard and **JEDEC** standard. Figures and tables follow **JEITA ED-7302A**.

3.2 Categorization and registration number

For the registration of the package, its outline category complies with the corresponding design guide of the integrated circuit package. The Subcommittee reviewed the categorization by derivative package names specified in **JEITA ED-7303C**, but concluded not to do that but chose the categorization of the design guide. The correspondence of the individual specification to the design guide must be emphasized, because the design guide is becoming more popular.

It was agreed that the packages that belong to the same package type are classified by package-dependent particular feature, such as package nominal dimension or lead pitch. In the early stage of the discussion, there was an opinion that the classification should follow the package nominal dimensions. But, for example, it is more practical to categorize QFPs by lead pitch, which facilitates the quotation of the specifications.

4. Deliberative Members

This standard was deliberated mainly by the Subcommittee on General Rules and Common, Technical Standardization Committee on Semiconductor Device Package.

The participated members are:

<Technical Standardization Committee on Semiconductor Device Packages>

TSC Chair	Chiaki Takubo	Toshiba Corp.
TSC assistant chair	Hirofumi Nakajima	NEC Electronics Corp.

<Subcommittee on General Rules and Common>

SC chair	Katsuro Hiraiwa	Fujitsu Ltd.
SC assistant chair	Masashi Otsuka	Toshiba Corp.
	Munehiro Yamada	Renesas Technology Corp.
Members	Shuichi Matsuda	NEC Electronics Corp.
	Teruto Yamauchi	Sony Corp.
	Jun-ichi Ohno	Toshiba Corp.
	Hiroyoshi Yoshida	Matsushita Electric Industrial Co., Ltd.
	Shinichi Nakamura	Unitechno Inc.
(SC on semiconductor socket)		
	Yoshihiro Ohashi	Enplas Corp.
(SC on Integrated Circuit Packages)		
	Kazunari Kosakai	Fujitsu Ltd.
(SC on Discrete Semiconductor Device Package)		
	Akio Mikami	Renesas Technology Corp.
Observer	Hirofumi Nakajima	NEC Electronics Corp.