JEITA

Standard of Japan Electronics and Information Technology Industries Association

JEITA ED－7302A

Manual for preparation of design guides of integrated circuits packages

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Foreword

This standard was prepared by the Subcommittee on General Rules and Common, Technical Standardization Committee (TSC) on Semiconductor Device Packages, Japan Electronics and Information Technology Industries Association (**JEITA**).

This standard was prepared in compliance with the "Rules for the drafting and presentation of **JEITA** Standards", **TSC-16**, based on the normative references that were established with the intention of harmonizing with international standards.

1. Scope

This standard stipulates the general requirements for drafting design guides of integrated circuit packages (hereafter referred to as design guide).

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document shall be applied.

a) **JEITA TSC-16**, Rules for the drafting and presentation of **JEITA** Standards

b) **JEITA ED-7300A**, General rules for preparation of standards of integrated circuit packages

c) **JEITA ED-7301A**, Manual for preparation of individual standards of integrated circuit packages

d) **JEITA ED-7303C**, Name and code for integrated circuit packages

e) **IEC 60191-6 Second edition**, Mechanical standardization of semiconductor devices - Part 6: General rules for the preparation of outline drawings of surface mounted semiconductor device packages

f) **ISO 1101**, Technical drawings - Geometrical tolerancing - Tolerancing of form, orientation, location, and run-out - Generalities, definitions, symbols, indications on drawings

g) **ISO 5459**, Technical drawings - Geometrical tolerancing - Datums and datum-systems for geometrical tolerances

h) **ISO 10578**, Technical drawings - Tolerancing of orientation and location - Projected tolerance zone

3. Terms and definitions

3.1 design guide

document providing orientations and guides to designing package outlines for each package type with the aim of standardization.

Note: Design guide is not the specification on which semiconductor suppliers assures the dimensions to users.

4. Structure

4.1 Elements

The design guide is composed of the following elements. See Clause **5.** of **JEITA TSC-16** for the elements other than those described bellow, such as preliminary element.

- **a)** Scope
- **b)** Normative references
- **c)** Terms and definitions
- **d)** Definition of the package
- **e)** Terminal position numbering
- **f)** Package nominal dimension
- **g)** Symbols and drawings
  - **1)** Outline drawings
  - **2)** Pattern of terminal position areas
- **h)** Table of outline dimensions
- **i)** Table of standard-package variations
- **j)** Dimension table of individual standards
- **k)** Table, etc.
- **l)** Explanation

4.2 Details of the elements

4.2.1 Scope

The scope defines the objective packages and the limits of the applicability of the drafting design guide without ambiguity. The description of the objective packages shall include the package designation codes. It shall quotes **JEITA TSC-16**, **JEITA ED-7300A**, and **JEITA ED-7303C**, which define the basic rules for drafting the design guide.

4.2.2 Normative references

The normative references show a list of the indispensable reference documents based on **JEITA TSC-16**.

4.2.3 Terms and definitions

The general terms and definitions follow **JEITA ED-7300A** and **JEITA ED-7303C**, while undefined terms shall be defined in each design guide.

4.2.4 Definition of the package

The definition of the packages follows the **JEITA ED-7300A** and **JEITA ED-7303C**. Package categories (Forms), features, structure, and so forth shall be described. If necessary, mounting technologies and the designs of the printed wiring boards are described in this subclause.

4.2.5 Terminal position numbering

The terminal position numbering follows **JEITA ED-7300A**.

4.2.6 Package nominal dimension

Design guide specifies the representative dimensions of the package body as package nominal dimensions.

4.2.7 Symbols and drawings

The symbols and drawings comply with **JEITA ED-7300A**.

- Outline drawings

Examples of the package outlines are shown in **Figures 1** to **3** of the **Annex**. The outline drawing shall include the symbols and datums; if necessary, notes as well. The outline drawings of individual packages shall comply with **IEC 60191-6 Second edition**.

- Pattern of terminal position areas

An example of pattern of terminal position areas is shown in **Figure 4**, which is not the footprint but the pattern of permissible terminal-existing zones. It is prepared for the surface mount devices as a reference of footprint design. Through-hole devices may have the pattern of terminal position area if necessary. The definition of the pattern of terminal position conforms to **JEITA ED-7300A**.

4.2.8 Table of outline dimensions

The table of outline dimensions is shown in **Table 1** as an example. The preparation of this table conforms to **JEITA ED-7300A**. It includes the terms, symbols, specifications, recommended values, notes, etc.

4.2.9 Table of standard package variations

An example of the table of standard variations of the package is shown in **Table 2**. Among the combinations of dimensions and tolerances specified in **3.2.8**, the permissible combinations are listed in the table. Also, the recommended combinations of dimensions are encouraged to be listed in tables.

4.2.10 Dimension table of individual standards

The dimension table of individual standards specifies the dimensions and tolerances of the package for registration. An example is shown in **Table 3**.

The corresponding design guide specifies which dimensions to be specified in the dimension table of the individual standard by the mark “*” in **Table 3**. The dimension table of individual standard shall be prepared by package type. If all dimensions are available for the combination listed in the table of standard packages in the design guide, this combination is not necessary to be registered as a individual standard.

The details of preparation procedures and the implementation of individual standard shall conform to **JEITA ED-7301A**.

The part 6 in **IEC 60191** specifies the design guides for packages. Whenever the dimension table of the individual standard is specified in the design guide, the individual standard shall conform to it other than having any particular reason.

4.2.11 Table, etc.

The table and so forth may, if necessary, accompany the document in accordance with **JEITA TSC-16**. The explanation is provided.

4.2.12 Explanation

The explanation is provided as **JEITA TSC-16** specifies. The title “Explanation” shall be followed by the statement, “This part of the document is not a specification but the explanation of the normative elements, appendix, informative description, and related issues.”

Typical explanation items are as follows.

- **a)** Purpose of establishment or revision
- **b)** History of deliberations
- **c)** Brief contents of deliberations
- **d)** Industry property rights
- **e)** Relation to the international standard
- **f)** (Revised points)
- **g)** Deliberative members

Annex

4. Symbols and drawings

4.1 Outline drawings

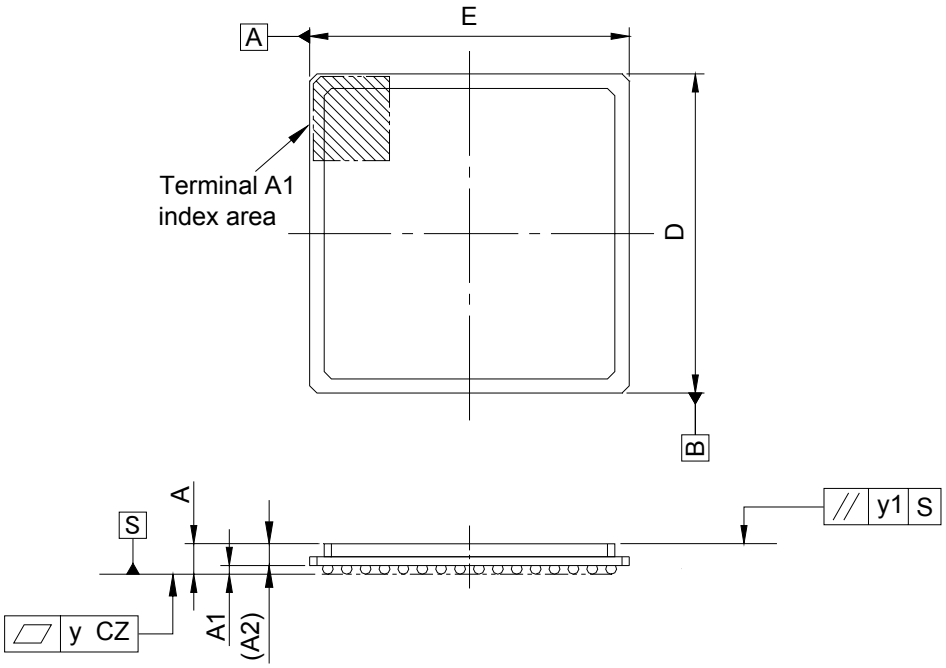


Figure 1

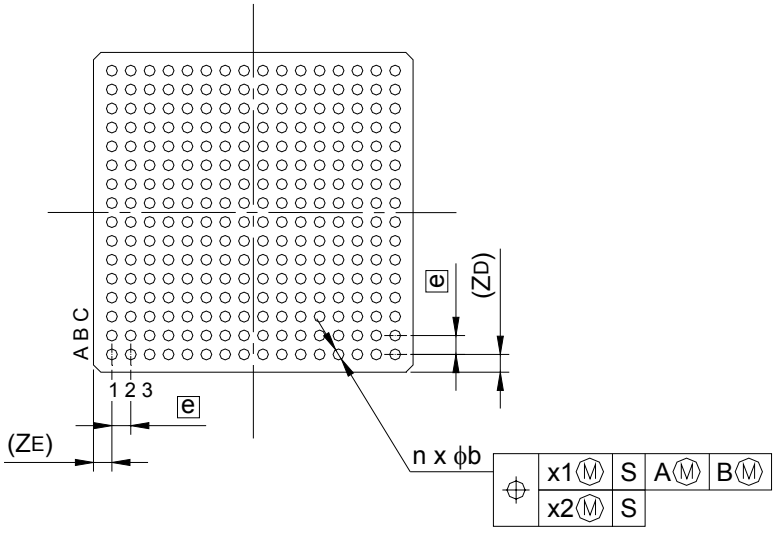


Figure 2

An example of the pattern of terminal position areas: P-BGA

The pattern of terminal position areas illustrates terminal-existing zones.

The drawing of the functional gauge shall be accompanied by the pattern of terminal position if necessary.

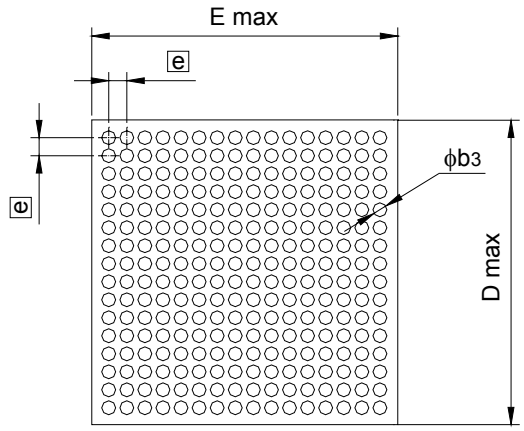


Figure 3 The drawing of the functional gauge

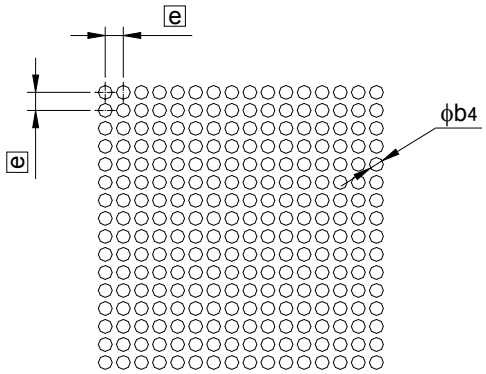


Figure 4 Pattern of terminal position areas

5. Outline dimensions

The specifications of the package dimensions are shown in **Table 1**. Since large variations of the packages are allowed by the combination of the dimensions of individual parts, new package design shall conform to the table of standard package variations in Clause **6**.

Table 1

Unit: mm

Term	Symbol	Specification	Recommended value	Notes
Nominal package dimension	E × D	**(1)** A nominal package dimension is defined as "the package width (E) × length (D)", which is expressed in the tenths place in millimeter. **(2)** Variations on nominal package dimensions are: 7.0×7.0 25.0×25.0 8.0×8.0 27.0×27.0 9.0×9.0 29.0×29.0 10.0×10.0 31.0×31.0 11.0×11.0 33.0×33.0 12.0×12.0 35.0×35.0 13.0×13.0 37.5×37.5 14.0×14.0 40.0×40.0 15.0×15.0 42.5×42.5 16.0×16.0 45.0×45.0 17.0×17.0 47.5×47.5 18.0×18.0 50.0×50.0 19.0×19.0 52.5×52.5 20.0×20.0 55.0×55.0 21.0×21.0 57.5×57.5 23.0×23.0 60.0×60.0	Refer to **Table 5** through **10**.	
Package length	D	**(1)** Package length D 7.0 25.0 8.0 27.0 9.0 29.0 10.0 31.0 11.0 33.0 12.0 35.0 13.0 37.5 14.0 40.0 15.0 42.5 16.0 45.0	Refer to **Table 5** through **10**.	

6. Table of the standard package variations

The table of the standard package variations aims at clarifying combinations of the dimensions in every part of the packages. These combinations are shown below to facilitate the designs and developments of the new packages.

Table 2 Standard package variations

Unit: mm (The tabulated number indicates pin count.)

D, E	e = 1.27				e = 1.00			
	M_{Dmax} M_{Emax}	n_{max}	M_{Dmax-1} M_{Emax-1}	n_{max}	M_{Dmax} M_{Emax}	n_{max}	M_{Dmax-1} M_{Emax-1}	n_{max}
7.0	5	25	4	16	6	36	5	25
8.0	6	36	5	25	7	49	6	36
9.0	6	36	5	25	8	64	7	49
10.0	7	49	6	36	9	81	8	64
11.0	8	64	7	49	10	100	9	81
12.0	9	81	8	64	11	121	10	100
13.0	10	100	9	81	12	144	11	121
14.0	10	100	9	81	13	169	12	144
15.0	11	121	10	100	14	196	13	169
16.0	12	144	11	121	15	225	14	196
17.0	13	169	12	144	16	256	15	225
18.0	13	169	12	144	17	289	16	256
19.0	14	196	13	169	18	324	17	289
20.0	15	225	14	196	19	361	18	324
21.0	16	256	15	225	20	400	19	361
23.0	18	324	17	289	22	484	21	441
25.0	19	361	18	324	24	576	23	529
27.0	21	441	20	400	26	676	25	625
29.0	22	484	21	441	28	784	27	729
31.0	24	576	23	529	30	900	29	841
33.0	25	625	24	576	32	1024	31	961
35.0	27	729	26	676	34	1156	33	1089
37.5	29	841	28	784	37	1369	36	1296
40.0	31	961	30	900	39	1521	38	1444
42.5	33	1089	32	1024	42	1764	41	1681
45.0	35	1225	34	1156	44	1936	43	1849
47.5	37	1369	36	1296	47	2209	46	2116
50.0	39	1521	38	1444	49	2401	48	2304
52.5	41	1681	40	1600	52	2704	51	2601
55.0	43	1849	42	1764	54	2916	53	2809
57.5	45	2025	44	1936	57	3249	56	3136
60.0	47	2209	46	2116	59	3481	58	3364

7. Table of individual standard

The committee member who wishes to propose a new outline standard will fill in the Annex Form 5 in "Administrative Rules of the TSC on Semiconductor Device Packages", and proceed to the registration procedure of the standard, following the "Manual for preparation of individual standard of integrated circuit packages". Package outline dimension table, section 2 of Form 5, shall follow the table below, appropriate dimensions shall be listed where symbol "*" are there. Package code shall be described based on the "Name and code for the integrated circuit packages", **JEITA ED-7303C**.

Table 3

Reference Number				
Package codes		□_□BGA□□□□_□□□□_□.□□		
Symbols		MIN	NOM	MAX
Group I	D	*	*	*
	E	*	*	*
	V			*
	W			*
	A	*	*	*
	A_1	*	*	*
	A_4	*		
	e		*	
	b	*	*	*
	x			*
	y			*
	y_1			*
	S_D		*	
	S_E		*	
	n		*	
	M_D		*	
	M_E		*	
	Terminal depopulation	* (**Note**)		
Group II	Z_D		*	
	Z_E		*	

Explanation

This part of the document is not a specification but the explanation of the normative elements, appendix, informative description, and related issues.

1. Purpose of establishment

This standard is established to provide the guidelines for the preparation of the design guide of the integrated circuit packages by specifying the items and contents to be described.

2. History of deliberation

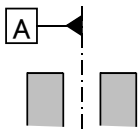
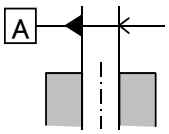
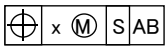
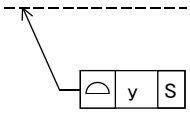
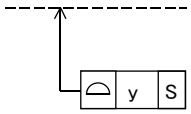
After the establishment of the “Administrative Rules of the TSC on Semiconductor Device Packages” (PKG-OP-001) on Dec. 1995, the Subcommittee on General Rules and Common decided to create the manual for preparation of design guides of integrated circuit packages. It aims at the smooth processing of the proposals to **IEC** standards in associated with the diversification of the integrated circuit packages. The outcome was published as **EIAJ ED-7302** on Apr. 1997.

In response to the establishment of **IEC 60191-6 Second edition** on Sep. 2004, the Subcommittee started reviewing and revising the contents of this document in compliance with **JEITA TSC-16**.

3. Changes in IEC 60191-6 Second edition

IEC 60191-6 Second edition was revised so that the package outline drawing would be drawn accurately in compliance with the rules of the technical drawing in **ISO**. Brief changes are described in **Explanatory table 1** for reference.

Explanatory table 1　Brief changes in IEC 60191-6 Second edition

Item	Brief changes		Reasons
	Before	After	
Datum	Datum letter and triangle is directly connected to the median plane. 	Datum letter and triangle is connected to the extension of dimension line. 	**1.** Feature outline is inevitable to specify the datum median plane. (Drawing rule: **ISO 5459**) **2.** The previous datum expression is prohibited to use. (Drawing rule: **ISO 1101**)
Lead positional tolerance			**1.** The tolerance that controls the position of the protruded feature including lead is referred to as projected tolerance zone. It is expressed by Ⓟ following the tolerance value and symbol Ⓜ in a tolerance frame. (Drawing rule: **ISO 10578**) **2.** Where the common datum is established by two features, the datum is indicated by two letters separated by a hyphen (e.g. A-B). (Drawing rule: **ISO 5459**)
Leader line to the toleranced feature	An angled leader line pointing the feature. 	A leader line pointing the object at right angle. 	The side of tolerance frame is connected to the toleranced feature by a leader line with an arrowhead perpendicular to the feature. (Drawing rule: **ISO 1101**)

As a general rule, outline drawings need to be prepared based on **IEC 60191-6 Second edition** when making design guide.

4. Deliberative members

This standard was deliberated mainly by the Subcommittee on General Rules and Common, Technical Standardization Committee on Semiconductor Device Package.

The participated members are as follows.

<Technical Standardization Committee on Semiconductor Device Packages>

TSC Chair	Chiaki Takubo	Toshiba Corp.

<Subcommittee on General Rules and Common>

SC chair	Katsuro Hiraiwa	Fujitsu Ltd.
SC assistant chair	Masashi Otsuka	Toshiba Corp.
	Munehiro Yamada	Renesas Technology Corp.
Members	Shuichi Matsuda	NEC Electronics Corp.
	Teruto Yamauchi	Sony Corp.
	Jun-ichi Ohno	Toshiba Corp.
	Hiroyoshi Yoshida	Matsushita Electric Industrial Co., Ltd.
	Shinichi Nakamura	Unitechno Inc.
(SC on semiconductor socket)		
	Yoshihiro Ohashi	Enplas Corp.
(SC on Integrated Circuit Packages)		
	Kazunari Kosakai	Fujitsu Ltd.
(SC on Discrete Semiconductor Device Package)		
	Akio Mikami	Renesas Technology Corp.