# JEITA

Standard of Japan Electronics and Information Technology Industries Association

## EIAJ ED - 7311-16A

## Standard of integrated circuits package

(C-LGA)

Established in June, 2000 Revised in November, 2003

Prepared by

Technical Standardization Committee on Semiconductor Device Package

Published by

Japan Electronics and Information Technology Industries Association

11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan Printed in Japan Translation without guarantee in the event of any doubt arising, the original standard in Japanese is to be evidence.

JEITA standards are established independently to any existing patents on the products, materials or processes they cover.

JEITA assumes absolutely no responsibility toward parties applying these standards or toward patent owners.

(C) 2003 by the Japan Electronics and Information Technology Industries Association

All rights reserved. No part of this standards may be reproduced in any form or by any means without prior permission in writing from the publisher.

Standard of Japan Electronics and Information Technology Industries Association

# Standard of integrated circuits package (C-LGA)

#### 1. Scope of Application

This standard regulated which among the packages classified as form D in the **EIAJ ED-7300** [Recommended practice on Standard for the preparation of outline drawings of semiconductor packages]. Ceramic Land Grid Array (hereinafter referred to as C-LGA) that the package carrier material is ceramic. C-LGA which terminal pitch is e = 1.00mm and Ceramic Fine pitch Land Grid Array (hereinafter referred to as C-FLGA) which terminal pitch is e = equal to or less than 0.80mm. This standard provides about those outline drawings and dimensions.

**Note:** This standard is correspond to **EIAJ EDR-7316A** (Design guideline of integrated circuits for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (FBGA/FLGA)), established in April 2002.

#### 2. Definition of the Technical Terms

The definition of the technical terms used in this standard is in conformity with **EIAJ ED-7300** and **EIAJ ED-7303B** (Name and Code for Integrated Circuits Package). And the definitions of technical terms appearing a new are given within the text of this standard.

#### 3. Background

In recent years, it corresponds to the multifunction of the electronic equipment, and the demand to the numerous pin package is increasing rapidly. It answers the demand, at first, Pin Grid Array (PGA) appeared and which the pin insertion type to into the printed circuit board through hole. Then, with to do mount area small being possible that Ball Grid Array (hereinafter referred to as BGA) and LGA appeared which surface mount type of the printed circuit board. This standard intended to standardize the outer dimensions of C-LGA and C-FLGA ensure compatibility between products as far as possible for standardization.

#### 4. Definition of LGA, FLGA

At the "Outline classification of shapes of semiconductor package" in **EIAJ ED-7300**, It is package "LGA" which is classified into form D. "LGA" define that package with metal Lands or metal bumps which terminal height is less than or equal to 0.10mm, and positioned in an array on base plane of the package as the external terminals. This packages structure makes it possible to surface mount the packages to the printed circuit board. ("BGA" define that package with metal Balls or metal bumps which terminal height exceeds 0.10mm.)

#### (1) Notation in terminal pitch ( e)

It defines Notation in terminal pitch ( e) as follows.

In case of terminal pitch e = less than or equal to 1.00mm, "LGA" (Land Grid Array)

In case of terminal pitch e = less than or equal to 0.80mm, "FLGA" (Fine-pitch Land Grid Array)

#### (2) Definition of material notation

It defines a material notation in the package name and the code as follows.

Ceramic type (C-), It is classified to packages which consist of ceramic substrate as interposer material.

#### (3) Notation in terminal array

It defines notation in terminal array as follows.

"ILGA" (Interstitial Land Grid Array) Terminal array are staggered.

#### 5. Numbering of Terminals

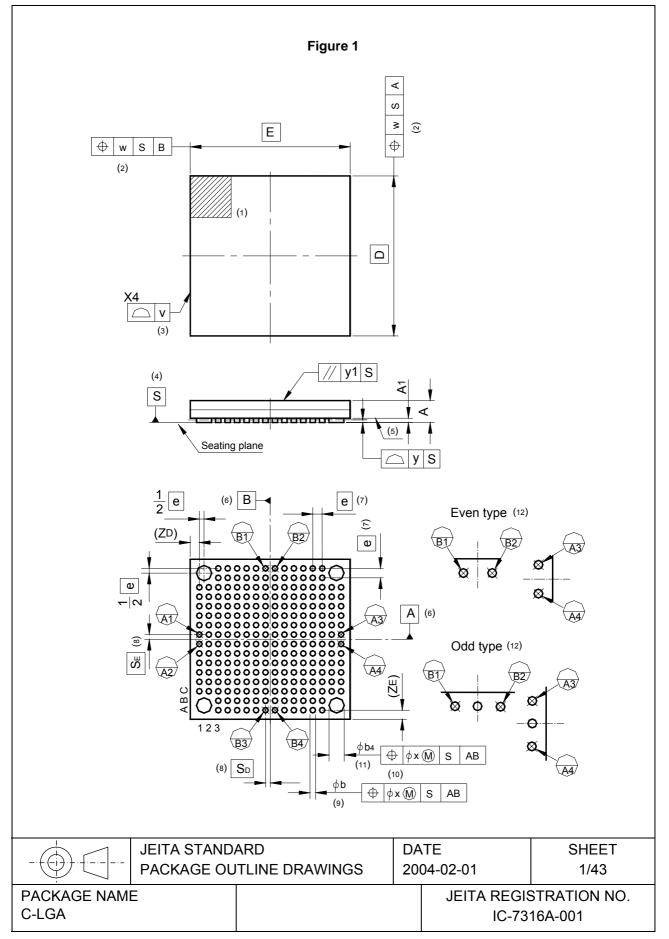
According to **EIAJ ED-7300** rules, Index is positioned at the lower left corner of the package body when it is viewed from the seating plane. A row that is the closest to the index corner is named, A, and as the row moves further away from the index the rows are named, B, C, ..... AA, AB, ..... Also, a column that is the closest to the index corner is numbered 1, and as the column moves further away to the right, they are numbered 2, 3,...... The numbering of terminals are named by these combinations A1, B1,..... In naming the rows, the letters I, O, Q, S, X, and Z should not be used.

## 6. Definition of package length (D), package width (E)

The index is positioned at the lower left corner of the package body when it is viewed from the seating plane. A vertical direction side is classified as package length ( $\square$ ) and A horizontal direction side ( $\blacksquare$ ) is package width. It doesn't define size relation between the package length and the package width.

#### 7. Nominal Dimensions

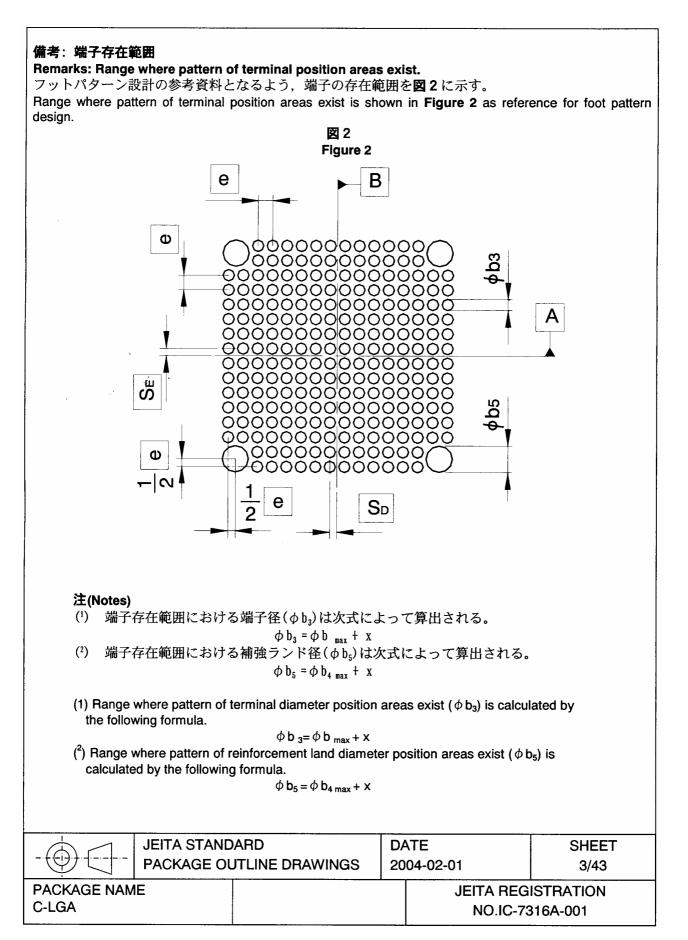
The package body size D×E (package length: D, package width: E) is regarded as Nominal dimensions.



#### Notes:

- (<sup>1</sup>) Shows the allowable position of the Index mark area, which is basically 1/16 with package body size, however in case of small package body size, it is less than 1/4 with package body size, It must be included in the shaded area entirely.
- (<sup>2</sup>) Indicates package center offset (w). Package center offset (w) prescribes each of directions package width (E) and length (D) to datum lines A, B in the package center.
- (<sup>3</sup>) Indicates tolerance of package lateral profile (v). Tolerance of package lateral profile (v) is applied to 4 sides of the package body. Meaning is tolerance zone of package outline.
- (<sup>4</sup>) Indicates seating plane (S). Seating plane is defined by the plane, which package contacts to mount surface.
- (<sup>5</sup>) Indicates base plane, which is in parallel with seating plane ( $\underline{S}$ ) and links lowest point of package body. However, it except the stand off (A<sub>1</sub>).
- (<sup>6</sup>) Datum lines of package center (A, B) are coordinates axes, which were looked for in the minimum square method for the offset of the terminal position with the geometrical true to become smallest. (Refer to **explanation 4. Definition of datum**)
- (<sup>7</sup>) Terminal pitch (e) specifies the true geometric position of the terminal axis.
- (<sup>8</sup>) Center terminal position in package direction of width and length ( $\underline{S}_{E}$ ,  $\underline{S}_{D}$ ) are stipulated the position of the closest terminal with respect to datum lines  $\underline{A}$ ,  $\underline{B}$ .
- (<sup>9</sup>) Terminal diameter (φb) provides at the maximum diameter when regarding as the projection perpendicularly from seating plane (S).
- (<sup>10</sup>) Maximum material requirements apply to the positional tolerance of the terminal center (φX), and it is applied to all terminals. (Refer to **ISO 2692/JIS B 0023**)
- $(^{11})$  Indicates reinforcement land( $\varphi b_4$ ), which are situated on the package 4 corner.
- $(^{12})$  (A1, A2), (A3, A4), (B1, B2), (B3, B4) shows the terminals which decides datum line A, B.
- (<sup>13</sup>) Position of terminal matrix and reinforcement land. It is assumed 1/2 e -->0, because it agrees for e =0.50mm.

	JEITA STAND.	ARD	DA	TE	SHEET
	PACKAGE OU	ITLINE DRAWINGS	200	04-02-01	2/43
PACKAGE NAM C-LGA	E			•=•••	STRATION NO. 16A-001



#### 8. Registration table Package name: LGA, FLGA

#### 8.1 Registration number: IC-7316A-001

It indicate registration number, [(Number of existing terminals "n")-001-(serial number, 3 cords)]

#### serial number table

Registration Numbers in the table indicate, (serial number) of 1st cord and 3rd cord.

CODE		1st		2nd		3rd
symbol	е		D		E	
	1.00	Α	3.00	Α	3.00	Α
	0.80	В	4.00	В	4.00	В
	0.65	С	5.00	С	5.00	С
	0.50	D	6.00	D	6.00	D
	0.40	E	7.00	E	7.00	E
			8.00	F	8.00	F
			9.00	G	9.00	G
			10.00	Н	10.00	Н
			11.00	J	11.00	J
			12.00	К	12.00	K
			13.00	L	13.00	L
			14.00	М	14.00	М
			15.00	N	15.00	Ν
			16.00	Р	16.00	Р
			17.00	Q	17.00	Q
			18.00	R	18.00	R
			19.00	S	19.00	S
			20.00	Т	20.00	Т
			21.00	U	21.00	U

	JEITA STAN	IDARD	DATE		SHEET
	PACKAGE OUTLINE DRAWINGS			04-02-01	4/43
PACKAGE NAME				JEITA REGIS	STRATION NO.
C-LGA				IC-73	16A-001

		-		C-LGA, C-FLGA A,C-FLGA List c	登録一覧表 of Registration ta	able			
				Terminal	Pitch	tch e			
			1.00	0.80	0.65	0.50			
		3x3							
		4x4				······			
		5x5							
		6x6							
		7x7	32-001-AEE 45-001-AEE	47-001-BEE 60-001-BEE	83-001-CEE 96-001-CEE	132-001-DEE 165-001-DEE			
		8x8	47-001-AFF 60-001-AFF	83-001-BFF 96-001-BFF	104-001-CFF 117-001-CFF	188-001-DFF 221-001-DFF			
		9x9	64-001-AGG 77-001-AGG	104-001-BGG 117-001-BGG	152-001-CGG 165-001-CGG	252-001-DGG 285-001-DGG			
		10x10	83-001-AHH 96-001-AHH	127-001-BHH 140-001-BHH	179-001-CHH 192-001-CHH	324-001-DHH 357-001-DHH			
,			104-001-AJJ	152-001-BJJ	239-001-CJJ	404-001-DJJ			
		11x11	117-001-AJJ	165-001-BJJ	252-001-CJJ	437-001-DJJ			
	ш	12x12							
		13x13	152-001-ALL 165-001-ALL	239-001-BLL 252-001-BLL	344-001-CLL 357-001-CLL	588-001-DLL 621-001-DLL			
		14x14							
		15x15	208-001-ANN 221-001-ANN	307-001-BNN 320-001-BNN	467-001-CNN 480-001-CNN	804-001-DNN 837-001-DNN			
		16x16	221-001-ANN	320-001-DININ	460-001-CININ	837-001-DINN			
			272-001-AQQ	424-001-BQQ	608-001-CQQ 621-001-CQQ	1052-001-DQQ 1085-001-DQQ			
		17x17 18x18	205-001-AQQ	437-001-DQQ	621-001-CQQ	1065-001-DQQ			
		19x19							
		20x20							
		21x21				8.2 /R 1111/1-p.			
			TANDARD		DATE		SHEET		
			GE OUTLINE [		2004-02-01		5/43		

									Unit: mm
	里番号 Number	8	32-001-AE	E	值考 Remark	4	45-001-AE	E	備考 Remark
	ジタイプ nal Type	C-LGA0	32-07.00×0	7.00-1.00		C-LGA0	45-07.00×0	7.00-1.00	
Refe	}文字 arence mbol	min	nom	max		min	nom	max	
	D	_	7.00	-		-	7.00	-	
	E	-	7.00	-		-	7.00	-	~
	v		-	0.20		-	-	0.20	
	w	-	-	0.30		-	-	0.30	
	e		1.00	-		-	1.00	-	
	A	-	-		*See below	-	-		*See below
	A <sub>1</sub>	_	-	0.10		-	-	0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	x	-	-	0.15		-	-	0.15	
	У	_	-	0.05		-	-	0.05	
	<b>y</b> 1	_	-	0.20		-	-	0.20	
	n	_	32	-	n <sub>max</sub> -16-1	-	45	-	n <sub>max</sub> -4
	Mp		7	-		-	7	-	
Ŀ	Me	-	7	-		-	7	-	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.32AEE	7	フルマトリックス Full matrix		
	So	-	0.00	_		-	0.00	_	
	St	_	0.00	-		-	0.00	-	
	Zo	_	0.50	-		-	0.50	-	
Group2	ZE	_	0.50	-		-	0.50	-	
	Φb <sub>3</sub>	_	0.60	-		-	0.60	-	
	Φb <sub>4</sub>	1.50	1.60	1.70		-	-	-	
1		_	_	1.20	TLGA		_	1.20	TLGA
		_		1.00	VLGA	-	_	1.00	VLGA
	A	_	_	0.80	WLGA	-	-	0.80	WLGA
			-	0.65	ULGA	-	_	0.65	ULGA
			-	0.50	XLGA		- 1	0.50	XLGA
							_		OUEET
			A STAN		DRAWINGS	DATE 2004-02-01			SHEET 6/43

\_\_\_\_\_

	潘号 Number	4	7-001-BE	E	備考 Remark	6	0-001-BE	E	信考 Remark
	タイプ al Type	C-FLGA0	47-07.00×0	7.00-0.80		C-FLGA	)60-07.00×0	07.00-0.80	
Refe	·文字 rence mbol	min	nom	max		min	nom	max	
	D	-	7.00			-	7.00	-	
	E	-	7.00	-		-	7.00	-	
	v	-	-	0.20		-	-	0.20	
	w	-	-	0.30		-	-	0.30	
	е	-	0.80	-		-	0.80	-	
	A	-	-		*See below	-	-		*See below
	A <sub>1</sub>	-	-	0.10		-	-	0.10	
	Φb	0.40	0.50	0.60		0.40	0.50	0.60	
Group1	x		-	0.10		-	-	0.10	
	У	_		0.05		-		0.05	
	<b>y</b> 1	-	-	0.20		-		0.20	
	n	-	47	-	n <sub>max</sub> -16-1	-	60	-	n <sub>max</sub> -4
	Mp	-	8	-		-	8	-	
	ME		8	-		-	8	-	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.47BEE	7	ルマトリック Full matrix		*See Fig.60BEE
	Sp	_	0.40	-		-	0.40	-	
	SE	_	0.40	_			0.40	-	
	Zp	_	0.70	_		-	0.70	_	
Group2	ZE	_	0.70	-		-	0.70	-	
	Φb <sub>3</sub>	_	0.50	-		-	0.50	-	
	Φb <sub>4</sub>	1.20	1.30	1.40		-	-	-	
		_	-	1.20	TFLGA	-	-	1.20	TFLGA
		_	-	1.00	VFLGA		-	1.00	VFLGA
	Α	-	-	0.80	WFLGA	-	-	0.80	WFLGA
		_	-	0.65	UFLGA	-	-	0.65	UFLGA
		-	-	0.50	XFLGA	-	-	0.50	XFLGA
			A STAN		DRAWINGS	DAT 2004	E I-02-01		SHEET 7/43

Г

	l番号 Number	ε	3-001-CE	E	備考 Remark	ę	96-001-CE	E	備考 Remark
	タイプ al Type	C-FLGA0	83-07.00×0	7.00-0.65		C-FLGA	096-07.00×0	07.00-0.65	
Refe	ì文字 rence mbol	min	nom	max		min	nom	max	
	D		7.00	-		-	7.00	-	
	E	_	7.00	-		-	7.00	-	
	v	_	-	0.20		-	-	0.20	
	w	_	-	0.30		-	-	0.30	
	e	_	0.65	_		-	0.65	-	
	A	_	-		*See below	-	-		*See below
	A <sub>1</sub>	-	-	0.10		-	-	0.10	
_	Φb	0.30	0.40	0.50		0.30	0.40	0.50	
Group1	x	-	-	0.10		-	-	0.10	
	У	_	-	0.05		-	-	0.05	
	<b>У</b> 1	-	-	0.20		-	-	0.20	
	n	-	83	-	n <sub>max</sub> -16-1	-	96	-	n <sub>max</sub> -4
	Mo	_	10	-		-	10	-	
t	Me		10	-		-	10	-	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.83CEE	7	・ ルマトリック Full matrix		*See Fig.96CEE
	Sp	_	0.325	_		-	0.325	-	
ł	S	_	0.325	_		-	0.325	-	
	ZD	_	0.575	_		-	0.575	_	
Group2	ZE	_	0.575	-		-	0.575	_	
ł	Φb <sub>3</sub>	_	0.40	-		-	0.40	_	
	Φb <sub>4</sub>	0.95	1.05	1.15		-	-	-	
. [		_	-	1.20	TFLGA	-	-	1.20	TFLGA
		_	-	1.00	VFLGA	_	-	1.00	VFLGA
	A	_	-	0.80	WFLGA	-	-	0.80	WFLGA
		_	-	0.65	UFLGA	-	-	0.65	UFLGA
l		-	-	0.50	XFLGA	_	-	0.50	XFLGA
			A STANE		RAWINGS	DAT 2004	E -02-01		SHEET 8/43

	(			=07.00X07					Unit: mm
	!番号 Number	13	32-001-DE	EE	備考 Remark	1	65-001-DI	E	備考 Remark
	タイプ al Type	C-FLGA1	32-07.00×0	)7.00-0.50		C-FLGA	165-07.00×0	07.00-0.50	
Refe	文字 rence nbol	min	nom	max	nax		nom	max	
	D	_	7.00	_			7.00		
	Ē	_	7.00	_		_	7.00	-	
	v	_		0.20		_	-	0.20	
	w	_	_	0.30			-	0.30	
	е	-	0.50			_	0.50	_	
	A				*See below	-	-		*See below
	A <sub>1</sub>	_		0.10		-	_	0.10	
	Φb	0.20	0.30	0.40		0.20	0.30	0.40	
Group1	x			0.10		_		0.10	
	у	<u> </u>	_	0.05		-	_	0.05	
	у У1		-	0.20			-	0.20	
	n		132		n <sub>max</sub> -36-1	-	165		n <sub>max</sub> -4
	M <sub>D</sub>	_	13			_	13	_	
	M <sub>E</sub>	_	13				13		
	端子配列 Terminal arry	補強ランドタイプ Reinforcement Land type			*See Fig.132DEE		ハマトリック Full matrix		*See Fig.165DE
	SD		0.00			-	0.00	-	
	S₌		0.00				0.00	-	
	<u> </u>		0.50	_			0.50	_	
Group2	ZE		0.50	_			0.50		
	Φb <sub>3</sub>	-	0.30	-		_	0.30	_	
	Φb <sub>4</sub>	0.70	0.80	0.90		_	-	_	
		T	1	T.=	r	r			· · · · · ·
				1.20	TFLGA			1.20	TFLGA
	_			1.00	VFLGA			1.00	VFLGA
	A			0.80	WFLGA		-	0.80	WFLGA
				0.65	UFLGA			0.65	UFLGA
				0.50	XFLGA		-	0.50	XFLGA
			A STAN	DARD		DAT	Ē		SHEET
					DRAWINGS		_ 4-02-01		9/43

	፤番号 Number	4	7-001-AF	F	備考 Remark		60-001 <b>-A</b> F	F	Unit: mm 備考 Remark
	タイプ al Type	C-LGA04	47-08.00×0	8.00-1.00		C-LGA	)60-08.00×0		
Refe	☆文字 rence mbol	min	nom	max		min	nom	max	:
	D	_	8.00	_		_	8.00		
	E		8.00				8.00	-	
	v	_		0.20				0.20	
	w	<del></del>	-	0.30		_		0.30	
	e		1.00			_	1.00	-	
	A		_		*See below	-	_		*See below
	A <sub>1</sub>	-	_	0.10			_	0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	x			0.15		-		0.15	
	у			0.05		_	_	0.05	
	y <sub>1</sub>	_		0.20		_		0.20	
	n	_	47		n <sub>max</sub> -16-1	_	60		n <sub>max</sub> -4
	Mp		8			_	8		
	ME		8				8		
	端子配列 Terminal arry		」 強ランドタイ cement La		*See Fig.47AFF	-	/ ハマトリック Full matrix		*See Fig.60AFF
	SD		0.50				0.50	_	
	SE		0.50			_	0.50		
	ZD		0.50			_	0.50		
Group2	ZE		0.50				0.50	<b>—</b> .	
	−⊑ Φb <sub>3</sub>		0.60				0.60		
	Φb <sub>4</sub>	1.50	1.60	1.70				_	
	71		1		L <u></u> J	L		1	L
		_	-	1.20	TLGA	_	-	1.20	TLGA
		_		1.00	VLGA	-	_	1.00	VLGA
	A			0.80	WLGA			0.80	WLGA
		-	_	0.65	ULGA	_	_	0.65	ULGA
				0.50	XLGA			0.50	XLGA
			A STANI		DRAWINGS	DAT			SHEET 10/43
ACKAG					DRAWINGS 2004-02-01 JEITA REGISTRA IC-7316A-			ATION NC	

Externa		Ċ	33-001-BF	F	備考 Remark	9	96-001-BF	F	備考 Remark
	タイプ al Type	C-FLGA0	83-08.00×0	08.00-0.80		C-FLGA	)96-08.00×(	08.00-0.80	
	文字 rence nbol	min	nom	max		min	nom	max	
	D	· —	8.00	_		_	8.00		
F	E		8.00	_		-	8.00	_	
F	v	_	-	0.20				0.20	
	w			0.30			-	0.30	
	е	_	0.80	_		-	0.80	_	
F	A	_	-		*See below	_	-		*See below
F	A <sub>1</sub>	_	_	0.10		_	-	0.10	
	Φb	0.40	0.50	0.60		0.40	0.50	0.60	
Group1	х			0.10		_	_	0.10	_
	у	_	—	0.05		_	-	0.05	
Γ	<b>y</b> 1		-	0.20			-	0.20	
ſ	n		83		n <sub>max</sub> -16-1		96		n <sub>max</sub> -4
F	M <sub>D</sub>	_	10	_		_	10	_	
F	ME		10				10		
	端子配列 Terminal arry		強ランドタ⊣ cement La		*See Fig.83BFF		ルマトリック Full matrix		*See Fig.96BFF
	SD	_	0.40	_		_	0.40	_	
_	SE		0.40				0.40	_	
F	ZD		0.40				0.40	_	
Group2	ZE	_	0.40	—			0.40		·····
	Φb <sub>3</sub>	_	0.50				0.50	_	
	Φb <sub>4</sub>	1.20	1.30	1.40			-	-	
Г	[	-		1.20	TFLGA		-	1.20	TFLGA
			-	1.00	VFLGA	-	_	1.00	VFLGA
	A	_	_	0.80	WFLGA			0.80	WFLGA
			_	0.65	UFLGA	_	—	0.65	UFLGA
				0.50	XFLGA	_	_	0.50	XFLGA
			A STANE KAGE O		DRAWINGS	DAT	E -02-01		SHEET 11/43

	番号 Number	1(	)4-001-CF	F	備考 Remark	1	17-001-CF	=F	備考 Remark
	タイプ al Type	C-FLGA1	04-08.00×0	8.00-0.65		C-FLGA	117-08.00×0	8.00-0.65	
Refe	·文字 rence nbol	min	nom	max		min	nom	max	
	D	_	8.00			-	8.00		
	E	_	8.00			_	8.00	—	
ŀ	v		_	0.20		_	-	0.20	
-	w			0.30		_	-	0.30	
	e		0.65	_			0.65	—	
	A		_		*See below				*See below
	A <sub>1</sub>		-	0.10		_	_	0.10	
	Φb	0.30	0.40	0.50		0.30	0.40	0.50	
Group1	x		_	0.10		_	—	0.10	
	у	_		0.05			—	0.05	
	y <sub>1</sub>	_		0.20		_	-	0.20	
	n		104		n <sub>max</sub> -16-1	-	117	-	n <sub>max</sub> -4
	MD	_	11			_	11	_	
F	M <sub>E</sub>		11				11	_	
	端子配列 Terminal arry		」 強ランドター cement La		*See Fig.104CFF	-	ルマトリック Full matrix		*See Fig.117CFI
	Sp		0.00	_		_	0.00	_	
	SE		0.00				0.00		
			0.75				0.75	-	
Group2	ZE		0.75				0.75	<u> </u>	
	Φb <sub>3</sub>		0.40			_	0.40	_	
	Φb <sub>4</sub>	0.95	1.05	1.15		_	_	_	
		_	_	1.20	TFLGA	_		1.20	TFLGA
			_	1.00	VFLGA		_	1.00	VFLGA
	A	-		0.80	WFLGA			0.80	WFLGA
			_	0.65	UFLGA	_	_	0.65	UFLGA
		-		0.50	XFLGA	_	-	0.50	XFLGA
			TA STAN		DRAWINGS	DA1 200	TE 4-02-01		SHEET 12/43
ACKAG				- <u></u>			EGISTR	ATION NC -001	

	里番号 Number	1	88-001-DI	=F	備考 Remark	2	21-001-D	FF	備考 Remark
	タイプ nal Type	C-FLGA1	88-08.00×0	8.00-0.50		C-FLGA	221-08.00×(	08.00-0.50	
Refe	ີ☆字 erence mbol	min	nom	max		min	nom	max	
	D		8.00	-		_	8.00	_	
	E	_	8.00	_			8.00	_	
	v		_	0.20			_	0.20	
	w	_	-	0.30		_	_	0.30	
	e	-	0.50	_		_	0.50		
	A		_		*See below		_		*See belov
	A <sub>1</sub>	_	_	0.10				0.10	
	Фb	0.20	0.30	0.40		0.20	0.30	0.40	
Group1	x	_		0.10		_		0.10	
	у			0.05				0.05	
	<b>У</b> 1			0.20		-	_	0.20	
	n		188		n <sub>max</sub> -36-1		221	_	n <sub>max</sub> -4
	M <sub>D</sub>		15	_		-	15	-	
-	M <sub>E</sub>	_	15			_	15	_	
	端子配列 Terminal arry		強ランドター cement La		*See Fig.188DFF	7	ルマトリック Full matrix		*See Fig.221DFI
	SD		0.00	_		_	0.00	_	
	SE	_	0.00				0.00		
	Ζn		0.50				0.50		
Group2	Z <sub>E</sub>		0.50	_		-	0.50		
	Φb <sub>3</sub>		0.30	_		_	0.30		·
	Φb <sub>4</sub>	0.70	0.80	0.90		_		-	
	[]		_	1.20	TFLGA	<u> </u>		1.20	TFLGA
		_		1.00	VFLGA			1.00	VFLGA
	A			0.80	WFLGA		<u> </u>	0.80	WFLGA
			_	0.65	UFLGA		_	0.65	UFLGA
		_		0.50	XFLGA	_		0.50	XFLGA
		1	A STANE		DRAWINGS	DAT 2004			SHEET 13/43
ACKAC	PACKAGE OUT CKAGE NAME GA				JRAWINGS	2004-02-01 JEITA REGISTRA IC-7316A-0			TION NO

г

	፤番号 Number	6	4-001-AG	G	備考 Remark	7	7-001 <b>-</b> AG	iG	備考 Remark
	タイプ nal Type	C-LGA0	64-09.00×0	9.00-1.00		C-LGA0	77-09.00×0	9.00-1.00	
Refe	↑文字 erence mbol	min	nom	max		min	nom	max	
	D	_	9.00				9.00	-	
	Ē	_	9.00	_		_	9.00	_	
	 V	_		0.20				0.20	
	w		_	0.30		_		0.30	
	e		1.00			_	1.00		
	A				*See below	_			*See below
	A <sub>1</sub>		_	0.10		-		0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	x			0.15		_		0.15	
	у		_	0.05		-	—	0.05	
	<b>y</b> 1	_		0.20			_	0.20	
	n	_	64		n <sub>max</sub> -16-1	-	77		n <sub>max</sub> -4
	Mp		9			_	9		
	ME		9				9		
	端子配列 Terminal arry		」 強ランドタ₁ cement La		*See Fig.64AGG		ルマトリック Full matrix		*See Fig.77AGG
	S₀		0.00	_		_	0.00	_	
	SE		0.00			_	0.00		
	Z <sub>D</sub>	_	0.50				0.50		
Group2	Z <sub>E</sub>		0.50			_	0.50		
	Φb <sub>3</sub>		0.60			_	0.60		
	Φb <sub>4</sub>	1.50	1.60	1.70		_		-	
			r · ·	F	F			1	, <u> </u>
				1.20	TLGA	-	_	1.20	TLGA
			_	1.00	VLGA		—	1.00	VLGA
	А			0.80	WLGA			0.80	WLGA
				0.65	ULGA		-	0.65	ULGA
		_		0.50	XLGA	_		0.50	XLGA
		JEIT		DARD	· · · · · · · · · · · · · · · · · · ·	DAT	E		SHEET
					DRAWINGS		-02-01		14/43
ACKAC						<b>_</b>			ATION NO

Г

外形/ Externa 照合			04-001-BC	GG	備考 Remark	1	17-001-B(	GG	備考 Remark
		C-FLGA1	04-09.00×0	9.00-0.80		C-FLGA1	17-09.00×0	09.00-0.80	
Syn	rence	min	nom	max		min	nom	max	
	D		9.00			_	9.00	-	
F	E	—	9.00			-	9.00	_	
	<u>v</u>	—		0.20		-	-	0.20	
h h	w	_	-	0.30			_	0.30	
F	e		0.80			_	0.80	_	
F	A	_	-		*See below	_	_		*See below
F	A <sub>1</sub>		_	0.10		-	_	0.10	
_	Φb	0.40	0.50	0.60		0.40	0.50	0.60	
Group1	х		_	0.10		-	_	0.10	
	у		_	0.05				0.05	
-	У1			0.20		_	-	0.20	
F	n		104	-	n <sub>max</sub> -16-1		117	_	n <sub>max</sub> -4
	M <sub>D</sub>		11	_		-	11	—	
F	M <sub>E</sub>		11	_		_	11	_	
	端子配列 Terminal arry		」 強ランドタ⊲ cement La		*See Fig.104BGG		レマトリック Full matrix		*See Fig.117BG0
	SD		0.00	_			0.00		
-	SE	_	0.00	_		_	0.00		
-	ZD	_	0.50				0.50		
Group2	ZE		0.50			_	0.50		
F	Φb <sub>3</sub>		0.50	_			0.50	_	
-	Φb <sub>4</sub>	1.20	1.30	1.40			_		
<u> </u>					J	L	1	I	
Γ		_	_	1.20	TFLGA	_	_	1.20	TFLGA
	-	_		1.00	VFLGA		·	1.00	VFLGA
	A	_		0.80	WFLGA	_	—	0.80	WFLGA
		_		0.65	UFLGA		-	0.65	UFLGA
		_		0.50	XFLGA			0.50	XFLGA
			A STANE		DRAWINGS	DATI 2004	≡ -02-01		SHEET 15/43

	【番号 Number	15	52-001-CC	GG	備考 Remark	1	65-001-C0	GG	備考 Remark	
	タイプ al Type	C-FLGA1	52-09.00×0	09.00-0.65		C-FLGA	165-09.00×0	9.00-0.65		
Refe	·文字 rence nbol	min	nom	max		min	nom	max		
	D		9.00	_		_	9.00			
	E		9.00	_			9.00			
	 V		-	0.20		-	_	0.20		
	w		_	0.30			_	0.30		
	е		0.65	_			0.65	_		
	A				*See below		_		*See below	
	A <sub>1</sub>			0.10			_	0.10		
_	Фb	0.30	0.40	0.50		0.30	0.40	0.50		
Group1	x	_		0.10			-	0.10		
	у		_	0.05		_	-	0.05		
	<b>У</b> 1			0.20			-	0.20		
	n		152		n <sub>max</sub> -16-1		165	-	n <sub>max</sub> -4	
	M <sub>D</sub>		13	_			13	_		
	M <sub>E</sub>	_	13			_	13			
	端子配列 Terminal arry		強ランドタ- cement La		*See Fig.152CGG	7	フルマトリックス Full matrix			
	S⊳		0.00				0.00	_		
	SE		0.00			_	0.00	_		
_	ZD		0.60				0.60			
Group2	ZE		0.60				0.60			
	Φb <sub>3</sub>		0.40	_		_	0.40	_		
	Φb₄	0.95	1.05	1.15		_	-	_		
ſ		_		1.20	TFLGA	[		1.20	TFLGA	
				1.20	VFLGA			1.00	VFLGA	
	А			0.80	WFLGA			0.80	WFLGA	
				0.65	UFLGA		_	0.65	UFLGA	
				0.50	XFLGA			0.50	XFLGA	
			A STAN			DAT	<b>F</b>		SHEET	
					DRAWINGS		⊏ I-02-01		16/43	

[\_\_\_\_\_

$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	備考 Remark		5-001-DGG	285	備考 Remark	iG	52-001-DG	25	∃番号 Number	整理 Serial			
Reference Symbol         min         nom         max         min         nom         max $D$ -         9.00         -         -         -         9.00         - $E$ -         9.00         -         -         9.00         -         -         9.00         - $V$ -         -         0.20         -         -         9.00         - $V$ -         -         0.20         -         -         9.00         - $W$ -         -         0.20         0.30         -         -         0.20 $A$ -         -         0.10         -         -         0.10 $\Phi$ 0.20         0.30         0.40         0.20         0.30         0.40 $Y$ -         0.10         -         -         0.10         -         -         0.10         -         -         0.20         0.30         0.40         -         -         0.20         0.30         0.40         -         -         0.20         -         0.20         -         0.20         -         0.20 <td< th=""><th></th><th>00-0.50</th><th>5-09.00×09.00</th><th>.GA28</th><th></th><th>9.00-0.50</th><th>52-09.00×0</th><th>C-FLGA2</th><th></th><th></th></td<>		00-0.50	5-09.00×09.00	.GA28		9.00-0.50	52-09.00×0	C-FLGA2					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		max	nom n	n		max	nom	min	rence	Refe			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		_	9.00				9.00	_					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		_	9.00			-	9.00	_					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		0.20	- 0			0.20	—	_					
A         -         -         *See below         -         -         -         0.10           Φb         0.20         0.30         0.40         -         -         0.10           Φb         0.20         0.30         0.40         -         -         0.10           x         -         -         0.10         -         -         0.10           y         -         -         0.05         -         -         0.05           y1         -         -         0.20         -         -         0.20           n         -         252         -         nmax-36-1         -         285         -           Mb         -         17         -         -         17         -           Mb         -         17         -         -         17         -           Mag         -         17         -         -         17         -           Mag         -         0.00         -         -         0.00         -           Group2         Sp         -         0.00         -         -         0.00         -           Zb         -         0.		0.30	- 0			0.30	_		w				
A         -         -         *See below         -         -         -         0.10           Φb         0.20         0.30         0.40         -         -         0.10           Φb         0.20         0.30         0.40         -         -         0.10           x         -         -         0.10         -         -         0.10           y         -         -         0.05         -         -         0.05           y1         -         -         0.20         -         -         0.20           n         -         252         -         nmax-36-1         -         285         -           Mb         -         17         -         -         17         -           Mb         -         17         -         -         17         -           Mag         -         17         -         -         17         -           Mag         -         0.00         -         -         0.00         -           Group2         Sp         -         0.00         -         -         0.00         -           Zb         -         0.			0.50				0.50	-	е				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	*See below				*See below		—	_					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		0.10	- 0			0.10			A <sub>1</sub>				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		0.40	0.30 0	20		0.40	0.30	0.20	Φb				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0.10	- 0			0.10		_	x	Group1			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		0.05	- 0			0.05	—	—	У				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		0.20	- 0			0.20	_		<b>y</b> 1				
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	n <sub>max</sub> -4		285		n <sub>max</sub> -36-1	_	252	-		ĺ			
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			17				17		M <sub>D</sub>				
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		_	17			—	17		ME				
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	*See Fig.285DG0								Terminal				
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		_	0.00				0.00		Sn				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		_	0.00			_	0.00						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			0.50	.		_	-	_					
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$			0.50		<u> </u>	_		_		Group2			
Φb <sub>4</sub> 0.70         0.80         0.90              μ          -         1.20         TFLGA          -         1.20           μ          -         1.00         VFLGA          -         1.00           μ          -         0.80         WFLGA          -         0.80			0.30				0.30						
-         -         1.00         VFLGA         -         -         1.00           A         -         -         0.80         WFLGA         -         -         0.80		—				0.90	0.80	0.70					
-         -         1.00         VFLGA         -         -         1.00           A         -         -         0.80         WFLGA         -         -         0.80	TFLGA	1 20		r	TELCA	1 20				ſ			
A 0.80 WFLGA 0.80	VFLGA				·╆╼╌────┥ ┝╌─								
	WFLGA				<u> </u>				Δ				
	UFLGA	0.65			UFLGA	0.65							
0.50   XFLGA   - 0.50	XFLGA				· <u>+</u>			_					
			I,							L			
JEITA STANDARD DATE PACKAGE OUTLINE DRAWINGS 2004-02-01	SHEET 17/43				DRAWINGS								

\_\_\_\_\_

	!番号 Number	8	3-001-AH	н	備考 Remark	9	6-001-AH	н	備考 Remark
	タイプ nal Type	C-LGA0	83-10.00×1	0.00-1.00		C-LGA0	96-10.00×1	0.00-1.00	
Refe	☆字 erence mbol	min	nom	max		min	nom	max	
	D		10.00	_		_	10.00	_	
	Ē	_	10.00	_			10.00		
	v	-	_	0.20		-	—	0.20	
	w	_		0.30		_	_	0.30	
	е	_	1.00				1.00		
	A	_	_		*See below		_		*See below
	A <sub>1</sub>	<u> </u>	-	0.10			_	0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	x	_	_	0.15			_	0.15	
	у		_	0.05		_		0.05	
	<b>У</b> 1			0.20		_	—	0.20	
	n	_	83	-	n <sub>max</sub> -16-1	_	96		n <sub>max</sub> -4
	M <sub>D</sub>	_	10				10	_	
	M <sub>E</sub>	_	10			-	10	_	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.83AHH		ルマトリック Full matrix		*See Fig.96AHH
	SD		0.50				0.50	_	
	SE		0.50			_	0.50		
_	Z <sub>D</sub>		0.50			_	0.50	_	
Group2	Z <sub>E</sub>		0.50			_	0.50		
	Φb <sub>3</sub>		0.60				0.60		
	Φb₄	1.50	1.60	1.70			-		
			1			L			
		_	-	1.20	TLGA	_	—	1.20	TLGA
				1.00	VLGA		_	1.00	VLGA
	A [	_	_	0.80	WLGA		-	0.80	WLGA
		_		0.65	ULGA			0.65	ULGA
Į			_	0.50	XLGA	_		0.50	XLGA
						DATI 2004			SHEET 18/43
					ODVI I AND A	2004-02-01			10/40

Γ\_

	፤番号 Number	1:	27-001-BH	IH	備考 Remark	1	40-001-BH	łH	備考 Remark
	タイプ nal Type	C-FLGA1	27-10.00×1	0.00-0.80		C-FLGA	140-10.00×1	0.00-0.80	
Refe	☆文字 erence mbol	min	nom	max		min	nom	max	
	D		10.00	_			10.00	_	
	Ē	_	10.00	_			10.00		
	v			0.20			_	0.20	
	w	_		0.30		_		0.30	
	e		0.80	-		_	0.80		
	A		-		*See below		-		*See below
	A <sub>1</sub>	—	-	0.10			-	0.10	
	Φb	0.40	0.50	0.60		0.40	0.50	0.60	
Group1	x			0.10			-	0.10	
	у		_	0.05				0.05	
	<b>y</b> 1		_	0.20			-	0.20	
	n		127		n <sub>max</sub> -16-1		140	_	n <sub>max</sub> -4
	Mp		12	_		_	12		
	M <sub>E</sub>		12	-			12		
			は 強ランドタイ cement La		*See Fig.127BHH	7	ルマトリック Full matrix		*See Fig.140BHI
	SD		0.40				0.40		
	Se		0.40	_			0.40		
			0.40				0.60	_	
Group2	Z <sub>E</sub>		0.60				0.60		
	<del>∠</del> ε Φb <sub>3</sub>		0.50				0.50		
	Φb <sub>4</sub>	1.20	1.30	1.40			-		
1		L = =	L	L	I				•
				1.20	TFLGA		_	1.20	TFLGA
				1.00	VFLGA	_	_	1.00	VFLGA
	А	—	-	0.80	WFLGA		_	0.80	WFLGA
				0.65	UFLGA		_	0.65	UFLGA
		_		0.50	XFLGA	_	_	0.50	XFLGA
		1				DAT			SHEET
			KAGE O		DRAWINGS	2004	-02-01		19/43

1	里番号	1	79-001-C	———— НН	備考	4	92-001-CI		Unit: mm 備考
Serial	Number	•			Remark		32-001-01	II I 	Remark
	タイプ nal Type	C-FLGA	179-10.00×	10.00-0.65		C-FLGA	192-10.00×1	10.00-0.65	
Refe	☆文字 erence mbol	min	nom	max		min	nom	max	
	D	_	10.00	-			10.00	_	···- ·
	E		10.00	_			10.00		
	v		_	0.20		_		0.20	
	w	_	<u> </u>	0.30			-	0.30	
	е	_	0.65	_		_	0.65		
	A	_	-		*See below				*See below
	A <sub>1</sub>		_	0.10		_		0.10	
_	Фb	0.30	0.40	0.50		0.30	0.40	0.50	
Group1	x	-	-	0.10			-	0.10	
	у		_	0.05		_	_	0.05	
	<b>y</b> 1		_	0.20		_	- 1	0.20	
	n		179	_	n <sub>max</sub> -16-1	_	192	_	n <sub>max</sub> -4
	M <sub>D</sub>		14	_		_	14	_	
	ME	_	14				14	_	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.179CHH	フルマトリックス Full matrix			*See Fig.192CHł
	SD		0.325	_			0.325	-	
	SE		0.325	_		_	0.325	-	
Group2	Z <sub>D</sub>		0.775	-		_	0.775	_	
aroupzr	ZE		0.775	—		_	0.775	-	
	Φb₃	_	0.40	_		_	0.40		·····
	Φb₄	0.95	1.05	1.15			_	—	
				1.20	TFLGA	_	_	1.20	TFLGA
		_	—	1.00	VFLGA		_	1.00	VFLGA
	A		-	0.80	WFLGA			0.80	WFLGA
			_	0.65	UFLGA			0.65	UFLGA
			—	0.50	XFLGA	0.50			XFLGA
					RAWINGS	DATE	E -02-01		SHEET 20/43

	已番号 Number	32	24-001-Dł	ΗH	備考 Remark	3	57-001-DI	ΗH	備考 Remark
	タイプ al Type	C-FLGA3	24-10.00×1	10.00-0.50		C-FLGA3	857-10.00×1	0.00-0.50	
Refe	☆字 erence mbol	min	nom	max		min	nom	max	
	D	_	10.00			_	10.00	_	
	E	_	10.00			_	10.00		
	 V	_		0.20			_	0.20	
	w		_	0.30		-	_	0.30	
	е		0.50	_		_	0.50	_	
	 	_			*See below	_			*See below
	A <sub>1</sub>	_	_	0.10		_	-	0.10	
	Φb	0.20	0.30	0.40		0.20	0.30	0.40	
Group1	х	_	-	0.10		_	-	0.10	
	у		_	0.05			—	0.05	-
	<b>y</b> 1		_	0.20		_	—	0.20	
	n		324	_	n <sub>max</sub> -36-1		357	_	n <sub>max</sub> -4
	MD		19				19	_	
	ME	_	19	_		_	19	_	
	端子配列 Terminal arry		強ランドター cement La		*See Fig.324DHH	7	ルマトリック Full matrix		*See Fig.357DH
	SD	_	0.00	_		_	0.00	_	
	SE	—	0.00			_	0.00		
0	Z <sub>D</sub>	_	0.50	_		_	0.50		
Group2	Z <sub>E</sub>		0.50				0.50		
	Фb <sub>3</sub>	—	0.30	_		-	0.30	—	
	$\Phi b_4$	0.70	0.80	0.90					
ſ			_	1.20	TFLGA	_	_	1.20	TFLGA
		_	_	1.00	VFLGA	_		1.00	VFLGA
	А		_	0.80	WFLGA			0.80	WFLGA
		_	_	0.65	UFLGA			0.65	UFLGA
		_	—	0.50	XFLGA			0.50	XFLGA
						DAT	F		SHEET
					DRAWINGS		-02-01		21/43

較田	播号				備考		47.004.4		Unit: mm 備考
	Number	1	04-001-A	IJ	Remark		17-001-A	JJ	Remark
	タイプ nal Type	C-LGA1	04-11.00×1	1.00-1.00		C-LGA1	17-11.00×1	1.00-1.00	
Refe	☆文字 erence mbol	min	nom	max		min	nom	max	
<b>,</b>	D		11.00	_			11.00	_	
	E		11.00			_	11.00	—	
	v	_	_	0.20		_		0.20	
	w	_	_	0.30			_	0.30	
	e	_	1.00				1.00	_	
	A				*See below		_		*See below
	<b>A</b> <sub>1</sub>			0.10			_	0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	x			0.15		_	-	0.15	
	у	_	_	0.05		_		0.05	
	У1		_	0.20				0.20	
	n	_	104		n <sub>max</sub> -16-1	_	117	—	n <sub>max</sub> -4
	Mp		11	_			11	—	
	M <sub>E</sub>		11			·	11	—	
	端子配列 Terminal arry		は 強ランドタイ cement La		*See Fig.104AJJ	7	ルマトリック Full matrix		*See Fig.117AJ
	SD	_	0.00	_		_	0.00		
	SE		0.00	_		_	0.00		
	7.		0.50			_	0.50		
Group2	Z <sub>E</sub>		0.50				0.50		
	Φb <sub>3</sub>	<u> </u>	0.60				0.60		
	Φb <sub>4</sub>	1.50	1.60	1.70					
	[]					[	I		
				1.20	TLGA			1.20	TLGA
			-	1.00	VLGA		-	1.00	VLGA
	A		—	0.80	WLGA			0.80	WLGA
				0.65	ULGA			0.65	ULGA
		-		0.50	XLGA			0.50	XLGA
		JEIT		DARD		DAT	E		SHEET
		1			DRAWINGS	2004	-02-01		22/43
ACKAC	GE NAM	<sup>_</sup>					JEITA R	EGISTR	ATION NC
LGA						JEITA REGISTRATIO IC-7316A-001			

	!番号 Number	1	52-001-B	IJ	備考 Remark	1	65-001-B	JJ	備考 Remark
	タイプ al <b>Type</b>	C-FLGA1	52-11.00×1	1.00-0.80		C-FLGA1	65-11.00×1	11.00-0.80	
Refe	☆文字 erence mbol	min	nom	max		min	nom	max	
	D	_	11.00				11.00		
,	E	_	11.00				11.00		
	v	_	-	0.20				0.20	
	w	_	_	0.30		_	_	0.30	
	е		0.80	-		_	0.80	_	
	A		_		*See below	_	_		*See below
	A <sub>1</sub>			0.10		_	-	0.10	
	Φb	0.40	0.50	0.60		0.40	0.50	0.60	
Group1	x	_		0.10			-	0.10	
	У	_	_	0.05			-	0.05	
	<b>У</b> 1	_	_	0.20		—	—	0.20	
	n	_	152	_	n <sub>max</sub> -16-1		165	_	n <sub>max</sub> -4
	M <sub>D</sub>		13				13	_	
	ME		13	_		_	13	_	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.152BJJ		ルマトリック Full matrix		*See Fig.165BJ
	S₀		0.00	_		_	0.00	_	
	SE		0.00	_		_	0.00		
	ZD	_	0.70	_			0.70		
Group2	Z <sub>E</sub>	_	0.70	_			0.70		
	Φb <sub>3</sub>		0.50				0.50	_	
	Φb <sub>4</sub>	1.20	1.30	1.40		_	-		
				1.20	TFLGA	_		1.20	TFLGA
		_	—	1.00	VFLGA			1.00	VFLGA
	А	_	_	0.80	WFLGA			0.80	WFLGA
			_	0.65	UFLGA		_	0.65	UFLGA
			_	0.50	XFLGA		_	0.50	XFLGA
		JEIT	A STAN	DARD		DAT	E		SHEET

					·····				Unit: mm
	፤番号 Number	2	39-001-C	JJ	備考 Remark		252-001-C	JJ	備考 Remark
	タイプ al Type	C-FLGA2	239-11.00×1	1.00-0.65		C-FLGA	252-11.00×1	1.00-0.65	
Refe	·文字 rence nbol	min	nom	max		min	nom	max	
	D		11.00	—		-	11.00	-	
	E		11.00			-	11.00	—	
	v	<u> </u>	_	0.20		_		0.20	
	w	_	_	0.30		-	_	0.30	
	e		0.65	—			0.65		
	A	_	-		*See below				*See below
	A <sub>1</sub>	_		0.10		-		0.10	
•	Φb	0.30	0.40	0.50		0.30	0.40	0.50	
Group1	х			0.10		_	-	0.10	
	у	_	—	0.05		_	—	0.05	
	<b>y</b> 1		—	0.20		_	—	0.20	
	n		239	-	n <sub>max</sub> -36-1	_	252	_	n <sub>max</sub> -4
	M <sub>D</sub>	_	16	_			16	_	
	M <sub>E</sub>	_	16	_			16		
	端子配列 Terminal arry		強ランドター cement La		*See Fig.239CJJ	-	フルマトリック Full matrix		*See Fig.252CJ
	SD	<u> </u>	0.325	_		_	0.325		
	S	_	0.325				0.325	_	
	Z <sub>D</sub>		0.625	_			0.625		
Group2	Z <sub>E</sub>		0.625				0.625		
	Φb <sub>3</sub>		0.40			_	0.40		
	Φb₄	0.95	1.05	1.15			_		
			_	1.20	TFLGA	_		1.20	TFLGA
				1.00	VFLGA	_		1.00	VFLGA
	Α			0.80	WFLGA	_		0.80	WFLGA
			_	0.65	UFLGA		_	0.65	UFLGA
		_		0.50	XFLGA	·	_	0.50	XFLGA
		JEIT		DARD		DAT	E		SHEET
					DRAWINGS		4-02-01		24/43
						JEITA REGISTRA			

番号 Number								·····
外形タイプ ternal Type C-FLGA404-11.00×			JJ	備考 Remark		437-001-D	JJ	備考 Remark
	C-FLGA4	64-11.00× <sup>-</sup>	11.00-0.50		C-FLGA	437-11.00×1	11.00-0.50	
文字 rence nbol	min	nom	max		min	nom	max	
D	_	11.00	_		_	11.00	_	
Ε	_	11.00	_		_	11.00	-	
v	_	-	0.20		_		0.20	
w	_	_	0.30		_	_	0.30	
e	-	0.50	_			0.50	-	
А		_		*See below				*See belov
A <sub>1</sub>	<u> </u>	-	0.10			-	0.10	<u> </u>
Φb	0.20	0.30	0.40		0.20	0.30	0.40	
х	_	—	0.10		_		0.10	
у	<u> </u>	-	0.05		_	_	0.05	
<b>y</b> 1	—	_	0.20		_	-	0.20	
n		404	—	n <sub>max</sub> -36-1	_	437	-	n <sub>max</sub> -4
MD	_	21	_		-	21	-	
ME	—	21	—		-	21	_	
端子配列 Terminal arry				*See Fig.404DJJ	フルマトリックス Full matrix			*See Fig.437DJ
SD	_	0.00				0.00	_	
S⊨	—	0.00				0.00	_	
ZD		0.50	_			0.50	_	
ZE	_	0.50	_		_	0.50	_	
Φb <sub>3</sub>	_	0.30	-		_	0.30	_	
$\begin{array}{ c c c c c } \Phi b_3 & - & 0.30 \\ \hline \Phi b_4 & 0.70 & 0.80 \\ \hline \end{array}$					_		-	
			1.00	TELOA	r	<u>,                                     </u>	1.00	
F								TFLGA
A					<u> </u>			VFLGA WFLGA
	_		• • • • • • • • • • • • • • • • • • •					UFLGA
F	_	_	+					XFLGA
I	l				L.,	I		
				BAWINGS				SHEET 25/43
	ence hbol 下 v w e A A A M <sub>D</sub> M <sub>D</sub> M <sub>D</sub> M <sub>D</sub> M <sub>E</sub> 電 子 配列 Ferminal arry S <sub>D</sub> Z <sub>E</sub> Ф b <sub>3</sub> Ф b <sub>4</sub>	ence     min       D     —       Image: D     —       V     —       V     —       W     —       W     —       W     —       W     —       W     —       W     —       W     —       M     —       A     —       A     —       A     —       A     —       Y     —       y     —       y     —       MD     —       ME     —       Ferminal arry     Reinford       SD     —       ZD     —       ZD     —       ZE     —       Db4     0.70	ence hbol         min         nom           D         -         11.00           E         -         11.00           V         -         -           W         -         -           W         -         -           W         -         -           W         -         -           W         -         -           W         -         -           Q         -         0.50           A         -         -           A1         -         -           P         0.20         0.30           X         -         -           Y         -         -           Y         -         -           Y1         -         -           Y1         -         -           ME         -         21           ME         -         21           ME         -         0.00           SD         -         0.00           ZE         -         0.50           Øb3         -         0.30           Øb4         0.70         0.80      <	ence bol         min         nom         max           D         -         11.00         -           E         -         11.00         -           V         -         0.20           W         -         0.30           E         -         0.50         -           A         -         -         0.10           Фb         0.20         0.30         0.40           X         -         -         0.10           Øb         0.20         0.30         0.40           X         -         -         0.10           Øb         0.20         0.30         0.40           X         -         -         0.10           Y         -         -         0.10           Y         -         -         0.20           n         -         404         -           Mb         -         21         -           ME         -         21         -           ME         -         0.00         -           Sp         -         0.00         -           Zp         -         0.50         -	ence bbol         min         nom         max	ence bbol         min         nom         max         min           D         -         11.00         -         -           E         -         11.00         -         -           V         -         -         0.20         -           w         -         -         0.30         -           M         -         -         *See below         -           A         -         -         0.10         -           Pb         0.20         0.30         0.40         0.20           x         -         -         0.10         -           y         -         0.10         -         -           y         -         0.20         -         -         -           y         -         21         -         -         -         -           Mb         -         21         -         -         -         -         -           Sp	ence bbol         min         nom         max         min         nom           D         -         11.00         -         -         11.00           E         -         11.00         -         -         11.00           V         -         -         0.20         -         -         11.00           V         -         -         0.20         -         -         -         -           W         -         -         0.30         -         -         -         -           M         -         -         0.10         -         -         -         -           A1         -         -         0.10         -         -         -         -           Mb         0.20         0.30         0.40         -	ence bbol         min         nom         max         min         nom         max           □          11.00           11.00           0.20          11.00           0.20           0.20           0.20           0.20           0.20           0.20           0.20           0.30           0.30           0.30           0.30           0.30           0.30           0.30           0.30           0.30           0.30           0.10           0.10           0.10           0.10           0.10           0.10           0.10           0.10           0.10

Г

整理番号 Serial Number		107-001-80			備考 Remark	1	165-001-ALL		
	タイプ Ial Type	C-LGA152-13.00×13.00-1.00				C-LGA1	C-LGA165-13.00×13.00-1.00		
Refe	ስ文字 erence mbol	min	nom	max		min	nom	max	
	D		13.00	—		_	13.00		
	E		13.00	_			13.00	_	
	v		—	0.20		_		0.20	
	w	-	-	0.30		-		0.30	
	e		1.00	—			1.00	_	
	A	_			*See below	_			*See below
	A <sub>1</sub>	_	-	0.10		_		0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	x		_	0.15		_		0.15	
	у		_	0.05		_		0.05	
	<u>У</u> 1		—	0.20		_	_	0.20	
	n		152	-	n <sub>max</sub> -16-1	_	165	—	n <sub>max</sub> -4
	M <sub>D</sub>		13			_	13		
	M <sub>E</sub>	-	13	_			13	_	
	 端子配列 Terminal arry		強ランドタイ cement La		*See Fig.152ALL	フルマトリックス Full matrix			*See Fig.165AL
	SD		0.00				0.00	_	
	SE	_	0.00			_	0.00		
		_	0.50				0.50		
Group2	ZE		0.50				0.50		
	Φb <sub>3</sub>		0.60				0.60	_	
	Φb <sub>4</sub>	1.50	1.60	1.70			-		
	ſ			1.00	TICA		Г <u> </u>	1.00	TICA
			—	1.20	TLGA			1.20	TLGA VLGA
	А			1.00 0.80	VLGA WLGA			1.00 0.80	WLGA
				0.80	ULGA			0.65	ULGA
			_	0.65	XLGA		_	0.85	XLGA
		.151		DARD		DAT	E		SHEET
					DRAWINGS		-02-01		26/43

整理番号 Serial Number		r 239-001-BLL			備考 Remark	2	252-001-BLL		
	タイプ nal Type	C-FLGA2	239-13.00×1	3.00-0.80		C-FLGA	252-13.00×1		
Refe	☆字 erence mbol	min	nom	max		min	nom	max	
	D		13.00	_		_	13.00	_	
	Ē	1	13.00	_		_	13.00	-	
	v		_	0.20		_	_	0.20	
	w	_	_	0.30		·		0.30	
	е	—	0.80				0.80	-	
	A		-		*See below	_			*See below
	A <sub>1</sub>		_	0.10			_	0.10	
	Φb	0.40	0.50	0.60		0.40	0.50	0.60	
Group1	x			0.10		_	-	0.10	· · · · ·
	у		—	0.05		_		0.05	
	<b>y</b> 1		-	0.20		_	—	0.20	
	n	_	239	1	n <sub>max</sub> -16-1	_	252	_	n <sub>max</sub> -4
	M <sub>D</sub>	_	16				16	_	
	M <sub>E</sub>	_	16	—		_	16	_	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.239BLL	7	フルマトリックス Full matrix		
	SD	_	0.40	-		_	0.40		
	SE		0.40				0.40		
	ZD		0.50	_		_	0.50	_	
Group2	Z <sub>E</sub>		0.50	_		_	0.50	_	
·	Φb <sub>3</sub>	-	0.50	_		_	0.50		
	Φb <sub>4</sub>	1.20	1.30	1.40		_	_		
[			_	1.20	TFLGA			1.20	TFLGA
		_	_	1.00	VFLGA	-	-	1.00	VFLGA
	A		—	0.80	WFLGA	_	_	0.80	WFLGA
			_	0.65	UFLGA	_		0.65	UFLGA
			_	0.50	XFLGA	_		0.50	XFLGA
					DRAWINGS	DAT	E I-02-01		SHEET 27/43

.....

整理番号 Serial Number		er 344-001-CLL			備考 Remark	3	357-001-CLL			
	タイプ al Type	C-FLGA344-13.00×13.00-0.65				C-FLGA	C-FLGA357-13.00×13.00-0.65			
Refe	≻文字 rence mbol	min	nom	max		min	nom	max		
	D	-	13.00	—			13.00	_		
	E		13.00	_		_	13.00	_		
	v	-	-	0.20		_		0.20		
	w		_	0.30		_	_	0.30		
	е		0.65	_		_	0.65	_		
	A		_		*See below		-		*See below	
	A <sub>1</sub>	_		0.10		_	-	0.10		
	Φb	0.30	0.40	0.50		0.30	0.40	0.50		
Group1	x	_		0.10		_	-	0.10		
	У	_	_	0.05			-	0.05		
	y <sub>1</sub>			0.20		-	_	0.20		
	n		344		n <sub>max</sub> -16-1	-	357		n <sub>max</sub> -4	
	M <sub>D</sub>		19	_		_	19			
	M <sub>E</sub>	_	19	-		_	19			
	端子配列 Terminal arry		強ランドタィ cement La		*See Fig.344CLL	7	・ ・ ・ Full matrix		*See Fig.357CL	
	S <sub>D</sub>		0.00			_	0.00	_		
	SE		0.00				0.00			
	Z <sub>D</sub>		0.65			_	0.65			
Group2	Z <sub>E</sub>		0.65	-	·····		0.65			
	Φb <sub>3</sub>		0.40			_	0.40	_		
	Φb <sub>4</sub>	0.95	1.05	1.15						
ſ				1.20	TFLGA			1.20	TFLGA	
			_	1.00	VFLGA		<u> </u>	1.00	VFLGA	
	Α			0.80	WFLGA		_	0.80	WFLGA	
		—	_	0.65	UFLGA	_		0.65	UFLGA	
			_	0.50	XFLGA		_	0.50	XFLGA	
			A STANE		DRAWINGS	DAT 2004	E 4-02-01		SHEET 28/43	

整理番号 Serial Number		200-001-001			備考 Remark	6	621-001-DLL		
	外形タイプ External Type		, C-FLGA588-13.00×13.00-0.50			C-FLGA6			
Refe	☆字字 erence mbol	min	nom	max		min	nom	max	
	D	_	13.00	—			13.00		
	E		13.00	_			13.00	—	
	v		_	0.20		-	-	0.20	
	w			0.30				0.30	
	e	—	0.50				0.50		
	A				*See below	_	_		*See belov
	A <sub>1</sub>		_	0.10		_	_	0.10	
	Φb	0.20	0.30	0.40		0.20	0.30	0.40	
Group1	x	_	_	0.10		_		0.10	
	У	_		0.05			-	0.05	
	<b>У</b> 1		—	0.20		-	—	0.20	
	n	_	588	_	n <sub>max</sub> -36-1	-	621	—	n <sub>max</sub> -4
	M <sub>D</sub>		25	_		_	25	_	
	ME	_	25			_	25	_	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.588DLL		フルマトリックス Full matrix		
	SD	_	0.00				0.00		
·	S		0.00			_	0.00		
	Z <sub>D</sub>	_	0.50	_			0.50		
Group2	ZE	_	0.50	_			0.50		
	Φb <sub>3</sub>		0.30				0.30		
	Φb <sub>4</sub>	0.70	0.80	0.90			-		
[		_		1.20	TFLGA	_	_	1.20	TFLGA
		_	-	1.00	VFLGA		-	1.00	VFLGA
	А		_	0.80	WFLGA			0.80	WFLGA
				0.65	UFLGA		<u> </u>	0.65	UFLGA
			_	0.50	XFLGA	_	_	0.50	XFLGA
			A STANE		DRAWINGS	DATI 2004	E -02-01		SHEET 29/43

整理番号 Serial Number		20	08-001-AN	IN	備考 Remark	2	221-001-ANN		
	タイプ al Type	C-LGA20	08-15.00×1	5.00-1.00		C-LGA2	C-LGA221-15.00×15.00-1.00		
Refe	·文字 rence nbol	min	nom	max		min	nom	max	
	D	_	15.00			_	15.00	_	
	Ē		15.00				15.00	_	
	v	_	_	0.20		_	-	0.20	
	w			0.30		_	-	0.30	1
	e	_	1.00			_	1.00	_	
	A	-			*See below	_	-		*See below
	A <sub>1</sub>			0.10				0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	х	_	_	0.15		-		0.15	
	у	_	_	0.05		_	-	0.05	
	<b>y</b> 1		_	0.20				0.20	
	n	_	208		n <sub>max</sub> -16-1	-	221		n <sub>max</sub> -4
	M <sub>D</sub>		15			_	15		
	M <sub>E</sub>		15	_			15	_	
-	端子配列 Terminal arry	補強ランドタイプ Reinforcement Land type			*See Fig.208ANN	7	フルマトリック Full matrix		*See Fig.221AN
	SD	_	0.00			_	0.00	_	
	SE		0.00	_		-	0.00	_	
_	ZD		0.50			-	0.50	_	
Group2	Z <sub>E</sub>		0.50			-	0.50	_	
	Φb <sub>3</sub>		0.60				0.60	_	
	Φb <sub>4</sub>	1.50	1.60	1.70		_	—		
•									
		-	_	1.20	TLGA	-	—	1.20	TLGA
			_	1.00	VLGA	_		1.00	VLGA
	Α	_	—	0.80	WLGA	_		0.80	WLGA
		_	_	0.65	ULGA			0.65	ULGA
		_	—	0.50	XLGA		<u> </u>	0.50	XLGA
					DRAWINGS	DAT	E 4-02-01		SHEET 30/43

整理番号 Serial Number					備考 Remark	3:	320-001-BNN			
	タイプ al <b>Type</b>	C-FLGA3	807-15.00×1	5.00-0.80		C-FLGA3	20-15.00×1	5.00-0.80	5.00-0.80	
Refe	`文字 rence mbol	min	nom	max		min	nom	max		
	D	_	15.00			_	15.00	_		
	E		15.00				15.00	_		
	v			0.20		_	_	0.20		
	w	_		0.30				0.30		
	е	_	0.80	—		_	0.80	_		
	A		_		*See below		-		*See belov	
	A <sub>1</sub>		_	0.10		_	—	0.10		
	Φb	0.40	0.50	0.60		0.40	0.50	0.60	·	
Group1	x	_		0.10		_	_	0.10		
	у		_	0.05			—	0.05		
	у У1		_	0.20				0.20		
	n		307		n <sub>max</sub> -16-1		320		n <sub>max</sub> -4	
	M <sub>D</sub>	_	18	-		_	18			
	ME		18	_		_	18			
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.307BNN		レマトリック Full matrix		*See Fig.320BNI	
	S₀		0.40			_	0.40		-	
	SE		0.40	·		_	0.40	_		
	Z <sub>D</sub>		0.70				0.70			
Group2	ZE	_	0.70				0.70			
	Φb <sub>3</sub>		0.50				0.50			
	Φb <sub>4</sub>	1.20	1.30	1.40		_	_	_		
			_	1.20	TFLGA	_		1.20	TFLGA	
				1.00	VFLGA	-	—	1.00	VFLGA	
	A	_	·	0.80	WFLGA	_	_	0.80	WFLGA	
		_		0.65	UFLGA	-	_	0.65	UFLGA	
				0.50	XFLGA			0.50	XFLGA	
		-			DRAWINGS	DATI 2004	E -02-01		SHEET 31/43	

整理番号 467-001-		67-001-CN	N 備考 Remark		4	備考 Remark			
	タイプ al Type	C-FLGA4	67-15.00×1	5.00-0.65		C-FLGA4	180-15.00×1	5.00-0.65	
Refe	·文字 rence nbol	min	nom	max		min	nom	max	
	D		15.00				15.00		
	Ē		15.00	-		·	15.00		
	 V		_	0.20		_	_	0.20	
ľ	w			0.30		_		0.30	
ŀ	e	_	0.65	—		_	0.65	-	
	A		—		*See below	-	-		*See below
	A <sub>1</sub>		—	0.10		_		0.10	
	Φb	0.30	0.40	0.50		0.30	0.40	0.50	
Group1	x		_	0.10				0.10	
F	у	_		0.05		_	—	0.05	
	<b>y</b> 1	—		0.20			_	0.20	
	n		467	—	n <sub>max</sub> -16-1		480	_	n <sub>max</sub> -4
	M <sub>D</sub>	_	22	—		_	22	_	
	M <sub>E</sub>		22				22	_	
	端子配列 Terminal arry		強ランドタイ cement La		*See Fig.467CNN	7	ルマトリック Full matrix		*See Fig.480CN
	SD		0.325	_			0.325		
ŀ	S₌		0.325	—		_	0.325	_	
	ZD		0.675	_		-	0.675	_	
Group2	ZE		0.675	_		_	0.675	_	
-	Фbз		0.40			-	0.40		
	Φb₄	0.95	1.05	1.15		_		_	
[		_	_	1.20	TFLGA	_		1.20	TFLGA
				1.00	VFLGA			1.00	VFLGA
	А	_	_	0.80	WFLGA		_	0.80	WFLGA
			_	0.65	UFLGA		_	0.65	UFLGA
			_	0.50	XFLGA		_	0.50	XFLGA
					DRAWINGS	DAT	E -02-01		SHEET 32/43

整理	里番号				備考				Unit: mm 備考
	Number	8	04-001-DI	NN	Remark	8	37-001-D	NN	Remark
	タイプ nal Type	C-FLGA	304-15.00× <sup>-</sup>	15.00-0.50		C-FLGA	837-15.00×	15.00-0.50	
Refe	☆字 erence mbol	min	nom	max		min	nom	max	
	D		15.00			_	15.00		
	E		15.00	-		_	15.00	-	
	×		-	0.20			- 1	0.20	
	w			0.30				0.30	
	е		0.50	_			0.50	_	
	А		-		*See below		-		*See belov
	A <sub>1</sub>		_	0.10				0.10	
<b>A</b>	Φb	0.20	0.30	0.40		0.20	0.30	0.40	
Group1	x	-	-	0.10			_	0.10	
	у	_	_	0.05		_		0.05	
	<b>y</b> 1	—		0.20		_	-	0.20	
	n		804	-	n <sub>max</sub> -36-1	_	837	-	n <sub>max</sub> -4
	MD	_	29	—		_	29	_	
	ME		29	_		_	29	_	
	端子配列 Terminal arry	補強ランドタイプ Reinforcement Land type			*See Fig.804DNN	7	ルマトリック Full matrix		*See Fig.837DNI
	S₀	_	0.00	_		_	0.00		
Ĩ	SE		0.00	—			0.00	-	
Group2	ZD	_	0.50	-		_	0.50		
	Z <sub>E</sub>	_	0.50	_		_	0.50		
	Фbз	_	0.30	—		_	0.30	—	
	Φb <sub>4</sub>	0.70	0.80	0.90		_	_	-	
ſ		_		1.20	TFLGA		_	1.20	TFLGA
	F	_	_	1.00	VFLGA	_	-	1.00	VFLGA
	Α	_	_	0.80	WFLGA	_		0.80	WFLGA
		_	_	0.65	UFLGA		_	0.65	UFLGA
Ĺ			_	0.50	XFLGA	_		0.50	XFLGA
					RAWINGS	DAT	E -02-01		SHEET 33/43

	ℓ番号 Number	2	72-001-AC	Q	備考 Remark	28	285-001-AQQ		Unit: mm 備考 Remark
	タイプ al Type	C-LGA2	72-17.00×17	7.00-1.00		C-LGA2	85-17.00×1	7.00-1.00	
Refe	☆字 rrence mbol	min	nom	max		min	nom	max	
	D	_	17.00	_			17.00	_	
	E	-	17.00			-	17.00	_	
	v	_	_	0.20		_	_	0.20	
Ì	w	_	· _	0.30				0.30	
	е	_	1.00	_			1.00	_	
	A	_			*See below				*See below
	A <sub>1</sub>		_	0.10			_	0.10	
	Φb	0.50	0.60	0.70		0.50	0.60	0.70	
Group1	x			0.15		_	_	0.15	
	у		_	0.05		_	_	0.05	
·	<b>y</b> 1		-	0.20		-		0.20	
	n		272	-	n <sub>max</sub> -16-1	_	285	_	n <sub>max</sub> -4
	Mp		17	_		_	17		
	ME		17	_		-	17		
	端子配列 Terminal arry		」 強ランドタイ cement La		*See Fig.272AQQ	フルマトリックス Full matrix		*See Fig.285AQ0	
	SD	_	0.00	_			0.00		
	SE		0.00				0.00		
	ZD		0.50			_	0.50		
Group2	ZE		0.50			_	0.50		
-	Φb <sub>3</sub>		0.60			_	0.60	_	
-	Φb <sub>4</sub>	1.50	1.60	1.70		_	_		
[	Т			1.20	TLGA			1.20	TLGA
	ŀ			1.20	VLGA			1.20	VLGA
	A			0.80	WLGA			0.80	WLGA
				0.65	ULGA			0.65	ULGA
	F		<u> </u>	0.50	XLGA			0.65	XLGA
l	l.		I	0.00				0.00	
					ORAWINGS	DATE	E -02-01		SHEET 34/43

[

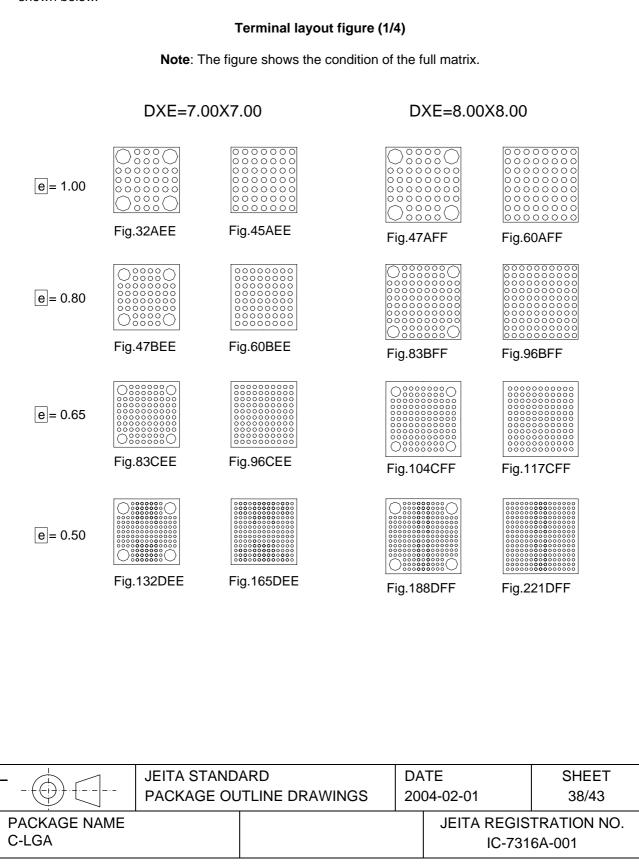
	!番号 Number	4	24-001-BC	QQ	備考 Remark	437-001-BQQ		備考 Remark	
	タイプ ial Type	C-FLGA4	4 <b>24-1</b> 7.00×1	7.00-0.80		C-FLGA4	137-17.00×1	17.00-0.80	
Refe	r文字 erence mbol	min	nom	max		min	nom	max	
	D	_	17.00	_			17.00	_	
	E	_	17.00	_		-	17.00	_	
	v	_	-	0.20				0.20	
	w	1	-	0.30		_	_	0.30	
	е		0.80				0.80	_	
	Ā		-		*See below				*See below
	A <sub>1</sub>	_		0.10				0.10	
	Фb	0.40	0.50	0.60		0.40	0.50	0.60	
Group1	x			0.10		_	_	0.10	
	у	_	_	0.05			-	0.05	
	<b>y</b> 1		_	0.20		_	_	0.20	
	n		424	_	n <sub>max</sub> -16-1	_	437		n <sub>max</sub> -4
	M <sub>D</sub>		21			_	21		
	ME		21			-	21	-	
	端子配列 Terminal arry		, 強ランドタイ rcement La		*See Fig.424BQQ		ルマトリック Full matrix		*See Fig.437BQ0
	SD	_	0.00			_	0.00		
	SE		0.00				0.00	_	
-	ZD		0.50	_			0.50		
Group2	Z <sub>E</sub>		0.50	_		_	0.50	_	
	 Φb <sub>3</sub>		0.50				0.50		
	Φb <sub>4</sub>	1.20	1.30	1.40		_	-		
[			_	1.20	TFLGA		_	1.20	TFLGA
		_		1.00	VFLGA	-		1.00	VFLGA
	A	_	_	0.80	WFLGA	-		0.80	WFLGA
			_	0.65	UFLGA	_	_	0.65	UFLGA
		_	_	0.50	XFLGA		_	0.50	XFLGA
					DRAWINGS	DATI	E -02-01		SHEET 35/43

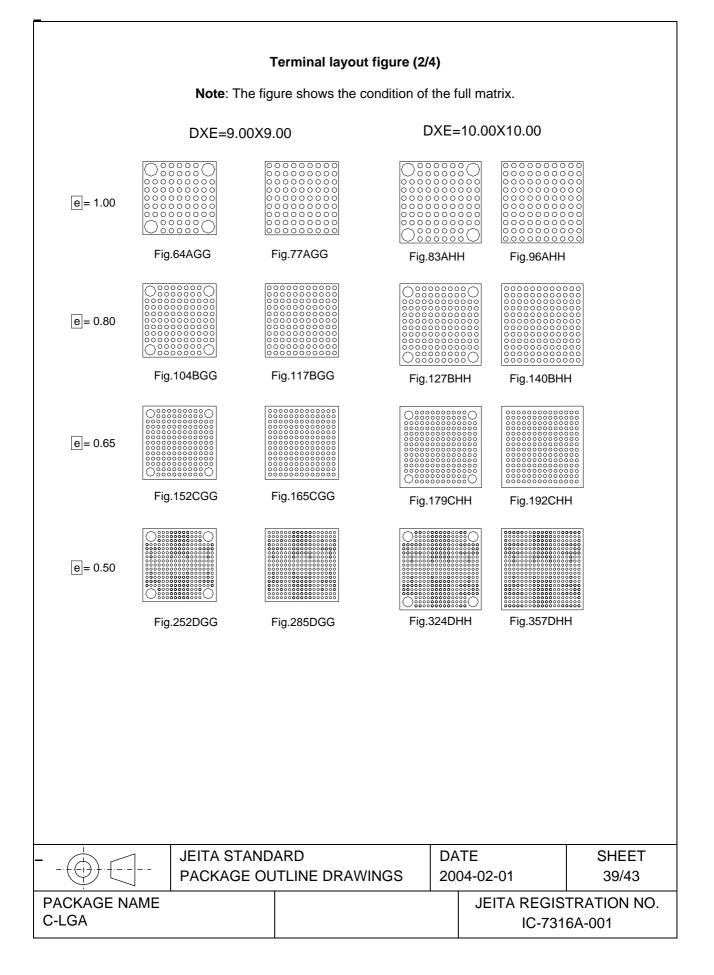
	番号 Number	60	08-001-CC	QQ	備考 Remark	6	621-001-CQQ		備考 Remark
	タイプ al Type	C-FLGA6	6 <b>08-17.00</b> ×1	7.00-0.65		C-FLGA	621-17.00×1	17.00-0.65	
Refe	·文字 rence nbol	min	nom	max		min	nom	max	
	D	_	17.00	_		_	17.00	_	
	Ē		17.00	_			17.00		
	 V			0.20		_	-	0.20	
	w	—		0.30		_		0.30	
Ì	е	_	0.65				0.65		
	A	_	-		*See below		-		*See below
	A <sub>1</sub>		_	0.10			-	0.10	
	Φb	0.30	0.40	0.50		0.30	0.40	0.50	
Group1	x	_		0.10		-	_	0.10	
	у		_	0.05				0.05	
	<u>У</u> 1			0.20			— —	0.20	
	n		608	-	n <sub>max</sub> -16-1	_	621	_	n <sub>max</sub> -4
	M <sub>D</sub>	_	25	-			25		
	M <sub>E</sub>	_	25	_		-	25	_	
	端子配列 Terminal arry		強ランドター cement La		*See Fig.608CQQ	7	レーー・レート ルマトリックス Full matrix		*See Fig.621CQ
	SD		0.00	_		_	0.00	_	
	SE	_	0.00	<u> </u>			0.00	_	
-	ZD		0.70				0.70		
Group2	Z <sub>E</sub>		0.70				0.70	_	
	Φb <sub>3</sub>	_	0.40			_	0.40		
	Φb <sub>4</sub>	0.95	1.05	1.15		_		_	
[		_	_	1.20	TFLGA	-		1.20	TFLGA
		_	_	1.00	VFLGA			1.00	VFLGA
	A		_	0.80	WFLGA	—		0.80	WFLGA
				0.65	UFLGA			0.65	UFLGA
		-	_	0.50	XFLGA	_	_	0.50	XFLGA
<u></u>		JEIT			DRAWINGS	DAT	E -02-01		SHEET 36/43

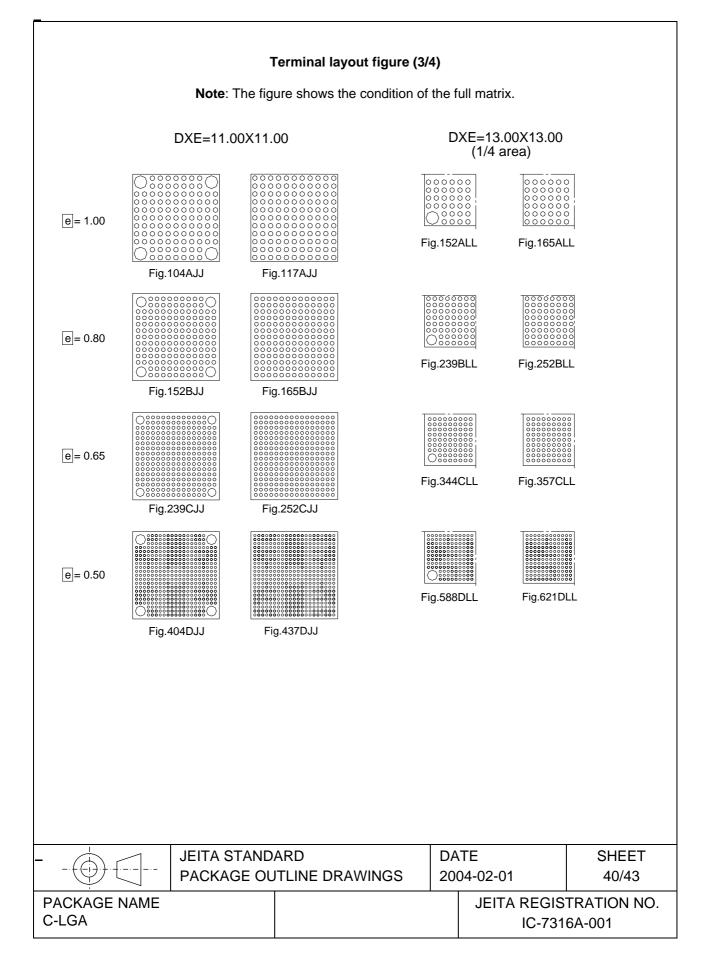
	፤番号 Number	10	52-001-D	QQ	備考 Remark	10	1085-001-DQQ		備考 Remark
	タイプ al Type	C-FLGA1	052-17.00×	17.00-0.50		C-FLGA1	085-17.00×	17.00-0.50	
Refe	♪文字 erence mbol	min	nom	max		min	nom	max	
	D	_	17.00			_	17.00	_	
	E	_	17.00				17.00		
	v	_	-	0.20			_	0.20	
	w		_	0.30				0.30	
	e	_	0.50	_		-	0.50	—	
	A	_	-		*See below	_			*See belov
	A <sub>1</sub>	_	_	0.10			_	0.10	
_	Φb	0.20	0.30	0.40		0.20	0.30	0.40	
Group1	x		_	0.10			_	0.10	
	у	_	-	0.05		_	-	0.05	
	<b>y</b> 1		—	0.20		—		0.20	
	n	_	1052	_	n <sub>max</sub> -36-1	_	1085	_	n <sub>max</sub> -4
	MD	_	33	_			33	_	
	M <sub>E</sub>	_	33	—		_	33		
	端子配列 Terminal arry	補強ランドタイプ Reinforcement Land type			*See Fig.1052DQQ	7	ルマトリック Full matrix		*See Fig.1085DQ
	S₀	_	0.00	_			0.00	_	
	SE	_	0.00			_	0.00	—	
	ZD	_	0.50			_	0.50	_	
Group2	Z <sub>E</sub>		0.50	_		_	0.50		
	Φb <sub>3</sub>		0.30	_			0.30	_	
	Φb <sub>4</sub>	0.70	0.80	0.90		_	_	-	
			_	1.20	TFLGA			1.20	TFLGA
			-	1.00	VFLGA		_	1.00	VFLGA
	А			0.80	WFLGA	_	-	0.80	WFLGA
			—	0.65	UFLGA		_	0.65	UFLGA
			_	0.50	XFLGA	_	_	0.50	XFLGA
			A STAN		DRAWINGS	DAT	E -02-01		SHEET 37/43

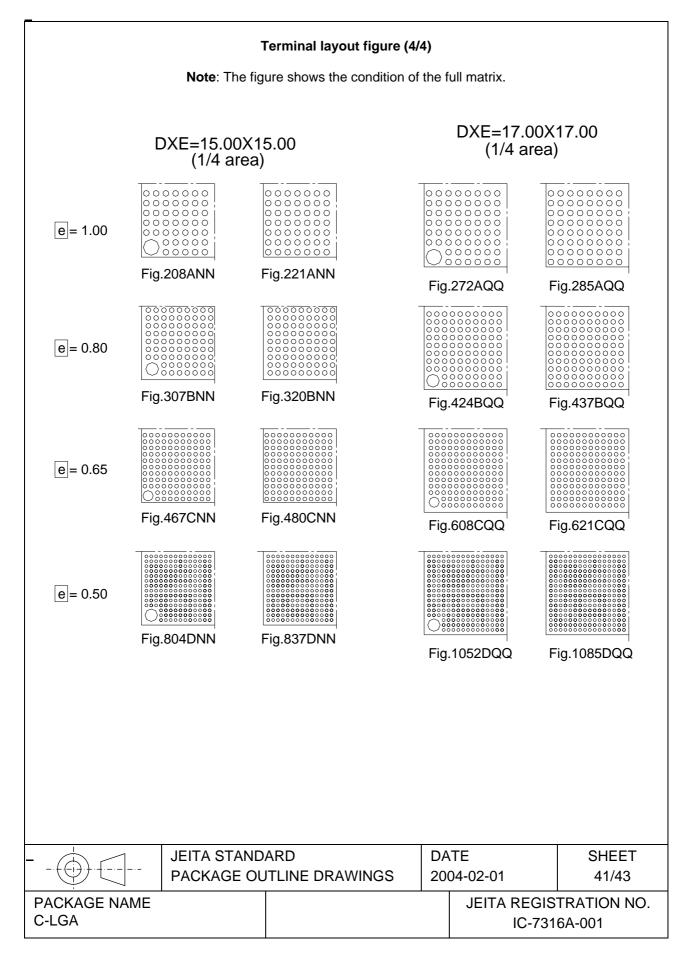
# 9. Terminal layout figure

As assistance in the design and development of new package in the future, **Terminal layout figure** shown below.









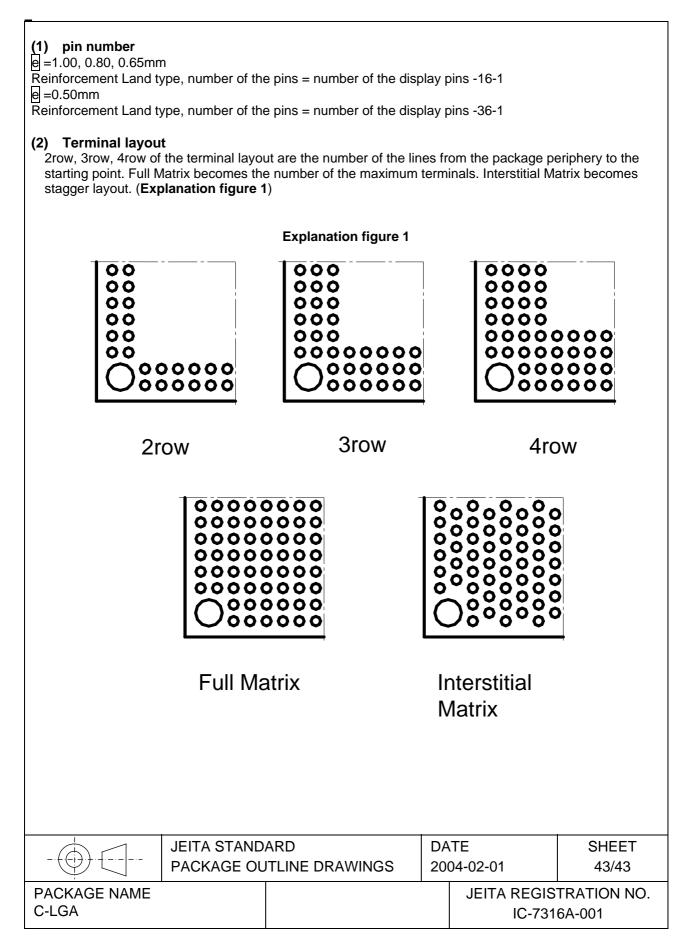
# 9.1 Terminal layout

C-LGA

As assistance in the design and development of new package in the future, **Terminal layout table** shown below. **Terminal layout table** 

								pin	number
				Termina	Pitch	n e			
		1.00		0.80		0.6	5	0.50	C
	7x7	Full M=7	45	Full M=8	60	Full M=10 3row 2row	80	Full M=13 5row 4row	165 156 140
								3row 2row	116 84
	8x8	Full M=8 2row	60 44	Full M=10 3row	80	Full M=11 4row	108	Full M=15 5row	221 196
				2row	60	3row 2row		4row 3row 2row	172 140 100
	9x9	Full M=9 3row 2row	77 68 52	Full M=11 4row 3row	108 92	Full M=13 5row 4row	156 140	Full M=17 5row 4row	285 236 204
				2row	68	3row 2row		3row 2row	164 116
	10x10	Full M=10 3row 2row	96 80 60	Full M=12 4row 3row 2row	140 124 104 76	Full M=14 5row 4row 3row	176 156 128	Full M=19 5row 4row 3row	357 276 236 188
Δ	11x11	Full M=11	117	Full M=13	165	2row Full M=16		2row Full M=21	132 437
× Ш		4row 3row 2row	108 92 68	5row 4row 3row	156 140 116	5row 4row 3row	216 188	5row 4row 3row	316 268 212
		2100	00	2row	84	2row	108	2row	148
	13x13	Full M=13 5row 4row	165 156 140	Full M=16 5row 4row	216 188	Full M=19 6row 5row	308 276	Full M=25 5row 4row	621 396 332
		3row 2row	116 84	3row 2row	152 108	4row 3row 2row	188	3row 2row	260 180
	15x15	Full M=15 6row	221 212 196	Full M=18 6row	320 284 256	Full M=22 6row	380	Full M=29 5row	837 476 396
		5row 4row 3row 2row	172 140 100	5row 4row 3row 2row	220 220 176 124	5row 4row 3row 2row	284 224	4row 3row 2row	308 212
	17x17	Full M=17 5row 4row 3row	285 236 204 164	Full M=21 5row 4row 3row	437 316 268 212	Full M=25 5row 4row 3row	396 332	Full M=33 5row 4row 3row	1085 556 460 356
		2row 2row Matrix) - (4corner of rows from the	116 • not co	2row 2row	148	2row		2row	244
		JEITA STAN			29	DATE 2004-			SHE 42/4
					50	2004-	02-01		42/4

IC-7316A-001



# **EXPLANATORY NOTES**

#### 1. Objective of establishment

This standard aims to be standardized by the industry of the package which Ceramic Land Grid Array (hereinafter referred to as C-LGA) and Ceramic Fine pitch Land Grid Array (hereinafter referred to as C-FLGA) that the package carrier material is ceramic. It was established to provide the design guideline when it is made in to product or when Automatic mounting machinery and associated parts are developed.

#### 2. History of review

In early 1995, the Society for the Study of CSP (Chip Scale Package) (its antecedents of the Society for the Study of Next Generational Packages) was established under the Mounting Technical Committee on Semiconductor. Device Packages and had investigated CSP, possibility of standardizing their external dimensions, and so on. The standardization of CSP had been proceeded at the Technical Standardization Committee on Semiconductor Device Packages based on the report from the Society for the Study of CSP, and the furthermore investigations for its standardization have been done at Area Array Package Committee (currently, Integrated Circuits Package Subcommittee), since October 1995.

#### (1) FBGA/FLGA design guide

In the half of 1990's, by the rise of the market needs of rapid FBGA and FLGA, their standard of the package outlines in the market avoids confusion, which is not. Therefore, the deliberation on the square types of Fine pitch BGA and LGA was done and **EIAJ EDR-7316** (hereinafter referred to as "FBGA / FLGA Design guideline") was issued in April 1998, which based on **EIAJ EDR-7315A** (hereinafter referred to as "BGA design guideline"), which the earlier published in half of 1990's. In the 2nd half of 1990's, the market needs of FBGA and FLGA for memory use are raised, and the standardization of package outlines of rectangular type is required. The deliberation on this had started in November 1998. Its deliberation had been proceeded based on the FBGA/FLGA design guideline (**EIAJ EDR-7316**) with its correction and/or addition. The practical activities were completed in May 1999, and Semiconductor Package Standardization Committee approved the final draft of the provisional standard, which was valid by March 2001, and it was issued as **EIAJ EDX-7316**. Related Committee brought forward problems of difference of square type and rectangular type standards (**EIAJ EDR-7316**, **EIAJ EDX-7316**). So these standards had unified and **EIAJ EDR-7316A** published in April 2002.

Rectangular type FBGA/FLGA design guide was proposed to **SC 47D** from Japan, **SC 47D** take charge of the standardization of the semiconductor package outline of **International Electrotechnical Commission** (hereinafter referred to as **IEC**). And 2 standards of the following are established.

**IEC 60191-6 -11** General Design guide for FBGA (Rectangular Type), establishment in June, 2002. **IEC 60191-6 -12** General Design guide for FLGA (Rectangular Type), establishment in June, 2002.

#### (2) C-LGA/ C-FLGA standard

In Area Array Package Committee, deliberation and establishment of C-LGA/C-FLGA standards were carried forward from 1998 to 2000 in parallel with deliberation of FBGA/FLGA design guide. And 3 standards of following are established.

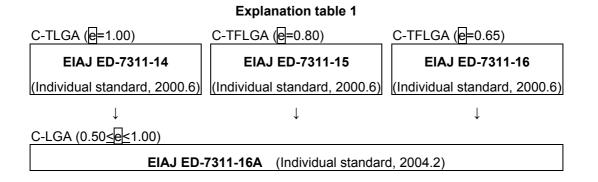
- EIAJ ED-7311-15 (Standard of integrated circuits package, C-TFLGA (0.80mm pitch)), establishment in June, 2000.
- **EIAJ ED-7311-16** (Standard of integrated circuits package, C-TFLGA (0.65mm pitch)), establishment in June, 2000.

Since 2000, to make terminal pitch a fine moves ahead, in coming to practical use spreading about C-FLGA that terminal pitch is 0.50 mm, too. To deliberate following contents as the standard to have integrated the standard of the three above into in Integrated Circuits Package Subcommittee and to establish were fixed in April, 2003.

It adds terminal pitch e =0.50mm, 0.40mm

It corresponds to package's becoming thinner, It prescribes seating height,  $A_{max}$  = equal to or less than 1.00mm (code: v).

The deliberation ends in Integrated Circuits Package Subcommittee in December 2003. **EIAJ ED-7311-16A** (Standard of integrated circuits package, C-LGA), establishment in February, 2004. The deliberation elapses of C-LGA relation standards are shown in **Explanation table 1** with the flow chart.



FLGA, FBGA design guide (0.40 < e < 0.80)

EIAJ EDR-7316A (Design guide, 2002.6)

After that, C-LGA relation standard is proposed to **IEC SC47D** from Japan and 2 standards of the following are established.

Amendment 1 to IEC 60191-2 C-FLGA 0.8 mm pitch / 1.0mm pitch, establishment in March 2001.

Amendment 2 to IEC 60191-2 FLGA Family 0.8 0.65 and 0.5mm pitch, establishment in March 2001.

**EIAJ ED-7311-14** (Standard of integrated circuits package, C-TLGA (1.00mm pitch)), establishment in June, 2000.

#### 3. Background of the dimension rule

#### (1) Datum

Datum was determined by the terminals, because it was an important parameter during package mounting, especially for fine pitch packages. However, as it is necessary to get a consensus of **Joint Electron Device Engineering Council** (hereinafter referred to as **JEDEC**), datum line definition Determined centers of opposite sides of a package is adapted. Details of the rule way are shown in **4**. **definition of the datum**.

#### (2) Nominal dimension

At **EIAJ EDR-7316A** (FBGA/FLGA design guide), it took a consistence to be **JEDEC** and it decided to display in combination (DXE) with package length and width. Defined as the numerical representation of the package length against the package width, considering up to one decimal place of the actual dimensions for Flanged type packages. In the case of Real chip size type packages, it is defined as the numerical representation of the package length against the package width, considering up to two decimal places of the actual dimensions (3rd digit the following of the decimal point abandons), which is necessary to express the CSP concept.

#### (3) Background on the revision of package length and width (D, E) definition

Based on **EIAJ EDR-7315A** (BGA design guide), the vertical direction defines the package width (D), while the horizontal direction defines the package length (E), upon the condition that the package index is located on the lower left side from the package bottom view. The following two problems arose from this definition.

- (a) When we apply this to the trend of rectangular type BGA package in the market, statements such as " Package width is larger than the package length " will be opposed by " Package length is larger than the package width ".
- (b) This definition of package length and package width contradicts the JEDEC design guide. In order to avoid confusion in the industry, we opted to change the definition of the vertical direction as the package length (D) and the horizontal direction to be the package width (E) upon the condition that the package index is located on the lower left side from the package bottom view. Also, we did not define to correlate package length and package width according to size. Since ball layout is defined in a standard, size correlation of package length and package width shall be reversed by a normal ball matrix and memory chip size.

#### (4) Package length (D) and width (E)

It thinks that the about 20.00 mm SQ chip is the biggest when thinking by the technology level of the present situation. Considering the size, which is prescribed by the **EIAJ EDR-7315A** (BGA design guide), Maximum size was defined to be 21.00mm, which is the same as in the FBGA/FLGA design guide. Minimum size was defined to be 1.50mm, which will allow possibility of further minimizing the package size.

In the previous standards (**EIAJ ED-7311-14** (C-TLGA (1.00mm pitch)), **EIAJ ED-7311-15** (C-TFLGA (0.80mm pitch)), **EIAJ ED-7311-16** (C-TFLGA (0.65mm pitch)), only A<sub>max</sub>=1.20mm (code: T) was prescribed. **EIAJ ED-7311-16A** (C-LGA) prescribed A<sub>max</sub> = 1.20, 1.00, 0.80, 0.65, 0.50mm (code: T, V, W, U, X), according to the IEC standard. A name by package seating height repartition is shown in **Explanation table 2**.

	Explanation table 2								
	Terminal pitch e								
A <sub>max</sub>	1.00	0.80	0.65	0.50	0.40	0.30			
1.70>	LGA	FLGA							
1.70	LLGA	LFLGA							
1.20	TLGA	TFLGA							
1.00	VLGA	VFLGA							
0.80	WLGA	WFLGA							
0.65	ULGA	UFLGA							
<u>&lt;</u> 0.50	XLGA	XFLGA							

Explanation table 2

#### (6) Stand off height (A<sub>1</sub>)

#### (a) FBGA

When making a ball diameter 60% of terminal pitch, 50% of terminal pitch was equivalent to ball height was confirmed by simulation and measurement, it is defined nom. value with standoff height. Stand off height was defined to express min., nom. and max. values. It was considered for socket which is used for Auto mounter and testing. The recommended nom. value is 50% of the package terminal pitch. However, in the case of 0.45mm ball diameter with 0.80mm pitch, which was added as a ball diameter option, stand off height is defined at nom. 0.35mm.

#### (b) FLGA

There are two terminal type for FLGA, flat type and bump type. Stand off height was defined to be  $A_{1 max}$  = less than 0.10mm to distinguish from FBGA.

#### (7) Package height (A<sub>2</sub>)

It shows package height (A<sub>2</sub>) in "  $A_{2 max} = A_{max} - A_{1 max}$ ". LGA becomes "  $A_{2 max} = A_{max} - 0.10$ mm ", because to be provided by  $A_{1 max} =$  equal to or less than 0.10 mm.

# (8) Terminal pitch (e)

Algorithm of 80% reduction was applied as the conventional packages. The basic pitch is 1.00mm and other pitches defined for this design guideline are 0.80/0.65/0.50/0.40mm.

#### (9) Terminal diameter (φb)

#### (a) FBGA

The preferable terminal diameter is defined as 60% of terminal pitch. In the case of 0.80mm pitch,  $\varphi$ 0.45mm and  $\varphi$ 0.40mm were considered to add to this design guideline, because  $\varphi$ 0.50mm (60% of terminal pitch) might be difficult for manufacturing. Then, it is decided to add  $\varphi$ 0.45mm as an option, and not to add  $\varphi$ 0.40mm, after the feasibility study of routing of circuit and socket.

#### (b) FLGA

In the same way FBGA, terminal diameter is defined as 60% of terminal pitch. However, plastic type is defined as 50% of terminal pitch. Because when making a ball diameter in FBGA 60% of terminal pitch, Land diameter of ball installation part becomes 50% of terminal pitch. It considered design of wiring pattern and sharing of the package substrate of FBGA and FLGA. At ceramic type, it stores up that linear expansion coefficient difference from printed circuit board is big. Therefore, to secure a temperature cycle characteristic in mounting device, it needed 60% of size of terminal diameter.

#### (10) Reinforcement Land (φb<sub>4</sub>)

As for in mounting of C-LGA, heat shrinkage difference from printed circuit board is big. Therefore, package with reinforcement Land becomes necessary to secure mounting strength by size and terminal pitch of package. In this standard, it prescribed reinforcement Land ( $\phi b_4$ ) in 4 corners, which stress to package concentrates.

	Reinforcement	Terminal
Terminal pitch	Land diameter	diameter
е	φb <sub>4 nom</sub>	φb <sub>3 nom</sub>
1.00	1.60	0.60
0.80	1.30	0.50
0.65	1.05	0.40
0.50	0.80	0.30

**Explanation table 3** 

#### (11) Parallelism of package top surface (y<sub>1</sub>)

Taking into account the limitation of the pick-up of the automatic mounter specified parallelism of top surface.

#### (12) Terminal co planarity (y)

It adopted the rule of QFP, which is consolidated by the identical printed circuit board.

#### (13) Positional tolerance of terminal (x)

At **EIAJ EDR-7316A** (FBGA/FLGA design guide), about 10% of terminal pitch is specified. However,  $X_{max}$ =0.10mm of the terminal pitch were equal to or less than 0.80mm from the ability value in case of manufacture.

#### (14) Tolerance of package lateral profile (v) and Package center offset (w)

At **EIAJ ED-7311-16A** (FBGA/FLGA design guide), as for Tolerance of package lateral profile (v) and Package center offset (w), it fixed questionnaire investigation by the doing. Tolerance of package lateral profile (v) decided acceptance value on the consideration, which h it was possible to sometimes adjust in package outline at the user. Also, it fixed Package center offset (w), which from the ability value in case of mounting.

#### (15) Number of terminal matrixes (M<sub>D</sub>, M<sub>E</sub>) rule

Maximum number for terminal matrixes (hereafter referred to as maximum terminal matrixes) M  $_{max}$  ( $M_{D max}$ ,  $M_{E max}$ ) was set as an integer which satisfied the inequality noted below, and this integer was stipulated as the standard number of terminal matrixes.

 $M_{D \max} \le (D - b_{\max} - v - w - x - 2 (E.C.))/e + 1$ 

 $M_{E \max} \le (E - b_{\max} - v - w - x - 2 (E.C.))/e + 1$ 

- D,E : Package length and width
- b<sub>max</sub> : Maximum terminal diameter(b<sub>nom</sub> + terminal diameter tolerance)
- v : Tolerance of package lateral profile
- w : Tolerance of package center offset
- x : Positional tolerance of terminal
- E.C. : Edge clearance (0.11mm)
- e : Terminal pitch

Also for D, E, the M<sub>D max</sub> and M<sub>E max</sub> determined as shown above, and the same figure with one row less (offset by one half-pitch), indicated that (M<sub>D max</sub> -1) by (M<sub>E max</sub> -1), were added to the stipulation as standard terminal matrixes. Furthermore (M<sub>D max</sub> +1) by (M<sub>E max</sub> +1) only for FLGA were added, if E.C. > 0 is satisfied.

#### (16) Background of calculation that number of terminal matrix

#### (a) Maximum number of terminal matrix ( $M_{max}$ )

At first, M <sub>max</sub> is though assumed the number in the range where the terminal edge does not begin to see the package edge, which can be maximum arranged. There is a demand by which the structure of the tray is assumed to be terminal non-contact to FBGA. Need the area (edge clearance) where some ball does not exist between terminal edge and package edge to prevent the transformation of the ball by the contact of an unexpected ball or the dropout at handling by the maker and the user. That was proposed from semiconductor packing sub-committee and **JEDEC JC-11**, and it was assumed that this was adopted.

# (b) Offset by one half-pitch maximum number of terminal matrix ( $M_{max}$ -1)

It provided for (M <sub>max</sub>) as a number of standard terminal matrix, also it provided for (M<sub>max</sub> -1) as offset by one half-pitch number of standard terminal matrix. Number of terminal matrix of both even and odd number of all package externals provided and can be selected by providing for both M<sub>max</sub> and M<sub>max</sub> -1 as a number of standard terminal matrix. Moreover, in case of FLGA, so a part of package externals was assumed to admit (M<sub>max</sub> +1) in the combination from being able multi array (M<sub>max</sub> +1) from M<sub>max</sub> when pitches were combined by one row about FLGA because there was no ball.

#### (17) Number of terminals (n)

The maximum terminals is n  $_{max}$  = M<sub>E</sub>X M<sub>D</sub>. The number of maximum terminals is the latently existing number of terminals. Therefore, as for the fact, the terminal often comes off partially. Then the maximum terminals don't often agree with the actual number of the terminals. (Example: It is depopulation in the package 4 corner). When described according to **EIAJ ED-7303B** [Name and Code for Integrated Circuits Package], The pin display which is in the deficit becomes as it is (Example 64/100), however in case of BGA and LGA, it writes at the number of existing terminals(n).

In case of C-LGA, on the reliability of the mounting, it decided not to recommend a terminal in the package 4 corner as the electric connection terminal especially. Therefore, it provided with  $n_{max} - 4$ .

When prescribing reinforcement Land in the package 4 corners, it calculates by the formula below.

terminal pitch e =1.00, 0.80, 0.65mm (It makes 4 pins of the package 4 corner reinforcement Land.)

Number of terminals with reinforcement Land (n) = number of maximum terminals (n  $_{max}$ ) -16-1(index) terminal pitch e =0.50mm (It makes 9 pins of the package 4 corner reinforcement Land.)

Number of terminals with reinforcement Land (n) = number of maximum terminals (n  $_{max}$ ) -36-1(index)

#### (18) The 1 pin display

The example of the concrete way of displaying about the 1 pin display for the automatic mounting machinery to recognize the direction of the package using the terminal, the way of adding one terminal to the corner part with the most internal circumference and the way of removing one terminal of A1 and so on were thought of. However, to prescribe the index display to have standardized on and for it to be unified didn't result in an arrangement for the following reason.

There are the package, which is depopulation terminals in 4 corners already, and the package that the space, which arranges a terminal in the corner part with the most internal circumference, isn't provided for. Also, the point that the user doesn't unify a request to the 1 pin display, too, is the reason. However, actually, in the form according to this, a 1 pin display is implemented.

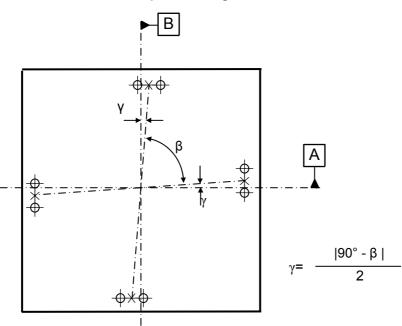
#### (19) Center terminal position in package width, length direction( $S_E$ , $S_D$ )

It prescribes the position of the terminal which is arranged in the nearest position to the datum line of the package center A, B. When the number of matrix (M) is an odd number,  $S_E = S_D = 0$ , when even number,  $S_E = S_D = e/2$ .

#### 4. Datum definition

So far the method for calculate the datum  $\boxed{A}$  and  $\boxed{B}$  was using ball positions. However, as it is necessary to get a consensus of opinion of **JEDEC**, and it adopts with ball datum definition, there is not a change but the definition way is definite, which is prescribed by clear **EIAJ ED-7304** (BGA measuring method). It is shown below about the definition.

Centers of opposite sides of a package, which are defined below, shall be connected together. An angle  $\beta$  subtended by the two crossing lines shall be obtained. A difference  $|90^{\circ} - \beta|$  of the angle  $\beta$  from  $90^{\circ}$  shall be equally distributed to the sides to obtain orthogonal axes. The orthogonal axes are depicted as datum lines  $\overline{A}$  and  $\overline{B}$  of the package.

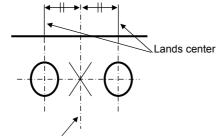


**Explanation figure 1** 

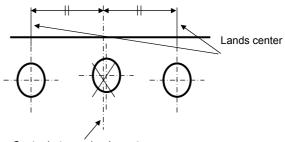
Definition of the center of side



Explanation figure 3 For an odd number



Center between lands center



Center between lands center

#### 5. The reference standard

#### (1) IEC standard

Revision of IEC 60191-6 Global drawing format, establishment schedule in 2004
IEC 60191-6 -11 General Design guide for FBGA (Rectangular Type), establishment in June 2002.
IEC 60191-6 -12 General Design guide for FLGA (Rectangular Type), establishment in June 2002.
Amendment 1 to IEC 60191-2 C-FLGA 0.8 mm pitch / 1.0mm pitch, establishment in March 2001.
Amendment 2 to IEC 60191-2 FLGA Family 0.8 0.65 and 0.5mm pitch, establishment in March 2001.
IEC 60191-6-4/Ed.1 BGA (Ball Grid Array) package measuring method, establishment in XXXX 2002.

#### (2) JEDEC standard

- **MO-222A** Very Thin Profile, Fine Pitch Land Grid Array Family 0.5 / 0.65mm pitch. SQ/RECT. establishment in February 2000.
- **MO-225A** Very Thin Profile, Fine Pitch Ball Grid Array Family 0.5 / 0.65mm pitch. SQ/RECT. establishment in February 2000.
- (3) JEITA standard
  - **EIAJ ED-7311-14** (Standard of integrated circuits package C-TLGA(1.00mm pitch)), establishment in June 2000.
  - **EIAJ ED-7311-15** (Standard of integrated circuits package C-TFLGA(0.80mm pitch)), establishment in June 2000.
  - **EIAJ ED-7311-16** (Standard of integrated circuits package C-TFLGA(0.65mm pitch)), establishment in June 2000.
  - EIAJ ED-7311-16A (Standard of integrated circuits package C-LGA), revised in February 2004.
  - **EIAJ EDR-7315A** (Design guideline of integrated circuits for Ball Grid Array (BGA)), establishment in November 1998.
  - **EIAJ EDR-7316A** (Design guideline of integrated circuits for Fine Pitch Ball Grid Array / Fine Pitch Land Grid Array (FBGA/FLGA)), establishment in April 2002.
  - **EIAJ ED-7300** (Recommended practice on standard for the preparation of outline drawings of semiconductor packages), establishment in August 1997.
  - EIAJ ED-7303B (Name and Code for Integrated Circuits Package), revised in September 2002.

# 6. COMMITTEE MEMBERS

The IC Package Subcommittee of the Technical Standardization Committee on Semiconductor Device Packages has mainly deliberated this standard. The subcommittee members are shown below.

<Technical Standardization Committee on Semiconductor Device Package>

< rechnical Standa	rdization Committee on Semiconductor Device Packag	e>
Chairman	SONY CORP.	Kazuo Nishiyama
< IC Package Subo	committee>	
Chief	RENESAS TECHNOLOGY CORP.	Kazuya Fukuhara
Co- chief	TOSHIBA CORP.	Yasuhiro Koshio
	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.	Tomohiro Tamaki
Members	AMKOR THECHNOROGY JAPAN. INC	Kazuaki Sorimachi
	ELPIDA MEMORY, INC.	Fumitake Okutsu
	ENPLAS CORP.	Takayuki Yamada
	OKI ELECTRIC INDUSTRY CO., LTD.	Yoshihiko Ino
	SANYO ELECTRIC CORP.	Hideyuki Iwamura
	SANYO ELECTRIC CORP.	Kiyoshi Mita
	SUMITOMO 3M CORP.	Koji Kukimoto
	SEIKO EPSON CORP.	Yoshiaki Emoto
	SONY CORP.	Nobuhisa Ishikawa
	DAI NIPPON PRINTING CO., LTD.	Hiroyuki Saito
	TEXAS INSTRUMENTS JAPAN LTD.	Takayuki Ohuchida
	NEC ELECTRONICS CORP.	Khoichi Hirosawa
	HITACHI CABLE LTD.	Tsuyoshi Ishihara
	FUJITSU LTD.	Michio Sono
	FUJI ELECTRIC CO., LTD.	Osamu Hirohashi
	MELCO INC.	Tsuneo Watanabe
	UNITECHNO INC.	Hitoshi Matsunaga
	ROHM CO., LTD.	Sadamasa Fujii
Special Members	SHIN-ETSU POLYMER	Ken Tamura
	TOYOJUSHI CO., LTD.	Hitoshi Kazama
<working group=""></working>		
Leader	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.	Toshiyuki Fukuda
	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.	Sigeru Nonoyama
	KYOCERA CORP.	Akihiko Funahashi
	YAMAICHI ELECTRONICS CO., LTD.	Noriyuki Matsuoka