

Standard of Electronic Industries Association of Japan

EIAJ ED-7311-6

Standard of integrated circuits package [60/90pins Fine-pitch Ball Grid Array (FBGA)]

Established in April, 1998

Prepared by

Technical Standardization Committee on Semiconductor Device Package

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Electronic Industries Association of Japan

5-13, Nishi-shinbashi 1-chome, Minato-ku, Tokyo 105-0003, Japan Printed in Japan — 登録一覧表 Registration Table ————

パッケージ名称:P-TFBGA(0.80mm pitch)

Package Name

登録番号: IC-0000-002

Registration No.

]	端子直線間隔 [Terminal pitcl	e n
	0. 80	
	60-002-AA	
	90-002-AB	

注 表中の数値は、「(端子数n) -(連番)-(整理番号)」を示す。

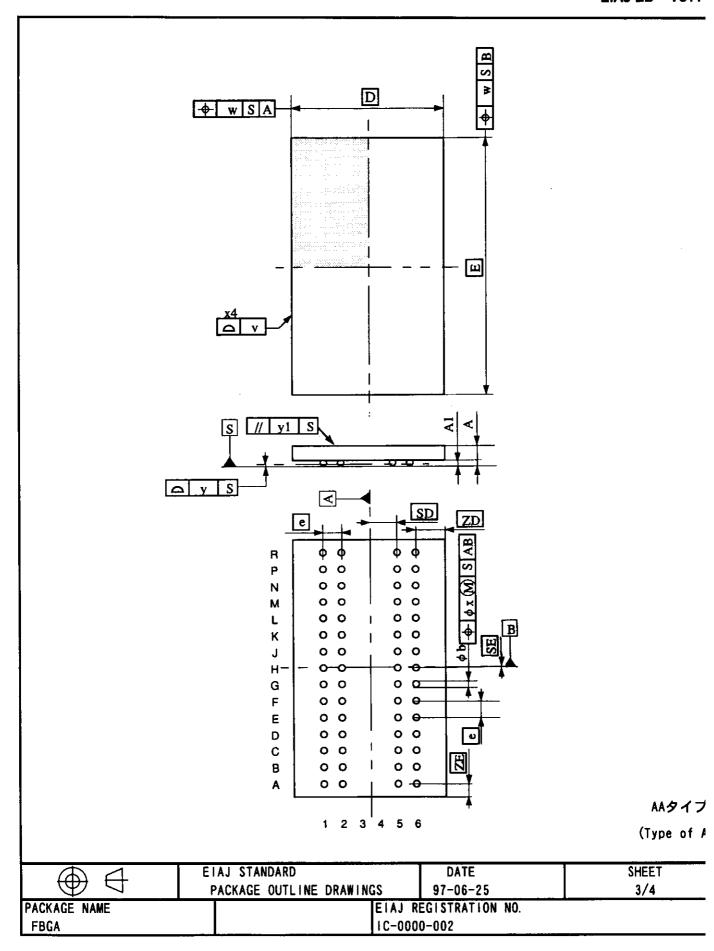
Note: Numerals in the Table indicate "(Terminal number n)-(Consecutive number)-(Serial number

Ф 4	EIAJ STANDARD	DATE	SHEET
	PACKAGE OUTLINE DRAWINGS	97-06-25	1/4
PACKAGE NAME	ĮE	IAJ REGISTRATION NO.	
FBGA] :	C-0000-002	

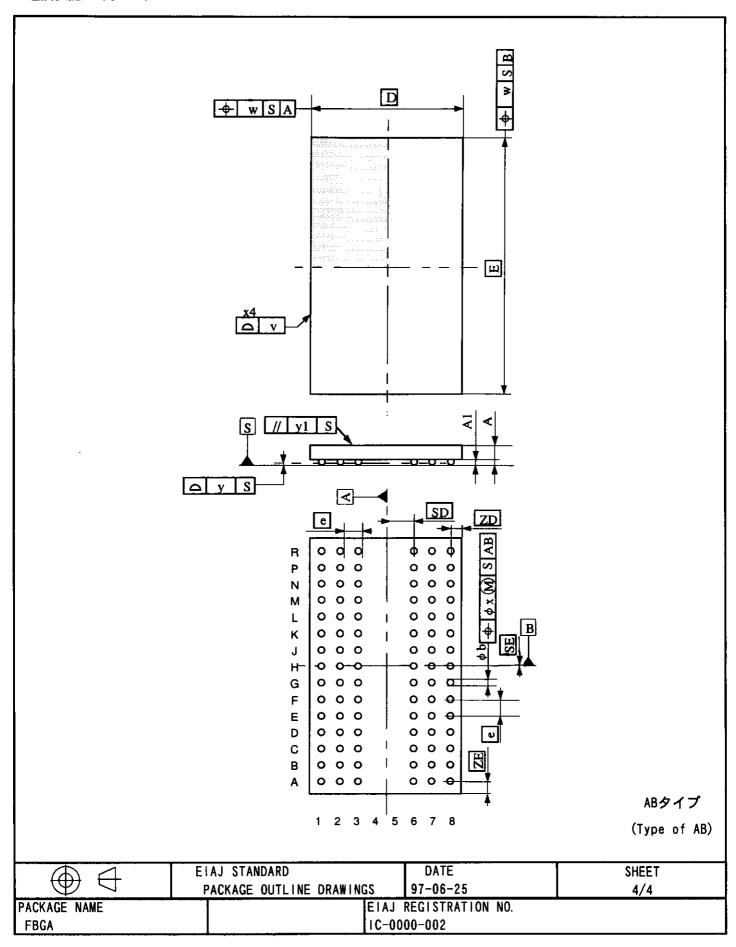
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整理番号 Serial Number		АА		АВ			
外形タイプ Extermal Type		P-T F B G A-6 0-0.80		P-TFBGA-90-0.80			
照合文字 Reference Symbol		min	nom	max	min	nom	max
D			4. 90~14. 00			6. 50~14. 00	
<u> </u>	E		12. 10~22. 00			12. 10~22. 00	
	L v			0. 15			0. 15
	w			0. 20			0. 20
A PLANT S P N N N N N N N N N N N N N N N N N N	Α			1. 20			1. 20
	A 1	0. 35	0. 40	0. 45	0. 35	0. 40	0. 45
	е		0. 80			0. 80	
	b	0. 45	0. 50	0. 55	0. 45	0. 50	0. 55
	х			0. 08			0. 08
	У			0. 10			0. 10
	y 1			0. 20			0. 20
	n		60			90	
	MD		6			8	
	ME		15			15	
グループ 2 Group2	S D		1. 2			1. 2	
	SE						
	ZD		0. 45~5. 00			0. 45~3. 80	
	ZE		0. 45~5. 40			0. 45~5. 40	

A 4	EIAJ STANDARD	DATE	SHEET
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FBGA	+C-00	000-002	



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COMMENTS

1. PROCESS OF DELIBERATION

FBGA includes not only Flanged type but also Real Chip Size type where the device decides the package dimension, therefore, the device size is required to be clarified. To decide the package size, it must be considered that the manufacturers have the various device types and the devices vary depending on the generation. We actually surveyed to decide the size, however, it was concluded that it was technically too difficult to decide a package size. As a result, it was decided to enable the device sizes to be converted and unify the minimum terminal arrangements.

Thus, the FBGA length and width (dimension D and E) are not unified. Instead, the maximum outer dimension estimated by each manufacturer including the minimum area where the terminal can fit was established as the dimension provision based on the agreement between the manufacturers. For terminal pitch and other dimensions, it was decided to comply with the square FBGA design guide based on the agreement between the manufacturers.

2. REVIEW COMMITTEE MEMBERS

The standard was mainly reviewed by the Subcommittee on Area Array Package, and Project Group of Technical Standardization Committee on Semiconductor Device Package of which members are as follows.

<technical committee="" device="" on="" package="" semiconductor="" standardization=""></technical>					
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