Standard of Electronic Industries Association of Japan

EIAJ ED-7441B

Standards for the packages of universal memory devices

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Prepared by
Technical Standardization Committee on Semiconductor Device Package

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The standard of the Electronic Industries Association of Japan

Standard for the package of universal Memory Devices

1. Scope

This standard sets the standards to be applied to standard package for widely used DRAM, SDRAM, VRAM, SRAM, HSSRAM, PROM, and MROM chips.

2. HISTORY

Semiconductor memory devices are widely used as universal, then the standardization of the configuration and compatibility are important.

The standard to be used in the standardization of universal memory devices will be augmented and improved as soon as new memory devices are introduced. Moreover, we will continuously evaluate and determine the compatibility of all types of memory devices.

3. DEFINITION OF TERMS

The definition of the majority of the terms used in this standard complies with the **EIAJ ED-7300** and **ED-7303**. The new terms not included therein shall be defined as follows.

(1) DRAM (Dynamic Random Access Memory)

Memory cells used for storing data, a type of RAM that has to be refreshed at regular intervals. (these cell enable read and write operations)

(2) SDRAM (Synchronous DRAM)

One type of DRAM. Data input and output are operated synchronously with clock pulse.

(3) VRAM (Video RAM)

RAM with two or more I/O ports used for efficient reading and writing of video and other display data.

(4) SRAM (Static RAM)

A RAM device that can maintain data without the need for internal or external control signals.

(5) HSSRAM (High Speed SRAM)

A specially designed SRAM which is faster than an ordinary SRAM device.

(6) PROM (Programmable Read Only Memory)

Each cell data of the write area can be erased or rewritten.

(7) MROM (Mask ROM)

A ROM with data in the write area written to a mask at the production of the integration circuit.

4. METHODS FOR STANDARDIZING UNIVERSAL MEMORY DEVICE PACKAGES

4.1 STANDARD PACKAGE SELECTION PROCEDURE

(1) Submitting packages for memory device at each of the following stages

Semiconductor manufacturers shall submit packages at each of the following stages to the plastic package subcommittee. The committee shall create a package list of the packages and distribute these lists.

(a) Level 1: Submission of packages (for each type of memory device) in the development stage for selection and approval.
These are packages that a semiconductor manufacturer is planning to use for new memory device. They will be shown to all the other manufacturers and if there are any differences between the packages they will be adjusted during the developing stage. The dimensions of new packages are to be standardized.
[Marked (*) in the memory package list.]

(b) Level 2: Submission of packages (for each type of memory device) whose development has been determined.
Semiconductor manufacturer shall submit samples of packages for new memory devices whose development has already been approved and whose precise dimensions have been set when the production of packaging tools are about to start. Thus the samples submitted are the ones that will eventually be put on the market.
[Indicated by (○) in the memory package list.]

(c) Level 3: Submitting packages for memory devices at the mass production stage
These are samples of marketable packages (e.g. commercial samples) for new memory devices submitted by semiconductor manufacturers.
[Indicated by (●) in the memory package list.]

(2) Selecting standard packages for each memory device

(a) The three semiconductor manufacturers that are members of the Plastic Package Subcommittee shall designate standard packages from among level 2 and 3 packages given in the package list. [Indicated by (/////) in the memory package list.]

(b) Once, the package is designated as standard package, it will be continuously designated as standard package, while it is Level 3 in more than one member of the Plastic Package Subcommittee.

(c) The standard package should be eliminated, when no member of the Plastic Package Subcommittee support its production. When the eliminated package will be designated standard package again, it should be follow the procedure (2)-(a).

(d) Only one type of package should be designated as the standard package. If absolutely necessary, two types of packages can be designated as standard packages. When more than three candidate packages are exist, two types of packages shall be designated standard package based on count of level 3 companies

(3) Announcing memory package list

(a) The memory package list to be used in committee deliberations is to be submitted to the Plastic Package Subcommittee.

(b) The memory package list shall be published once a year or whenever necessary to announce revisions of the standard when standard packages for each type of memory device have been designated.

5. STANDARD PACKAGES OF UNIVERSAL MEMORY DEVICES

Table 1 to 7 lists the standard packages for each memory device. Table 8 list the packages that has been eliminated from standard packages in this revision.

Remarks:

Each table indicate as follows.

(1) In column DIP, "P-18-300-2.54" means "P-DIP18-0300-2.54".

(2) In column QFP, "P-L100-1420-0.65" means "P-LQFP100-1420-0.65".

(3) In column SOP, "P-S64-525-0.80" means "P-SSOP64-0525-0.80".

(4) Lead depopulation is indicated "Maximum lead count / Existing lead count".

References:

(1) **EIAJ ED-7403-1** General Rules for the preparation of Outline Drawings of Integrated Circuits Plastic Dual In-line Packages

(2) **EIAJ ED-4705** General Rules for the preparation of Outline Drawings of Integrated Circuits Zig-zag In-line Packages

(3) **EIAJ ED-7405-1** General Rules for the preparation of Outline Drawings of Integrated Circuits Shrink Zigzag In-line Packages

(4) **EIAJ ED-7406A** General Rules for the preparation of Outline Drawings of Integrated Circuits Small Outline J-lead Packages

(5) **EIAJ EDR-7311** Design guidline of integrated circuits for Quad Flat Packages

(6) **EIAJ ED7402-1** General Rules for the preparation of Outline Drawings of Integrated Circuits Small Outline Packages

(7) **EIAJ EDR-7314** Design guidline of integrated circuits for Shrink Small Outline Packages

(8) **EIAJ ED-7424** General Rules for the preparation of Outline Drawings of Integrated Circuits Surface Vertical Packages

(9) **EIAJ EDR-7312** Design guidline of integrated circuits for Thin Small Outline Packages (Type1)

(10) **EIAJ EDR-7313** Design guidline of integrated circuits for Thin Small Outline Packages (Type2)

(11) **EIAJ ED-7407** General Rules for the preparation of Outline Drawings of Integrated Circuits Quad Flat J-lead Packages

(12) **EIAJ ED-7421** General Rules for the preparation of Outline Drawings of Integrated Circuits Ceramic Dual In-line Packages

(13) **EIAJ ED-7422** General Rules for the preparation of Outline Drawings of Integrated Circuits Glass Sealed Quad Flat Packages

Table 1 Standard packages for DRAM

Device		DIP	SOJ	ZIP	TSOP1	TSOP2
1M DRAM	×1	P-18-300-2.54	P-26/20-300-1.27	P-20/19-400-1.27	P-24/20-0616-0.50	P-26/20-300-1.27
	×4	P-20-300-2.54	P-26/20-300-1.27	P-20/19-400-1.27	P-24/20-0616-0.50	P-26/20-300-1.27
	×8					
	×16		P-40-400-1.27	P-40-475-1.27		P-44/40-400-0.80
4M DRAM	×1	P-18-300-2.54	P-26/20-300-1.27	P-20-400-1.27	P-32-0820-0.50	P-26/20-300-1.27
			P-26/20-350-1.27			
	×4	P-20-300-2.54	P-26/20-300-1.27	P-20-400-1.27	P-32-0820-0.50	P-26/20-300-1.27
			P-26/20-350-1.27			
	×8		P-28-400-1.27	P-28-400-1.27		P-28-400-1.27
	×9		P-28-400-1.27	P-28-400-1.27		P-28-400-1.27
	×16		P-40-400-1.27	P-40-475-1.27		P-44/40-400-0.80
	×18		P-40-400-1.27	P-40-475-1.27		P-44/40-400-0.80
16M DRAM	×1		P-28/24-400-1.27	P-24-475-1.27		P-28/24-400-1.27
			P-26/24-300-1.27			P-26/24-300-1.27
	×4		P-28/24-400-1.27	P-24-475-1.27		P-28/24-400-1.27
			P-26/24-300-1.27			P-26/24-300-1.27
	×8		P-28-400-1.27			P-28-400-1.27
			P-28-300-1.27			P-28-300-1.27
	×9		P-32-400-1.27			
	×16		P-42-400-1.27			P-50/44-400-0.80
	×18		P-42-400-1.27			P-50/44-400-0.80
64M DRAM	×1					P-34-500-1.27
	×4		P-34-500-1.27			P-34-500-1.27
			P-32-400-1.27			P-32-400-1.27
	×8		P-34-500-1.27			P-34-500-1.27
			P-32-400-1.27			P-32-400-1.27
	×16					P-50-400-0.80

Table 2 Standard packages for SDRAM

Device		SOJ	ZIP	TSOP1	TSOP2	QFP
4M SDRAM	×16				P-50-400-0.80	
16M SDRAM	×4				P-44-400-0.80	
	×8				P-44-400-0.80	
	×16				P-50-400-0.80	
64M SDRAM	×4				P-54-400-0.80	
	×8				P-54-400-0.80	
	×16				P-54-400-0.80	
	×32				P-86-400-0.50	
8M SGRAM	×32					P-100-1420-0.65

Table 3 Standard packages for VRAM

Device		DIP	SOJ	ZIP	SOP	TSOP2
1M Dual	×4	P-28-400-2.54	P-28-400-1.27	P-28-400-1.27		P-28-400-1.27
	×8		P-40-400-1.27	P-40-475-1.27		P-44/40-400-0.80
2M Dual	×8		P-40-400-1.27			P-44/40-400-0.80
	×16				P-S64-525-0.80	
4M Dual	×16				P-S64-525-0.80	

Table 4 Standard packages for SRAM

Device		DIP	SOP	TSOP1	TSOP2	BGA
256K SRAM	×8	P-28-600-2.54 P-28-300-2.54	P-28-450-1.27	P-28-0813.4-0.55 P-32-0814-0.50		
512K SRAM	×8			P-32-0820-0.50		
1M SRAM	×8	P-32-600-2.54	P-32-525-1.27	P-32-0820-0.50 P-32-0813.4-0.50		
	×16				P-44-400-0.80	
2M SRAM	×8			P-32-0813.4-0.50		
4M SRAM	×8	P-32-600-2.54	P-32-525-1.27		P-32-400-1.27	
1M PSRAM	×8	P-32-600-2.54	P-32-525-1.27	P-32-0820-0.50		
4M PSRAM	×8	P-32-600-2.54	P-32-525-1.27		P-32-400-1.27	

Table 5 Standard packages for HSSRAM

Device		DIP	SOJ	SOP	TSOP2	QFP
64K HSSRAM	×1	P-22-300-2.54	P-24-300-1.27			
	×4	P-22-300-2.54 P-24-300-2.54	P-24-300-1.27			
	×8	P-28-300-2.54	P-28-300-1.27	P-28-450-1.27		
72K HSSRAM	×9	P-28-300-2.54	P-28-300-1.27	P-28-450-1.27		
256K HSSRAM	×1	P-24-300-2.54				
	×4	P-24-300-2.54	P-24-300-1.27			
	×8	P-28-300-2.54	P-28-300-1.27			
288K HSSRAM	x9	P-32-300-2.54	P-32-300-1.27	P-32-450-1.27		
1M HSSRAM	×1		P-28-400-1.27			
	×4	P-28-400-2.54 P-32-400-2.54	P-28-400-1.27 P-32-400-1.27			
	×8	P-32-400-2.54	P-32-400-1.27			
	×9		P-36-400-1.27			
	×16		P-44-400-1.27		P-44-400-0.80	
	×18		P-44-400-1.27		P-44-400-0.80	
	×32					P-L100-1420-0.65
4M HSSRAM	×1		P-32-400-1.27		P-32-400-1.27	
	×4		P-32-400-1.27			
	×8		P-36-400-1.27			
	×16		P-44-400-1.27			

Table 6 Standard packages for PROM

Device		DIP	SOP	TSOP1	TSOP2	QFJ
1M FLASH	×8	P-32-600-2.54	P-32-525-1.27	P-32-0820-0.50		P-32-R450-1.27
				P-32-0814-0.50		
1M EPROM	×8	X-32-600-2.54	P-32-525-1.27			P-32-R450-1.27
	×16	X-40-600-2.54	P-40-525-1.27			P-44-S650-1.27
2M FLASH	×8			P-32-0820-0.50		P-32-R450-1.27
				P-40-1020-0.50		
2M EPROM	×8	X-32-600-2.54	P-32-525-1.27			P-32-R450-1.27
	×16	X-40-600-2.54				
4M FLASH	×8			P-40-1020-0.50		
	×16		P-44-600-1.27	P-48-1220-0.50		
4M EPROM	×8	X-32-600-2.54	P-32-525-1.27			
	×16	X-40-600-2.54	P-40-525-1.27			P-44-S650-1.27
			P-44-600-1.27			
8M FLASH	×8		P-44-600-1.27	P-40-1020-0.50		
	×16		P-44-600-1.27	P-48-1220-0.50		
8M EPROM	×8	X-32-600-2.54	P-32-525-1.27			
	×16	X-42-600-2.54				
16M FLASH	×8			P-48-1220-0.50		
16M EPROM	×16	X-42-600-2.54	P-44-600-1.27			

Note : Material Code " X" means Plastic package "P" or Ceramic Package "C".

Table 7 Standard packages for MROM

デバイス		DIP	SOP	TSOP1	TSOP2	QFP
1M MROM	×8	P-28-600-2.54	P-28-450-1.27			
		P-32-600-2.54	P-32-525-1.27			
	×16	P-40-600-2.54				
2M MROM	×8	P-32-600-2.54	P-32-525-1.27			
	×16	P-40-600-2.54				
4M MROM	×8	P-32-600-2.54	P-32-525-1.27		P-32-400-1.27	
	×16	P-40-600-2.54	P-40-525-1.27	P-48-1218-0.50	P-44-400-0.80	P-44-1414-0.80
8M MROM	×8	P-32-600-2.54	P-32-525-1.27		P-32-400-1.27	
	×16	P-42-600-2.54	P-44-600-1.27	P-48-1218-0.50	P-44-400-0.80	P-44-1414-0.80
					P-48-550-0.80	P-64-1420-1.00
16M MROM	×8	P-36-600-2.54				
	×16	P-42-600-2.54	P-44-600-1.27	P-48-1218-0.50	P-44-400-0.80	P-64-1420-1.00
					P-48-550-0.80	
	×32		P-S70-500-0.80			
32M MROM	×16	P-42-600-2.54	P-44-600-1.27			
	×32		P-S70-500-0.80		P-70-400-0.65	

Table 8 Standard packages that was eliminated by revision up.

デバイス		DIP	SOP	ZIP	TSOP2	QFP
1M DRAM	×1					
	×4					
16M DRAM	×9				P-32-400-1.27	
4M DRAM	×1	P-18-400-2.54				
	×4	P-20-400-2.54				
1M Dual VRAM	×8			P-S40-475-0.889		
2M Dual VRAM	×8			P-S40-475-0.889		
4M MROM	×16				P-48-550-0.80	P-64-1420-1.00
8M MROM	×16		P-S48-600-0.80			
16M MROM	×16		P-S48-600-0.80			

Comments

These comments are provided to help the understanding of the provisions and related matters, and do not form any part of this standard.

1. OBJECTIVE OF ESTABLISHMENT

This standard was established to ensure the compatibility of the package used for the high-generality semiconductor memory devices such as DRAM, SDRAM, VRAM, SRAM, HSSRAM, PROM, and MROM.

2. PROCESS OF DELIBERATION

It was found that the applicable package and package size for the homogeneous memory devices varied depending on the semiconductor makers. To help unifying them, **EIAJ ED-7441** was established in December, 1991, and revised in March, 1993 as **EIAJ-ED7441A**. However, it has not been revised since then, while the new standard package was determined.

Thus, since the revision was desired, it was suggested to review this standard at the 10th Plastic Package Subcommittee held in June, 1996, and the standard was actually revised under the approval of Technical Standardization Committee on Semiconductor Device Package in July of the same year. As the subordinate of Plastic Package Subcommittee, the Universal Memory Package Standardization Project was formed and proceeded the specific revision works.

The revised standard was smoothly discussed, passed the final deliberation at the 4th Universal Memory Package Standardization Project in April, 1997 and at the 23rd Plastic Package Subcommittee in January, 1998, approved by Technical Standardization Committee on Semiconductor Device Pacakge, and finally established and issued.

3. REVIEW POINTS

(1) Addition and Deletion of New Standard Package

Plastic Package Subcommittee has surveyed the development trend of universal memory devices of each maker, and added or deleted the standard packages mentioned at the 23rd Plastic Package Subcommittee in January, 1998.

(2) Selection of Standard Package

Since new packages are often applied due to the shrinkage of semiconductor devices, the deliberation focused on handling the standard package defined before the shrinkage, and the selection of standard package was partially reviewed.

4. COMMITTEE MEMBERS

The standard was mainly reviewed by Plastic Package Subcommittee and the Universal Memory Package Standardization Project of Technical Standardization Committee on Semiconductor Device Pacakge which members are as follows.

EIAJ ED－7441B Comments

<Semiconductor Package Standardization Committee>

Chairman	Toshiaki Shinohara	Mitsubishi Electric Corporation

<Plastic Package Subcommittee>

Chairman	Masanori Yoshimoto	Fujitsu Limited
Sub-Chairman	Yasuhito Suzuki	Mitsubishi Electric Corporation
Members	Tsutomu Kashiwagi	Enpulas Corporation
	Kazuhiko Sera	Oki Electric Industry Co.,LTD.
	Chun-Gu No	Samsung Electronics Japan Co.,LTD.
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	Masahiko Kobayashi	Sumitomo 3M,LTD.
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	Toshihiko Nojiri	Sony Corporation
	Takashi Okada	Toshiba Corporation
	Kenji kanesaka	Nippon Steel SemiconductorCorporation
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	Takahiro Imura	Texas Instruments Japan LTD.
	Kouichi Takekawa	NEC Corporation
	Nobuo Sato	Nippon Motorola LTD.
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	Nanahiro Hayakawa	Yamaichi Electronics Co.,LTD.
	Hitoshi Matunaga	Unitechno Inc.
	Hiromori Okamura	Rohm Co.,LTD.

<Universal Memory Package Standardization Project>

Leader	Hideo Taguchi	Toshiba Corporation
	Nobuhito Ohuchi	Oki Electric IndustryCo.,LTD.
	Hideyuki Iwamura	Sanyo Electric Co.,LTD.
	Katsuyuki Tarui	Sharp Corporation
	Takahiro Imura	Texas Instruments Japan LTD.

Kenichi Kurihara	NEC Corporation
Hiroshi Yano	Hitachi LTD.
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