



Standard of Japan Electronics and Information Technology Industries Association

JEITA ED - 7715

**Standard for open-top type socket
[54/66 Pin Thin Small Outline Package (Type 2)]**

Established in March, 2006

Prepared by
Technical Standardization Committee on Semiconductor Device Package

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Standard of open-top type socket [54/66 pin Thin Small Outline Packages (Type 2)]

Foreword

This standard is prepared by the Subcommittee on Semiconductor Socket, Technical Standardization Committee on Semiconductor Device Package. This is an individual standard which complies with the format of the “Rules for the drafting and presentation of JEITA Standards”, **TSC-16**, as well as the normative references that were established with the intention of harmonizing with international standards.

1. Scope

This standard specifies the outlines and dimensions of the open-top type sockets among the test and burn-in sockets for TSOPs (type 2) that are specified in the **EIAJ EDR-7313**, more specifically for the 54 pin TSOP (type 2) with the terminal pitch ϕ of 0.8 mm and the 66 pin TSOP (type 2) with ϕ of 0.65 mm.

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or supplements) applies.

JEITA standards:

- EIAJ EDR-7313** Design guideline of integrated circuits for Thin Small Outline Package (Type II) (TSOP (II))
- EIAJ ED-7300A** Recommended practice on standard for the preparation of outline drawings of semiconductor packages
- EIAJ ED-7303B** Name and code for integrated circuits package
- EIAJ ED-7701** Glossary of semiconductor socket for BGA, LGA, FBGA, and FLGA

3. Terms and definitions

Most of the terminology used in this document complies with **EIAJ ED-7300A**, **ED-7303B**, and **ED-7701**, while the new terminology is defined in the text.

4. Background

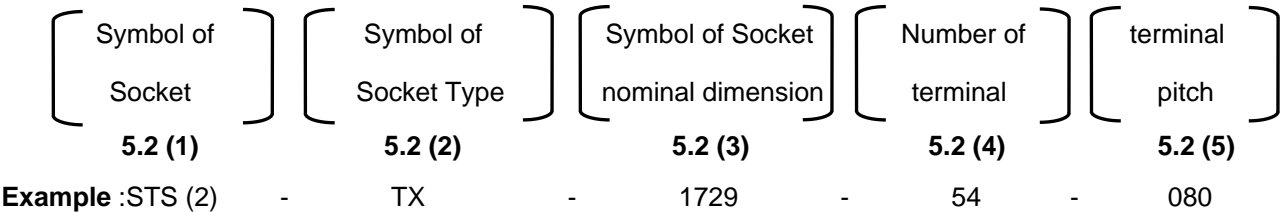
Requirements for the higher functionality and performances of the electronic products have resulted in the sharp rise of the demand for the surface mount devices. Among them, the demand for thin small outline packages with the mounting height of 1.2 mm or lower (TSOP (2)) is significant, because these are used in the thinner electronics products such as memory card.

This standard aims at standardizing the outline dimensions of sockets for 54 and 66 pin TSOP (2), which are the majority in production, and ensuring compatibility between sockets from various suppliers.

5. Socket code

5.1 Designation system of the socket code

The designation system of the socket code is as follows:



5.2 Symbol

(1) Socket designator

The socket designator is expressed by six characters. “STS(2)” is designated for the socket of TSOP(2), where the first character of “S” denotes socket and the following five characters are the part of the package code.

NOTE : Thin Small Outline Package (Type 2) is a derived package name, and the package code is expressed by seven characters, “TSOP(2)”. Since the package code TSOP(II) is no longer used, socket code shall not be “STS(II)”.

(2) Socket type designator

The socket type designator is expressed by two alphabetic characters; the first character is “T” denoting open-top type, and the second character shown as “X” is optional.

(3) Socket nominal dimension

The socket nominal dimension is expressed by four numeric characters. The first two characters indicate the socket width (W) and the last two indicate the socket length (L). The numbers are rounded off to the whole numbers.

(4) Terminal count

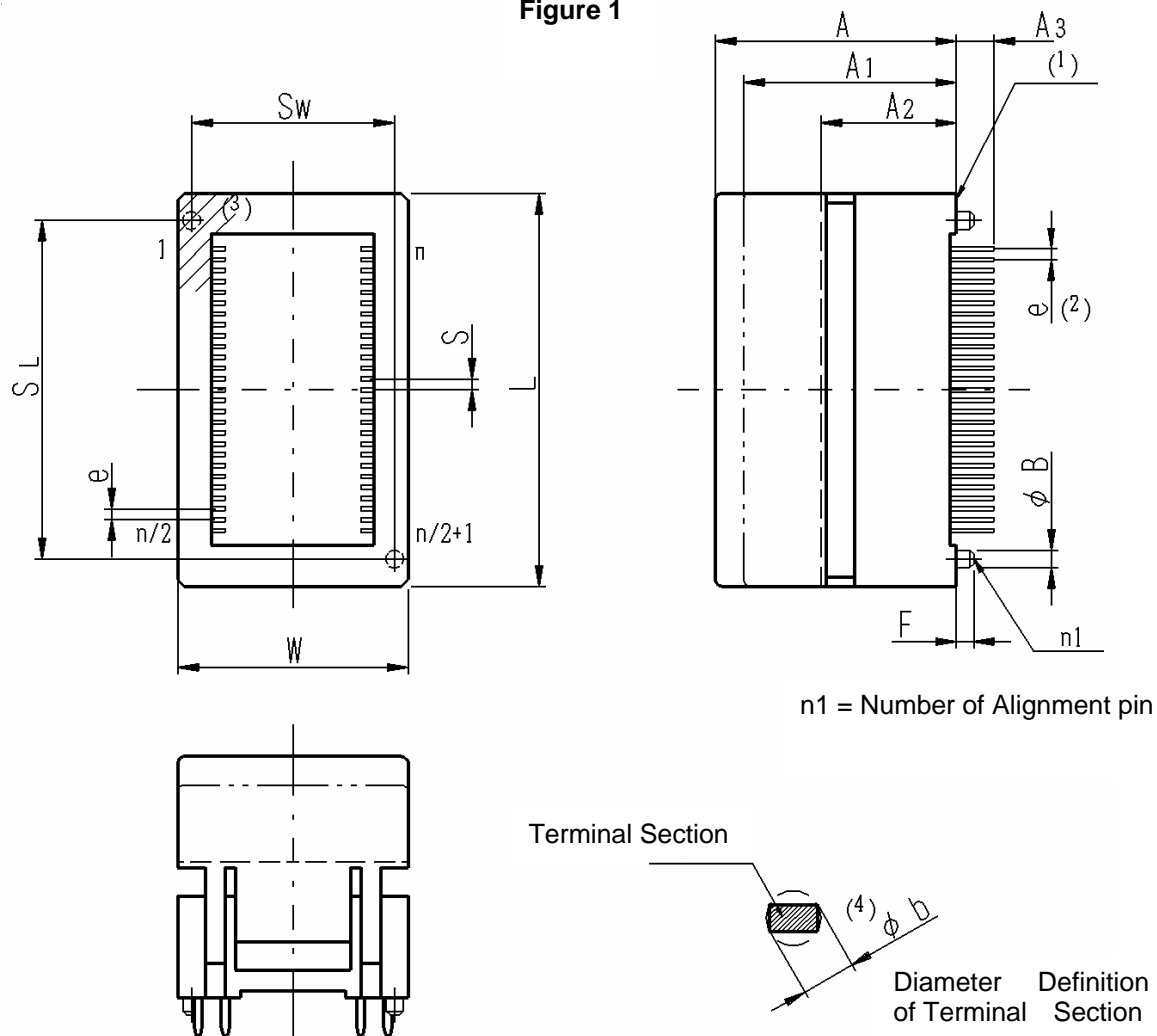
Terminal count is expressed by two numeric characters which are the number of terminals, n, of the corresponding package.

(5) Terminal pitch

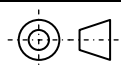
Terminal pitch is expressed by three numeric characters, where decimal point is omitted.

6. Reference symbols and schematics

Figure 1



- Notes:** (1) Indicates mounting plane. Mounting plane is defined by the plane where the socket contacts its mounting surface.
- (2) Stipulates true geometric position of the terminals.
- (3) Indicates positional tolerance of the index mark. Index mark should be completely within the shaded area where less than 1/16 with socket body size. It must be included in the shaded area entirely.
- (4) Terminal diameter is defined as the maximum diameter of a circle circumscribed about a vertical projection of the terminal from the mounting plane.



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Figure 2

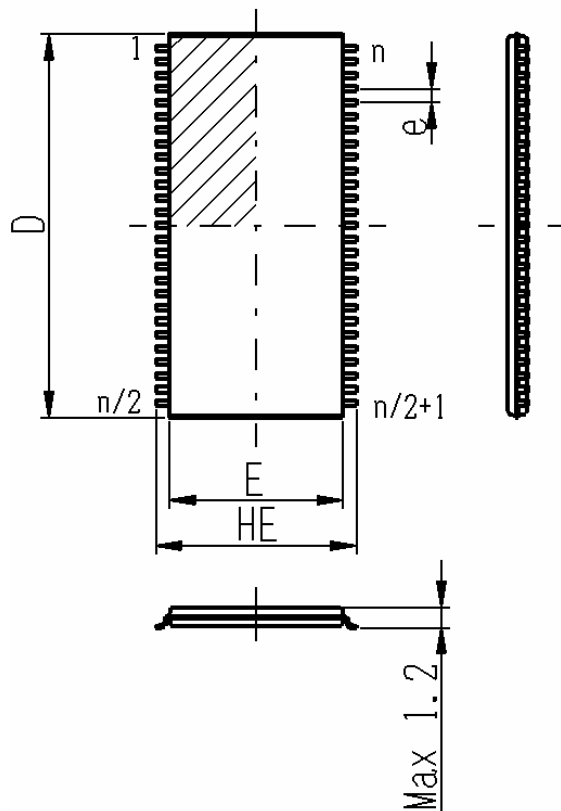
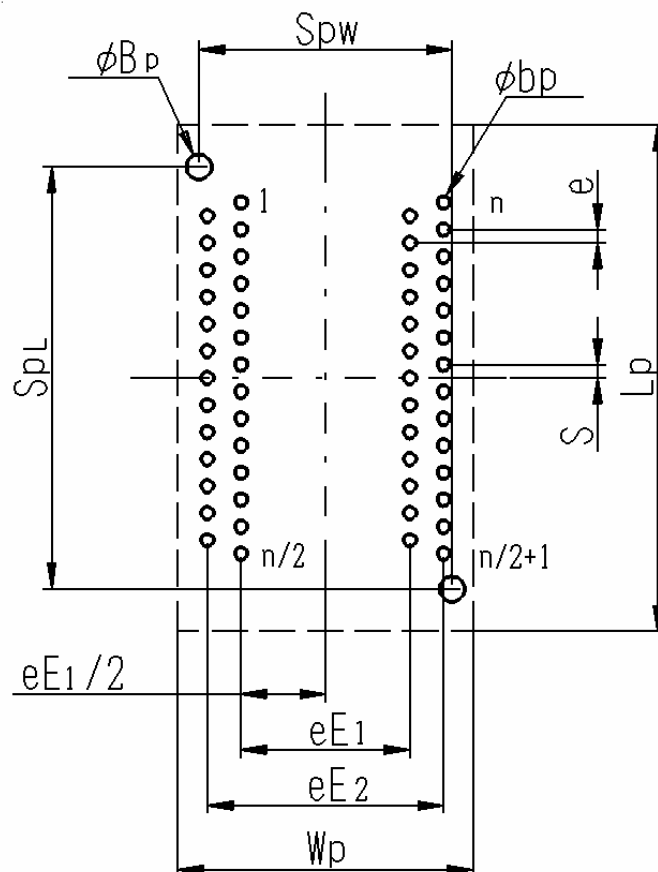


Figure 3



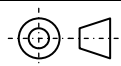
Notes.

1. Outline Drawings

Outline drawings of the socket are shown in **Figure1** and that for applicable package is in **Figure2**.

2. Reference Symbols and Schematics of Recommended Socket Mounting Pattern on Printed Circuit Board

The drawing of the recommended socket mounting pattern on printed circuit board is shown in **Figure 3** for reference in printed circuit board designing.



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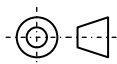
7. REGISTRATION TABLE

Socket Name : STS(2)

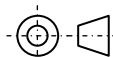
Object package : TSOP(2)

Registration No. XX-771X-001

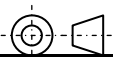
| Nominal Dimension | Terminal pitch e | |
|-------------------|--|------------------------|
| | 0.80 | 0.65 |
| 400mil | 54-001-AA 54-002-AB | 66-001-AC 66-002-AD |

Note: Numbers in the Table Indicate “(Terminal number n)-(Consecutive number)-(Serial number)”JEITA STANDARD
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| Reference Number | | AA | | | AB | | |
|------------------|----------------|----------------------|-------|-------|----------------------|-------|-------|
| Socket Code | | STS(2)-T-1729-54-080 | | | STS(2)-T-2028-54-080 | | |
| Reference Symbol | | min | nom | max | min | nom | max |
| Group 1 | L | | 28.78 | | | 28.00 | |
| | W | | 17.02 | | | 20.20 | |
| | A | | 17.80 | | | 14.80 | |
| | A ₁ | | 15.70 | | | 11.80 | |
| | A ₂ | | 10.00 | | | 8.60 | |
| | e | | 0.80 | | | 0.80 | |
| | n | | 54 | | | 54 | |
| | A ₃ | | 2.80 | | | 3.30 | |
| | Øb | | | 0.65 | | | 0.65 |
| | n ₁ | 0 | | 2 | 0 | | 2 |
| | F | | 1.30 | | | 1.30 | |
| | S _L | | 25.00 | | | 25.00 | |
| | S _w | | 15.00 | | | 12.40 | |
| | ØB | | 1.30 | | | 1.30 | |
| | S | | 0.80 | | | 0.80 | |
| Group 2 | Lp | | | 29.58 | | | 28.80 |
| | Wp | | | 17.82 | | | 21.00 |
| | Spl | | 25.00 | | | 25.00 | |
| | Spw | | 15.00 | | | 12.40 | |
| | eE1 | | 10.00 | | | 10.67 | |
| | eE2 | | 14.00 | | | 15.75 | |
| | ØBp | 1.40 | | 1.50 | 1.40 | | 1.50 |
| | Øbp | | | 0.80 | | | 0.80 |
| Group 3 | D | | 22.22 | | | 22.22 | |
| | E | | 10.16 | | | 10.16 | |
| | HE | | 11.76 | | | 11.76 | |

| | | | | | | |
|---|---|--|---------------------------------------|------------------|--|----------------|
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| Reference Number | | AC | | | AD | | |
|------------------|----------------|----------------------|-------|-------|----------------------|-------|-------|
| Socket Code | | STS(2)-T-1729-66-065 | | | STS(2)-T-2028-66-065 | | |
| Reference Symbol | | min | nom | max | min | nom | max |
| Group 1 | L | | 28.78 | | | 28.00 | |
| | W | | 17.02 | | | 20.20 | |
| | A | | 17.80 | | | 14.80 | |
| | A ₁ | | 15.70 | | | 11.80 | |
| | A ₂ | | 10.00 | | | 8.60 | |
| | e | | 0.65 | | | 0.65 | |
| | n | | 66 | | | 66 | |
| | A ₃ | | 2.80 | | | 3.30 | |
| | Øb | | | 0.65 | | | 0.65 |
| | n ₁ | 0 | | 2 | 0 | | 2 |
| | F | | 1.30 | | | 1.30 | |
| | S _L | | 25.00 | | | 25.00 | |
| | S _w | | 15.00 | | | 12.40 | |
| | ØB | | 1.30 | | | 1.30 | |
| | S | | 0.65 | | | 0.65 | |
| Group 2 | Lp | | | 29.58 | | | 28.80 |
| | Wp | | | 17.82 | | | 21.00 |
| | Spl | | 25.00 | | | 25.00 | |
| | Spw | | 15.00 | | | 12.40 | |
| | eE1 | | 10.00 | | | 10.67 | |
| | eE2 | | 14.00 | | | 15.75 | |
| | ØBp | 1.40 | | 1.50 | 1.40 | | 1.50 |
| | Øbp | | | 0.80 | | | 0.80 |
| Group 3 | D | | 22.22 | | | 22.22 | |
| | E | | 10.16 | | | 10.16 | |
| | HE | | 11.76 | | | 11.76 | |

| | | | |
|---|---|---------------------------------------|----------------|
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8. Members of the Committee

This Standard was deliberated by Semiconductor Socket Project Sub-Committee of Technical Standardization Committee on Semiconductor Device Package.

The members are as shown below.

<Technical Standardization Committee on Semiconductor Device Package>

| | | |
|-----------|------------------|--------------|
| Chairman: | Katsuroh Hiraiwa | Fujitsu Ltd. |
|-----------|------------------|--------------|

<Semiconductor Socket Project Group>

| | | |
|----------------------|---------------------|---|
| Chief Examiner: | Nobuhiro Katsuma | Matsushita Electric Industrial Co., Ltd |
| Vice-Chief Examiner: | Kazumasa Sato | Wells-CTI K.K. |
| | Yuji Wada | Renesas Technology Corporation |
| Member: | Satoshi Matsumoto | NEC Electronics Corporation |
| | Yoshiyuki Ohashi | Enplas Corporation |
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