JEITA

Standard of Japan Electronics and Information Technology Industries Association

JEITA ED - 7716

Standard for open-top type socket
[Fine-pitch Ball Grid Array (FBGA) for Memory IC]

Established in March, 2006

Prepared by

Technical Standardization Committee on Semiconductor Device Package

Published by

Japan Electronics and Information Technology Industries Association

11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan

Printed in Japan

Translation without guarantee in the event of any doubt arising, the original standard in Japanese is to be evidence.

JEITA standards are established independently to any existing patents on the products, materials or processes they cover.
JEITA assumes absolutely no responsibility toward parties applying these standards or toward patent owners.

© 2006 by the Japan Electronics and Information Technology Industries Association

All rights reserved. No part of this standards may be reproduced in any form or by any means without prior permission in writing from the publisher.

Registration Table

Socket Name：SFB (0.80mm pitch)

Object Package：FBGA (0.8mm pitch)

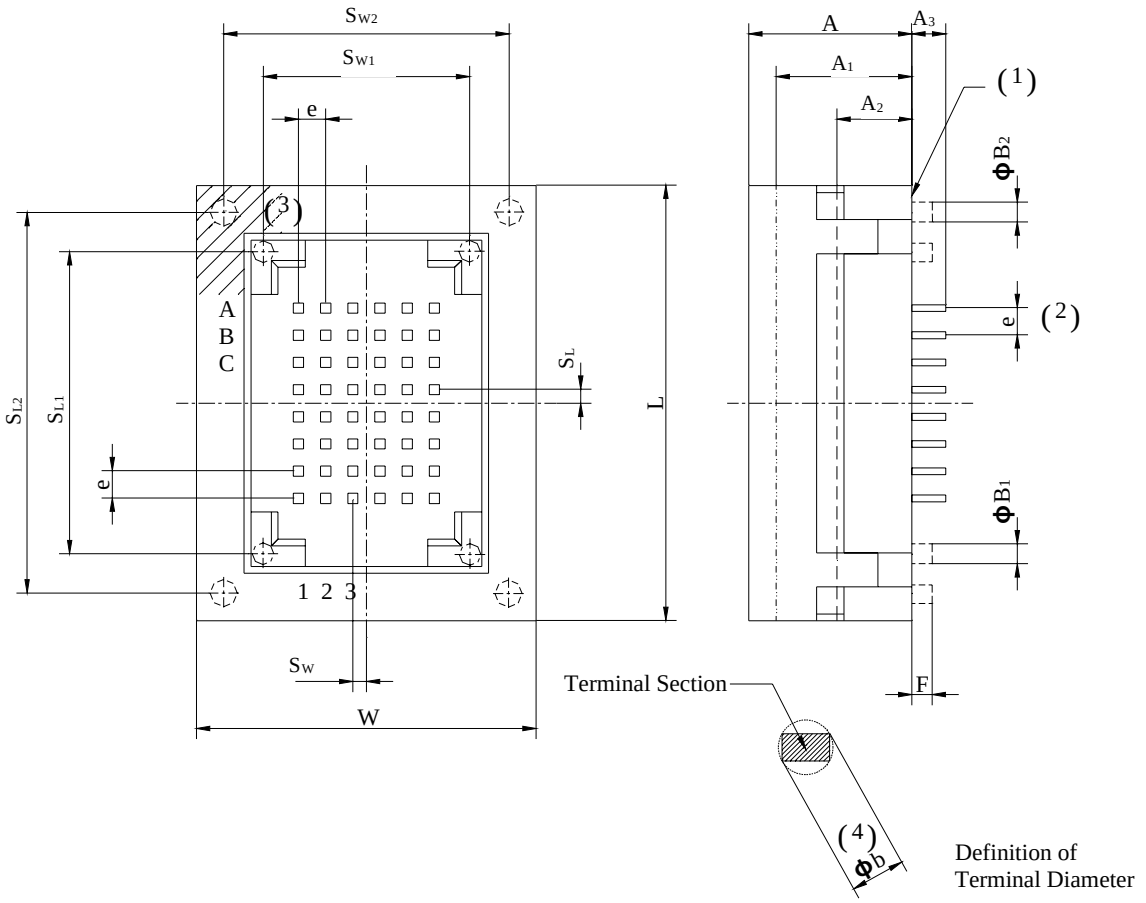
Registration No.：XXX-XXXX-001

E x D	Terminal pitch e	
	0.80	
	Package	Socket
6.00 × 8.00	48-001-AC 48-001-AD 48-001-AE	48-001-AC 48-001-AD 48-001-AE
6.00 × 10.00	32-001-BA	32-001-BA
10.00 × 8.00	56-001-CA	56-001-CA
8.00 × 8.00	64-001-DA	64-001-DA
9.00 × 9.00	65-001-EA	65-001-EA
8.00 × 10.00	68-001-FA	68-001-FA
11.00 × 8.00	72-001-GA	72-001-GA(1) 72-001-GA(2)
8.00 × 11.00	73-001-HA	73-001-HA(1) 73-001-HA(2)
9.00 × 11.00	73-001-HB	73-001-HB
9.00 × 12.00	73-001-HC	73-001-HC(1) 73-001-HC(2)
9.00 × 14.00	77-001-IA	77-001-IA

Note: Numbers in the Table Indicate “(Terminal number n)-(Consecutive number)-(Serial number)”

Reference symbol and schematics

Figure A



Notes: (1) Indicates mounting plane. Mounting plane is defined by the plane where the socket contacts its mounting surface.

(2) Stipulates true geometric position of the terminals.

(3) Indicates positional tolerance of the index mark. Index mark should be completely within the shaded area where less than 1/16 with socket body size. It must be included in the shaded area entirely.

(4) Terminal diameter is defined as the maximum diameter of a circle circumscribed about a vertical projection of the terminal from the mounting plane.

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 2/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Figure B

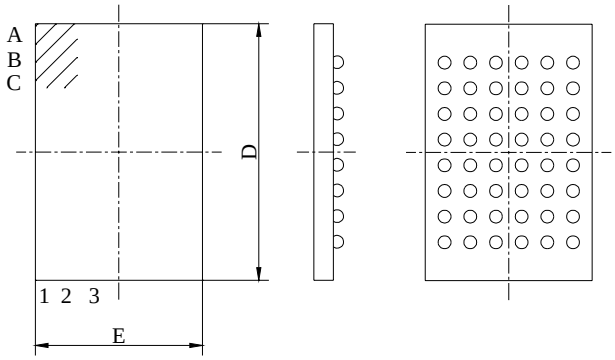
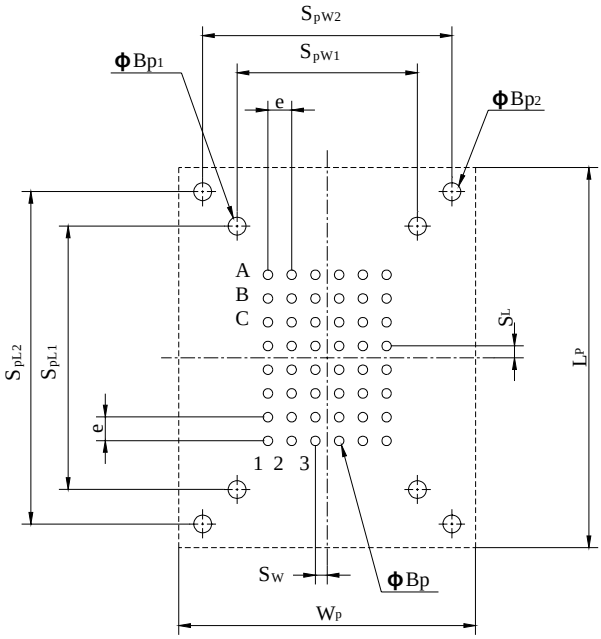


Figure C



Notes.

1. **Outline Drawings**
   Outline drawings of the socket are shown in **Figure A** and that for applicable package is in **Figure B.**
2. **Reference Symbols and Schematics of Recommended Socket Mounting Pattern on Printed Circuit Board**
   The drawing of the recommended socket mounting pattern on printed circuit board is shown in **Figure C** for reference in printed circuit board designing.

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 3/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Serial Number	AC / AD / AE			BA		
Socket Code	SFB-T-XXXXBB-0608-080			SFB-T- XXXXBB-0608-080		
Reference Symbol	min	nom	max	min	nom	max
L		22.0			22.0	
W		18.0			18.0	
A		15.9	16.4		15.9	16.4
A_1		12.4	12.9		12.4	12.9
A_2		8.2	8.7		8.2	8.7
E		0.8			0.8	
A_3		2.0	2.5		2.0	2.5
Øb		0.23	0.28		0.23	0.28
n_1	-		-	-		-
n_2	0		4	0		4
F	2.85	3.35		2.85	3.35	
S_{L1}		-			-	
S_{W1}		-			-	
S_{L2}		19.0			19.0	
S_{W2}		15.0			15.0	
$ØB_1$			-			-
$ØB_2$			1.5			1.5
S_L		0.4			0.4	
S_W		0.4			0.4	
n		48			32	
M_L		8			8	
M_W		6			6	
Ball layout	Fig. 1			Fig. 2		

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 4/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Serial Number	CA			DA		
Socket Code	SFB-T- XXXXBB-1006-080			SFB-T- XXXXBB-0808-080		
Reference Symbol	min	nom	max	min	nom	max
L		18.0			22.0	
W		22.0			18.0	
A		15.9	16.4		15.9	16.4
A_1		12.4	12.9		12.4	12.9
A_2		8.2	8.7		8.2	8.7
e		0.8			0.8	
A_3		2.0	2.5		2.0	2.5
Øb		0.23	0.28		0.23	0.28
n_1	-		-	-		-
n_2	0		4	0		4
F	2.85	3.35		2.85	3.35	
S_{L1}		-			-	
S_{W1}		-			-	
S_{L2}		15.0			19.0	
S_{W2}		19.0			15.0	
ØB_1			-			-
ØB_2			1.5			1.5
S_L		0.4			0.4	
S_W		0.4			0.4	
n		56			64	
M_L		6			8	
M_W		10			8	
Ball layout	Fig. 3			Fig. 4		

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 5/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Serial Number	EA			FA		
Socket Code	SFB-T- XXXXBB-0909-080			SFB-T- XXXXBB-0810-080		
Reference Symbol	min	nom	max	min	nom	max
L		22.0			22.0	
W		18.0			18.0	
A		15.9	16.4		15.9	16.4
A_1		12.4	12.9		12.4	12.9
A_2		8.2	8.7		8.2	8.7
e		0.8			0.8	
A_3		2.0	2.5		2.0	2.5
Øb		0.23	0.28		0.23	0.28
n_1	-		-	-		-
n_2	0		4	0		4
F	2.85	3.35		2.85	3.35	
S_{L1}		-			-	
S_{W1}		-			-	
S_{L2}		19.0			19.0	
S_{W2}		15.0			15.0	
ØB_1			-			-
ØB_2			1.5			1.5
S_L		0.4			0.4	
S_W		0.4			0.4	
n		65			68	
M_L		9			10	
M_W		9			8	
Ball layout	Fig. 5			Fig. 6		

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 6/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Serial Number	GA(1)			GA(2)		
Socket Code	SFB-T- XXXXBB-1208-080			SFB-T- XXXXBB-1208-080		
Reference Symbol	min	nom	max	min	nom	max
L		18.0			20.0	
W		22.0			20.0	
A		15.9	16.4		17.0	17.5
A_1		12.4	12.9		14.0	14.5
A_2		8.2	8.7		9.7	10.2
e		0.8			0.75	
A_3		2.0	2.5		2.8	3.2
Øb		0.23	0.28		0.215	0.28
n_1	-		-		0	
n_2	0		4	0		4
F	2.85	3.35		2.70	3.20	
S_{L1}		-			-	
S_{W1}		-			-	
S_{L2}		15.0			9.2	
S_{W2}		19.0			9.2	
$ØB_1$			-			-
$ØB_2$			1.5		1.9	2.0
S_L		0.4			0.4	
S_W		0.4			0.4	
N		72			72	
M_L		8			8	
M_W		12			12	
Ball layout	Fig. 7					

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 7/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Serial Number	HA(1)			HA(2)		
Socket Code	SFB-T- XXXXBB-1012-080			SFB-T- XXXXBB-1012-080		
Reference Symbol	min	nom	max	min	nom	max
L		22.0			25.4	
W		18.0			17.6	
A		15.9	16.4		18.0	18.5
A_1		12.4	12.9		15.0	15.5
A_2		8.2	8.7		9.7	10.2
e		0.8			0.8	
A_3		2.0	2.5		2.0	2.5
Øb		0.23	0.28		0.215	0.28
n_1	-		-	0		2
n_2	0		4	0		4
F	2.85	3.35		2.00	2.50	
S_{L1}		-			16.0	
S_{W1}		-			5.6	
S_{L2}		19.0			22.0	
S_{W2}		15.0			14.0	
$ØB_1$			-			1.5
$ØB_2$			1.5			2.0
S_L		0.4			0.4	
S_W		0.4			0.4	
N		72			72	
M_L		12			12	
M_W		10			10	
Ball layout	Fig. 8					

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 8/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Serial Number	HB			HC(1)		
Socket Code	SFB-T- XXXXBB-1012-080			SFB-T- XXXXBB-1012-080		
Reference Symbol	min	nom	max	max	nom	max
L		22.0			22.0	
W		18.0			18.0	
A		15.9	16.4		15.9	16.4
A_1		12.4	12.9		12.4	12.9
A_2		8.2	8.7		8.2	8.7
e		0.8			0.8	
A_3		2.0	2.5		2.0	2.5
Øb		0.23	0.28		0.23	0.28
n_1	-		-	-		-
n_2	0		4	0		4
F	2.85	3.35		2.85	3.35	
S_{L1}		-			-	
S_{W1}		-			-	
S_{L2}		19.0			19.0	
S_{W2}		15.0			15.0	
ØB_1			-			-
ØB_2			1.5			1.5
S_L		0.4			0.4	
S_W		0.4			0.4	
N		73			73	
M_L		12			12	
M_W		10			10	
Ball layout	Fig. 8			Fig. 8		

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 9/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Serial Number	HC(2)			IA		
Socket Code	SFB-T- XXXXBB-1012-080			SFB-T- XXXXBB-1014-080		
Reference Symbol	min	nom	max	max	nom	max
L		28.0	28.3		28.0	28.3
W		28.0	28.3		28.0	28.3
A		19.0	19.3		19.0	19.3
A_1		16.0	16.3		16.0	16.3
A_2		9.6	10.1		9.6	10.1
E		0.8			0.8	
A_3		1.9	2.4		1.9	2.4
Øb			0.28			0.28
n_1	-		-	-		-
n_2	0		4	0		4
F	2.85	3.35	3.38	2.85	3.35	3.38
S_{L1}		11.08			11.08	
S_{W1}		15.08			15.08	
S_{L2}		24.0	24.05		24.0	24.05
S_{W2}		24.0	24.05		24.0	24.05
ØB_1			-			-
ØB_2			1.5			1.5
S_L		0.4			0.4	
S_W		0.4			0.4	
N		73			77	
M_L		12			14	
M_W		10			10	
Ball layout	Fig. 8			Fig. 9		

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 10/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

TOP VIEW

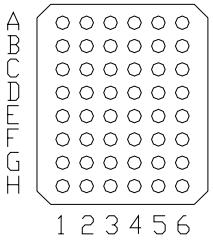


Fig.1

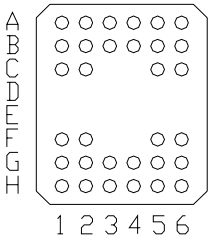


Fig.2

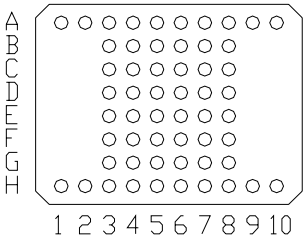


Fig.3

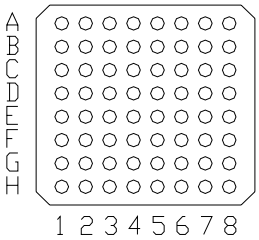


Fig.4

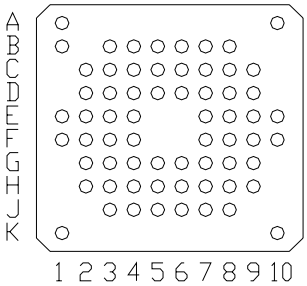


Fig.5

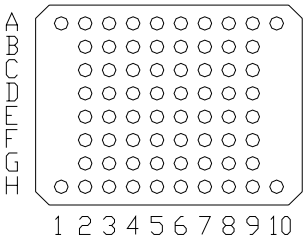


Fig.6

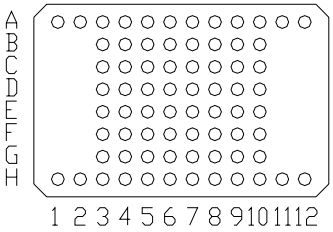


Fig.7

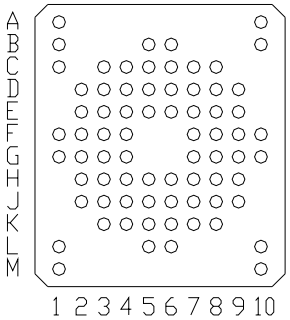


Fig.8

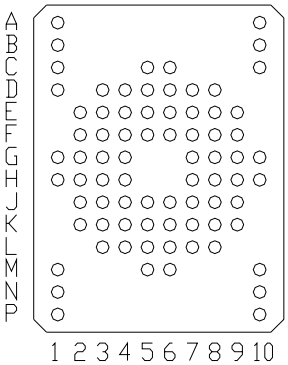


Fig.9

	JEITA STANDARD IC SOCKET OUTLINE DRAWING	DATE 05-XX-XX	SHEET 11/
IC SOCKET NAME SFB		JEITA REGISTRATION NO. XX-XXXX-001	

Members of the Committee

This design guideline was deliberated by Semiconductor Socket Project Sub-Committee of Technical Standardization Committee on Semiconductor Device Package.

The members are as shown below.

<Technical Standardization Committee on Semiconductor Device Package>

Chairman:	Katsuroh Hiraiwa	Fujitsu Ltd.

<Semiconductor Socket Project Group>

Chief Examiner:	Nobuhiro Katsuma	Matsushita Electric Industrial Co., Ltd
Vice-Chief Examiner:	Kazumasa Sato	Wells-CTI K.K.
	Yuji Wada	Renesas Technology Corporation
Member:	Satoshi Matsumoto	NEC Electronics Corporation
	Yoshiyuki Ohashi	Enplas Corporation
	Tohru Hayashi	SANYO Electric Co., Ltd.
	Takayuki Nagumo	Sumitomo 3M Limited
	Hidefumi Shiro	Toshiba Corporation
	Hideki Sano	Texas Instruments Japan Ltd.
	Hiroyuki Hosogi	Texas Instruments Japan Ltd.
	Fumio Konishi	Molex Japan Co., Ltd.
	Kazuhiro Tashiro	Fujitsu Ltd.
	Katsunori Takahashi	Yamaichi Electronics Co., Ltd.
	Tomoaki Adachi	Unitechno Inc.
	Akihiko Tadaoka	Rohm Co., Ltd.