

Technical Report of Electronic Industries Association of Japan

EIAJ EDR-4703

Quality Assurance Guidelines for Bare Die including KGD

Established in April, 1999

Prepared by

Technical Standardization Committee on Semiconductor Devices

Published by Electronic Industries Association of Japan

5-13, Nishi-shinbashi 1-chome, Minato-ku, Tokyo 105-0003, Japan Printed in Japan

CONTENTS

			page
1.	Out	line · · · · · · · · · · · · · · · · · · ·	• 1
2.	Qua	lity Assurance of Packaged Semiconductor Devices · · · · · · · · · · · · · · · · · · ·	• 1
3.	Bare	e Die Quality Level Classification · · · · · · · · · · · · · · · · · · ·	. 3
	3.1	Level1/KGD (Known Good Die)······	• 3
	3.2	Level2/KTD (Known Tested Die) · · · · · · · · · · · · · · · · · · ·	• 5
	3.3	Level3/PD (Probed Die) · · · · · · · · · · · · · · · · · · ·	• 5
4.	Sup	ply with Information about Bare Die · · · · · · · · · · · · · · · · · · ·	. 9
	4.1	Electric Design Information · · · · · · · · · · · · · · · · · · ·	• 9
	4.2	Physical Design Information · · · · · · · · · · · · · · · · · · ·	• 9
	4.3	Quality Information · · · · · · · · · · · · · · · · · · ·	. 9
5.	Ship	oment·····	11
	5.1	Shipment Configuration · · · · · · · · · · · · · · · · · · ·	11
		Traceability	
	5.3	Attached Information at the Time of Shipment · · · · · · · · · · · · · · · · · · ·	11
6.	Stor	age Period Standard · · · · · · · · · · · · · · · · · · ·	11
7.	Def	ective Die Handling · · · · · · · · · · · · · · · · · · ·	11
8.	Refe	erences ······	13
Ех	plan	ation ·····	15
	1.	Background · · · · · · · · · · · · · · · · · · ·	15
	2.	Details of Discussions · · · · · · · · · · · · · · · · · · ·	15
	3.	Members · · · · · · · · · · · · · · · · · · ·	15

Technical Report of Electronic Industries Association of Japan

Quality Assurance Guidelines for Bare Die including KGD

1. Outline

Electronic equipment has recently become significantly smaller, lighter and more functional because mobile products have spread. As a result of the popularizing, bare die mounting, which at customer's line was very rare case, has become widely performed at the assembly lines of consumer electronic equipment manufacturers. The purpose of this guideline is that both semiconductor users and manufacturers have common understanding of the quality assurance of bare die.

Note 1 Bare die: Is a die on the wafer or removed from the wafer by scribing, etc. Such a die as has had any metallization (bump, beam lead, etc.) on a pad is also included. We call it also "bare chip" in Japan. However, a "bare die" is better when this guideline is translated into English.

2. Quality Assurance of Packaged Semiconductor Devices

First we describe the outline of the quality assurance of those which are shipped after packaged. In this guideline we will study the quality assurance of semiconductor devices by using four factors "visual mechanical," "electric characteristics," "early failure" and "long-term reliability" which can demonstrate the quality of devices themselves. Visual mechanical and electric characteristics affect the quality at user's assembly line. Manufacturers screen devices by the following flow.

(1) Wafer probing

In general, DC characteristics are mainly measured.

For example, the following characteristics are measured for MOS devices:

- Open-short check;
- Input and output leakage;
- Input and output voltage/current;
- Power currents (dynamic/standby); and,
- Function check.

(2) Final characteristic inspection

In addition to the items in (1), final characteristic inspection for packaged products consists of analog characteristics, speed, timing, etc. to verify whether it can meet the detailed specifications for screening.

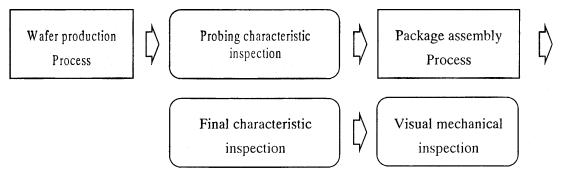


Fig.2.1 Example of semiconductor device inspection flow

EIAJ EDR-4703

Early failure and long-term reliability of semiconductor devices depend on the following, on which the market quality of the equipment mounting those devices will inevitably depend. Semiconductor manufacturers evaluate the above by reliability tests.

- (a) Early failure : Such a failure as occurs resulting from nonconformity of wafer or package assembly process. As time passes, the failure rate is reduced
- **(b) Long-term reliability**: Reliability of devices after the early failure period, explained by reliability characteristics, such as failure rate, duration of life

3. Bare Die Quality Level Classification

When discussing on the bare die quality assurance, it is naturally necessary to define what should be assured. To assure what are same to those for package products is most understandable. However, it is difficult to apply these criteria to all semiconductor devices for technical and financial reasons. Therefore, we classify into "Level1/known-good die (KGD)," "Level2/known tested die (KTD)" and "Level3/probed die (PD)" by the four factors "visual mechanical," "electric characteristics," "early failures" and "long-term reliability" mentioned in Chapter 2 above. The outline of the extent of the quality assurance for each of the levels is described in 3.1.

3.1 Level 1/ KGD

(1) Visual mechanical

Perform a visual mechanical inspection by sampling. Definitions of defects and nonconforming products, inspection items and inspection method, etc. should be specified in the detailed specification.

(2) Electric characteristics

Perform probing on die before scribing to screen good die by the same test items corresponding to the final inspection items for packaged products. The detailed test items and specifications should be specified in the detailed specification. Those electric characteristics after mounting by users are not assured.

(3) Early failures

Early failures caused by those failure modes not resulting from assembly or mounting at user's line but from the bare die wafer process, should be the same level as packaged products should be. Those which have not yet reached the specified quality level, should be subjected to the same screening including burn-in, as packaged products should be subjected to, according to manufacturer's judgment to accomplish the quality level.

(4) Long-term reliability

Long-term reliability concerning to those failure modes not resulting from assembly or mounting at user's line but from the bare die wafer process, should be the same level as packaged products should be.

3.2 Level 2/ KTD

(1) Visual mechanical

Perform the same sampling inspection as is performed on Level 1/KGD.

(2) Electric characteristics

Perform the same test items to those for Level 1/KGD.

(3) Early failures

Are not assured.

(4) Long-term reliability

Is not assured.

3.3 Level 3/PD

(1) Visual mechanical

Perform the same sampling inspection as is performed on Level 1/KGD.

(2) Electric characteristics

Perform probing on die before scribing to screen good die, as a part of the final inspection items for packaged products. The detailed test items and specifications should be specified in the detailed specification. Those electric characteristics after mounting by users are not assured.

(3) Early failures

Are not assured.

(4) Long-term reliability

Is not assured.

3.1 Outline of the extent of the quality assurance for each of the levels

	Processes	Level 1/KGD	Level 2/KTD	Level 3/PD
	Wafer	Wafer-processed articles before characteristic inspection	Same to the left.	Same to the left.
Semiconductor Manufacturers	Probing characteristic inspection	Same screening as is performed on packaged products. Details are specified in the detailed specification.	Same to the left.	As a part of final inspection items for packaged products. Details are specified in the detailed specification.
/Janufacturers	Visual mechanical inspection	Perform a sampling inspection. Details are specified in the detailed specification.	Same to the left.	Same to the left.
	Shipment	The shipment configuration is specified in the detailed specification.	Same to the left.	Same to the left.
	Incoming inspection	The visual mechanical and electric characteristics specified in the detailed specification should be assured.	Same to the left.	Same to the left.
Semiconductor Us	Mounting	Nonconformities resulting from mounting are not assured.	Same to the left.	Same to the left.
Users	Characteristic inspection	Failures resulting from the wafer process (except for characteristic defects resulting from mounting) should be the same level as packaged products should be.)	Same to the left.	Electric characteristics after mounting are not assured.
Market	Early failures	Failures resulting from the wafer process should be the same level as packaged products should be.	Not assured.	Same to the left.
rket	Long-term reliability	Failures resulting from the wafer process should be the same level as packaged products should be.	Not assured.	Same to the left.

4. Supply with Information about Bare Die

Semiconductor manufacturers will supply design information such as circuit design, mounting design, and quality information for users.

4.1 Electric Design Information

Electric design information corresponds to electric specifications of packaged products. The examples are as follows. Electric characteristics are determined by probing. Therefore, test items, conditions, specifications, etc. are frequently restricted:

- (1) Absolute maximum rating/recommended operating conditions
- (2) Pin information such as pin No., function, voltages, outline
- (3) Block diagrams/Pin arrangement
- (4) Electric characteristics
- (5) Circuit block functions and operations

4.2 Physical Design Information

Physical design information is that about package design and mounting design corresponding to bare die. It includes not only that on dimensions and materials but also on restrictions placed upon design and heat resistant design. The examples are as follows:

- (1) Device name
- (2) Dimensions (including tolerances)
 - Die (x, y, t)
 - Pad (x, y, t), pad opening (x, y), pad position coordinate
 - Electrode size (bump, etc.)

Note: Were any electrode, such as bump, has been generated

- (3) Pin-one identification
- (4) Materials
 - -Pad, passivation
 - Coating
 - Die back side
 - -Electrode (bump, etc.)

Note: Were any electrodes, such as bump, have been generated

- (5) Electric potential on the die back side
 - Floating, Vcc, GND, etc.
- (6) Restrictions placed upon packaging and bare mounting
 - Restrictions on design
 - Restrictions on heat resistant design
 - Restrictions on assembly

4.3 Quality Information

Semiconductor manufacturers supply quality information for users after due consultation between two parties.

5. Shipment

5.1 Shipment Configuration

Bare die have to be shipped after appropriate packing to protect them against mechanical damage, electrostatic discharge, contamination, etc. Packing specifications should be in accordance with "Chapter 6 of Handling Guidance for Semiconductor Devices (EIAJ EDR-4701B)." The details will be specified in the detailed specification.

5.2 Traceability

Semiconductor manufacturers have to establish a lot control system to trace bare die wafer lots. Users also have to establish.

5.3 Attached Information at the Time of Shipment

The following information should be attached at the time of shipment:

- (1) Manufacturer
- (2) Device name
- (3) Quantity in the shipment
- (4) Lot number

6. Storage Period Standard

Storage at users should be in accordance with "Chapter 6 of Handling Guidance for Semiconductor Devices (EIAJ EDR-4701B)." The outline is as follows:

- (1) Not yet opened articles
 - Atmosphere: 15 to 35° C/45 to 75% RH
 - -Storage period: within three months
- (2) Opened articles
 - -Atmosphere: dry nitrogen (dew point of -30°C or less) or dry air
 - -Storage period: within twenty days
- (3) Mounting
 - -Period between taking out dice from the packing or dry nitrogen/dry air and mounting: within 5 days

7. Defective Die Handling

Where any nonconformity occurs within the extent of the quality assurance described in Chapter 3, semiconductor manufacturers should consider it as a complaint. A concrete disposal should be consulted between two parties prior to implementation. Information about each complaint should include at least following:

- (1) Configuration of returned articles: Bare die, in principle
- (2) Information: Device name
- -Lot number
- Details of the nonconformity

(Detailed description of the failure mode of each die)

8. References

- (1) "Handling Guidance for Semiconductor Devices (EIAJ EDR-4701B), an EIAJ technical report
- (2) "A Proposal for Required specifications for Procurement of Bare Die and their Standardization" by MCM/KGD Standardization Research Study Group, Electronic Devices Mounting Technical Committee
- (3) "Procurement Standard for Known Good Die" (EIA/JESD 49)

Explanation

1. Background

Bare die shipments were very special cases because only limited industrial fields of users have performed bare die mounting. Generally, semiconductor manufacturers said, "We can not assure bare die characteristics." "We can not assure reliability." Therefore, quality-related items in the specifications are in general "package type" and "open/short" only. Users agreed on the items.

However, electronic equipment has become smaller and lighter day by day. Bare die mounting by users has been no longer special and many consumer-use equipment manufacturers perform bare die mounting at their production process. It is clear that such semiconductor users will increase in the future. User's request for the quality assurance level same as electronic parts, including semiconductor devices becomes stronger and stronger.

In 1996, the MCM/KGD Standardization Research Study Group, Electronic Devices Mounting Technical Committee edited "Requirements Specification and proposal for standardization at the time the bare die are purchased " and JEDEC established "Procurement Standard (EIA/JEDEC 49)."

Then Group on Semiconductor Devices Reliability of Technical Standardization Committee on Semiconductor Devices, EIAJ set the Known good Die/Chip Scale Package Quality Assurance Project Group to discuss bare die quality assurance.

2. Details of Discussions

We have edited the details of discussions and published as a report. The following are the reasons for the above:

It is very difficult to establish a quality assurance standard applying to all bare dice.

It would be necessary to consider "Requirements Specification and proposal for standardization at the time the bare die are purchased." to make users recognize the quality assurance of semiconductor devices and then to deliberate about bare die quality assurance.

We spent the most time to classify bare die quality levels. An opposing argument that even for packaged devices, defining a quality level by "Visual mechanical," "electric characteristics," "early failures" and "long-term reliability" had not yet authorized was proposed.

However, it is concluded that the current classification of levels is effective to make user understand the present quality assurance of bare die, and quality levels are the main subject of this report.

3. Members

This report is the conclusion of discussions among the following:

<Technical Standardization Committee on Semiconductor Devices/Group on Semiconductor Devices Reliability>

Chairman Kazutoshi Miyamoto MITSUBISHI ELECTRIC CORPORATION

EIAJ EDR-4703

<Known Good Die/Chip Scale Package Quality Assurance PG>

Leader Yoshiharu Fukuchi Motorola Japan Ltd.

Sakae Ueno Motorola Japan Ltd. (Nov. 1998~)

Sub-leader Kenji Sasaki Sony Corporation

Members Hirofumi Akiyama KAWASAKI STEEL CORPORATION

Koji Fujita SANYO Electric Co., Ltd.

Hiroyuki Nakamitsu Sharp Corporation

Atsushi Ozawa Nippon Steel Corporation Yoshiji Kiyono New Japan Radio Co.,Ltd

Kiyoshi Komatsu SEIKO EPSON CORPORARTION

Sumito Hayashida IBM Japan,Ltd.

Yasuo Kikuchi Texas Instruments Japan Limited

Makoto Morikawa NEC Corporation

Taisei Jin Hitachi,Ltd.

Akira Yamakawa FUJITSU LIMITED

Hiroshi Matsushima Matsushita Electronics Co.,Ltd.

Yasuo Yamaguchi MITUSUBISHI ELECTRIC CORPORATION