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Guideline for accelerated endurance testing of semiconductor devices

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CONTENTS

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1. Trend of reliability test technology

Technology breakthroughs over the past several decades have made electronic products familiar to the general public. A flood of new electronic products enhance to replace older models, thus product life cycle becomes apparently shorter. On the other hand, some of the products are expected to remain highly reliable for very long term use. The reliability should be correlated to the use condition life cycle.

Modern electronic products contain many semiconductor devices without exception. A semiconductor device comprises a lot of materials (Silicon, Oxide, Aluminum, Dielectric, and so on), and a device also contains more than several millions transistors and electrical conjunctions. Therefore, a device can be considered a very large scale system including its package wiring. Even though such a large scale system, the market sometimes requires higher or the same level reliability as lower density devices. Semiconductor devices are widely accepted as having better reliability than the mechanical parts. However, semiconductor devices should be qualified by the appropriate perspective from its application- specific use requirements.

The precedent reliability test conditions (ex. 1000 hours, 1000 cycles) may not be determined by the reasonable technical experiments.

Essentially, test time or cycles should be appropriately determined by estimating their acceleration factors and mechanisms that are fairly accelerated in the reliability tests. These appropriate considerations can reduce qualification times drastically from the conventional perspective.

Acceleration failure mechanisms can be roughly divided into two categories; intrinsic mode and extrinsic mode. The intrinsic mode is the wear-out failure mode, inherent characteristic of semiconductor device which is based on design rule. Furthermore, the extrinsic mode is interpreted in terms of process induced defects (ex. particle). These extrinsic factors obstruct reliability of inherent characteristic.

The distribution of intrinsic mode is narrow, so the life can be predicted by TEG (Test Element Group) correctly. On the other hand, in the extrinsic mode, the reliability test result is varied by the probability of process defect (external factor). Therefore reliability results strongly depend on sampling population.

Even on small quantity sample / TEG, we can grasp endurance life on intrinsic mode within the sufficient test time. As for the extrinsic mode (early failure mode), we can gather reliability data by using amount of samples within shorter test times.

It should be concluded, from what has been mentioned as two modes of failure, reliability test time can be reduced markedly.

2. Semiconductor reliability theory

This chapter shows theory, a way of thinking that is necessary to understand reliability of semiconductor on statistics.

2.1 A statistical thinking on semiconductor reliability

2.1.1 Reliability

The term "reliability" is defined as follows in "Glossary of Terms Used in Reliability (JIS Z 8115)" :

"The ability of an item to perform a required function under stated conditions for a stated period of time." In addition, its probability is defined as "reliability."

As is clear from the above definition, it is necessary to define the using condition, period and failures.

Note: failure: the termination of the ability of an item to perform a required function.

(1) Operating conditions

Operating conditions consist of the operating stresses which are essentially applied to a device to perform a required function, such as voltage, current, and environmental stresses which are applied from the outside such as temperature and its variation, humidity, vibration.

It is clear that any semiconductor devices will become unable to perform the required function during a short time, result in failure if they are made to operate under extremely severe conditions.

(2) Period

Since reliability has a factor of time, "period," we distinguish between it and quality in a narrow sense.

Therefore, reliability can also be defined as maintenance of quality for a certain time.

The period means a period of time or an amount corresponding to it, such as cycle numbers.

(3)Failures

Failures are classified into:

- a complete failure by which the required function of an item is completely lost;
- a gradual failure in which characteristics of an item gradually deteriorating; or,
- an intermittent failure which is caused by malfunction or imperfect contact of an item. It is difficult to judge whether an item is an intermittent failure or not, and the judgement depends upon the use conditions and/or the person to judge. Therefore, it is important to define the phenomena that are criteria for judging whether a semiconductor device is a failure or not.

2.1.2 Failure Rates

Any quantitative indication is essential to define reliability of these devices. The failure rate is an important indication for the quality level of semiconductor devices. It is introduced by the failure density function and reliability function mentioned below, and is defined as a function of time. However, instead of it, we sometimes use the "mean failure rate" introduced by the total operating hours and the number of failed units, as it is easier to measure.

The failure rate function and mean failure rate are described below.

(1) Failure rate function

The failure rate $\lambda(t)$ is defined as a function of time, the frequency of the failure occurrence of an item per successive unit period where the item has functioned normally until a certain period of time. It can be expressed as a function of failure density function $f(t)$ and reliability function $R(t)$.

At this time, where the number of units is n and the number of failed units at t is $r(t)$, the failure density function $f(t)$ is expressed as follows:

$$f(t) = \lim_{n\to\infty} \lim_{\Delta t\to 0} \frac{r(t+\Delta t) - r(t)}{n} \frac{1}{\Delta t} \quad \cdots (1)$$

In other words, where sample number n is infinity and section Δt is infinitesimal, the function of the successive time is $f(t)$.

And reliability function R(t) which is another function to decide failure rate $\lambda(t)$ is defined as the probability that would not break down by time "t."

This is expressed as follows by failure density function $f(t)$.

$$R(t) = \int_t^{\infty} f(t)\, dt \quad \cdots (2)$$

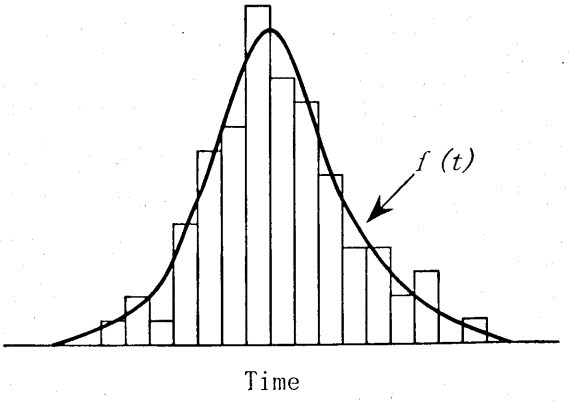
Therefore, failure rate $\lambda(t)$ is expressed as follows by the above two functions. Therefore, it has a dimension of time. As failure rates of semiconductor devices are generally very low, $Fit(=10^{-9}/h)$ is usually used as a unit.

$$\lambda(t) = \frac{f(t)}{R(t)} = \frac{-dR(t)/dt}{R(t)} = \frac{-d\ln R(t)}{d(t)} \quad \cdots (3)$$

The field failure rate $\lambda_1(t)$ of a device is generally presumed from an accelerated life test that is described later. Where the failure rate acceleration factor is "a" and failure rate is $\lambda_2(t)$, $\lambda_1(t)$ is found by solving the following:

$$\lambda_1(t) = \frac{\lambda_2(t)}{a} \quad \cdots (4)$$

Fig. 1 Failure time histogram (example)



(2) Mean failure rates

The term "failure rate" originally meant the above failure function $\lambda(t)$, however, when the reliability function $R(t)$ has not yet been determined, it can not be found. The reliability function $F(t)$ would be found by plotting life data on probability paper, such as the Weibull chart. However, probability paper is not always effective. Therefore, a mean failure rate during a certain period is used. The unit is generally Fit as well as failure rate functions.

$$\text{Mean failure rate} = \frac{\text{the total number of failures}}{\text{The total operating hours}} = \frac{\text{the total number of failures}}{\text{the number of operating units} \times \text{operating hours}} \quad \cdots (5)$$

Moreover, a mean failure rate in the field is found with the accelerated life test as follows:

$$\text{Mean failure rate in the field} = \frac{\text{the total number of failures}}{\text{the number of specimens} \times \text{test hours} \times \text{acceleration factor}} \quad \cdots (6)$$

Note: The failure rate $\lambda(t)$, failure density function $f(t)$ and reliability function R(t) are important measures of reliability of semiconductor devices. The failure distribution function $F(t)$ is also popular. It is called accumulated failure rate, and it is defined as probability to break down by time "t". Relation with reliability function $R(t)$ is as follows:

$$R(t)+F(t)=1 \quad \cdots (7)$$

It is also expressed as follows by failure density function:

$$F(t) = \int_0^t f(t)dt \quad \cdots (8)$$

Various relations between functions mentioned above are shown in Fig. 2 and Fig. 3.

Fig. 2 Relation between $R(t)$ and $F(t)$

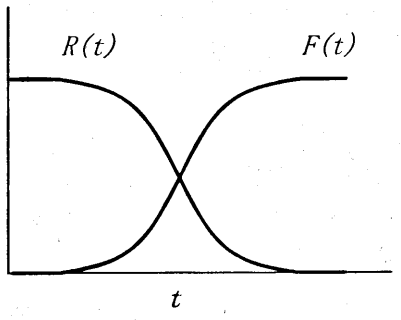
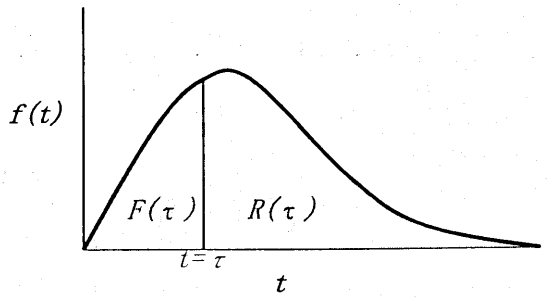


Fig. 3 Relations among $f(t)$, $R(t)$ and $F(t)$



2.2 Weibull Distribution and Bathtub Curve

2.2.1 Failure Rate Patterns

Generally, as time passes, failure rates of unrepaired parts change as shown in Fig. 4. This failure rate curve is divided into three periods, called a "bathtub curve" for its shape.

(1) Initial failure period

Failures resulting from an inherent defect, such as a process defect, (non-essential failure) would occur during the early life period of device operation. The failure rate at early time of this period is very high. However, it has a characteristic that it decreases with passage of time. Especially at the time of setting up of a process, the characteristic is conspicious.

If a wafer process cannot meet the intended failure rate at the time of setting up, defective semiconductor devices are removed by screening such as burn-in. Moreover, semiconductor manufacturers try to reduce defects causing an initial failure not only by screening but also by improving manufacturing processes. Therefore, semiconductor devices which have been shipped generally have a Bathtub-curved-failure rate as shown in Fig. 5.

(2) Random failure period

At the second half of the initial failure period, the number of the devices which are with inherent defects decreases with passage of time, and the failure rate tends to converge at a limit. While between this period and when those failures inheret to the devices, determined by materials, structure and manufacturing processes occur frequently is generally called the "random failure period." The failure rate λ during this period depends on over-stresses applied to the device caused by accidental environmental factors and human mistakes, etc.

It is said that the random failure periods of a semiconductor device are longer than that of other parts, and its failure rate is lower.

(3) Wear-out failure period

After a long term of the random failure period, essential failures determined by materials, structure and manufacturing process come to occur, and the life inherent to each device comes to be indicated. This period is called the "ware-out failure period." The failure rate during this period increases with the passage of time.

Fig. 4 Bathtub curve (General)

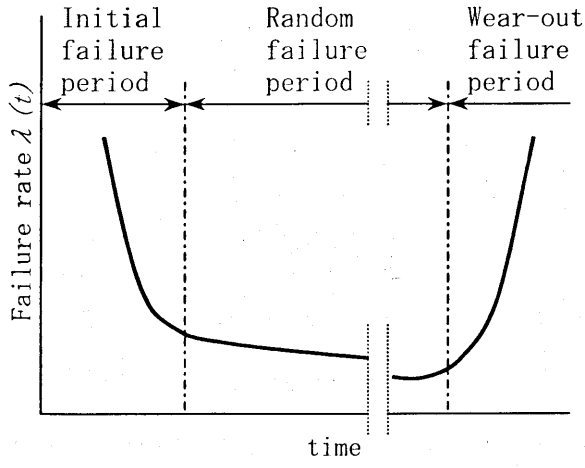
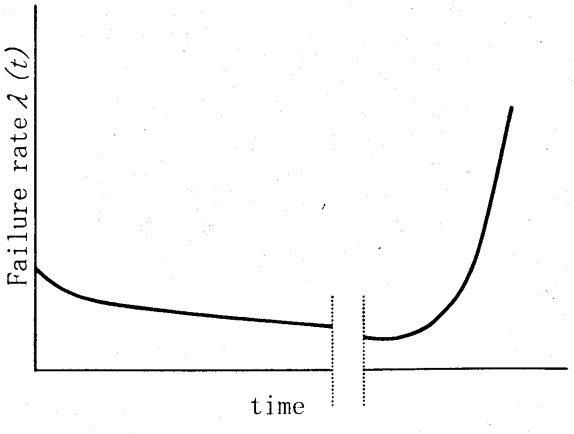


Fig. 5 Actual bathtub curve of semiconductor



2.2.2 Reliability Distribution Function

Any product life has a distribution because each semiconductor device belonging to electronic parts has a complex system consisting of materials, structure and manufacturing process, which are factors determining the reliability, which have dispersion. Moreover, during actual using, both device operation stresses and environmental stresses also have dispersion.

Therefore, when product reliability is considered, it is important to grasp the life distribution of the population, failure distribution function. Those statistical models, which indicate failure distributions of semiconductor devices, are known by experience. They are exponential distribution, lognormal distribution and the Weibull distribution. The Weibull distribution is described below which can apply to various failure modes.

2.2.3 Weibull Distribution and its Application

The Weibull distribution was proposed by W. Weibull, of Sweden for destruction strength of machines in 1939, and it is said that it has become popular as a reliability model since J.H.K.Kao applied it to the life of vacuum tubes in 1955. It is a model that generalizes exponential distribution. The reliability function R(t), failure density function $f(t)$ and failure rate λ (t) are expressed as follows. At this time, m is the shape parameter which determines the distribution shape, η is the measure parameter (characteristic life) and γ is the potential parameter.

$$R(t) = exp\left\{-\left(\frac{t-\gamma}{\eta}\right)^{m}\right\} \quad \cdots (9)$$

$$f(t) = \frac{m}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{m-1} exp\left\{-\left(\frac{t-\gamma}{\eta}\right)^{m}\right\} \quad \cdots (10)$$

$$\lambda(t) = \frac{m}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{m-1} \quad \cdots (11)$$

From Equation (11), the failure rate $\lambda(t)$ is:
a decreasing function when m<1;
constant when m=1; and,
an increasing function when 1<m.
In other words, the type of the failures, initial failure, random failure or wear-out failure on the bathtub curve above, can be determined by finding the value of m.
And the reliability function $R(t)$, failure density function $f(t)$ and failure rate $\lambda(t)$ at the random failure period are as follows by substituting 1 for m. They comply with an exponential distribution. (For simplifying equations, γ is regarded as 0.)

$$R(t) = exp(-\lambda t) \quad \cdots (12)$$

$$f(t) = \lambda exp(-\lambda t) \quad \cdots (13)$$

$$\lambda(t) = \frac{1}{\eta} \quad \cdots (14)$$

Moreover, in the area near the point "m=2," the failure density function $f(t)$ approximates to a lognormal distribution, and " m=4, " approximates to an exponential distribution. See figures for $R(t)$, $f(t)$ and $\lambda(t)$ values when m=0.5, 1, 2 and 4.

The Weibull distribution can cover the whole area of the bathtub curve by changing the value of m. Moreover, we have found that it approximates to a normal distribution and lognormal distribution.

Thus, it can apply to various reliability data. Lastly, The characteristic life η and potential parameter γ are described below.

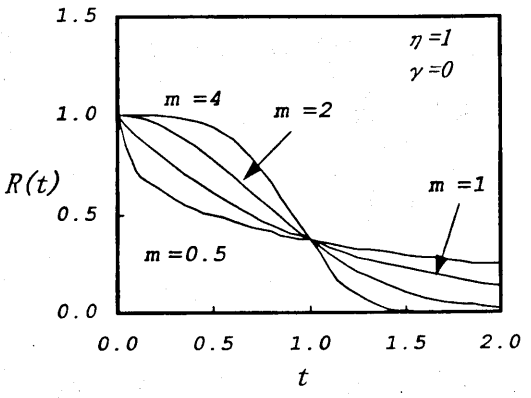
By substituting η for t of Equation (12) above, the following equation is given:

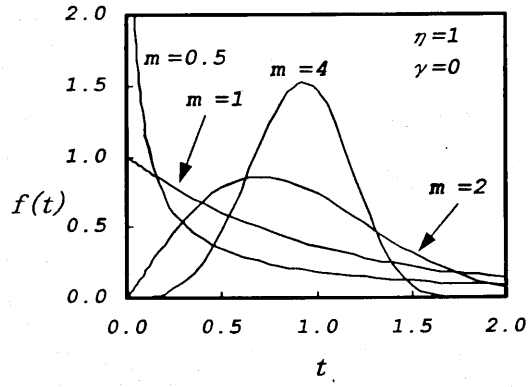
$$R(t) = exp(-1) \fallingdotseq 0.368 \quad \cdots (15)$$

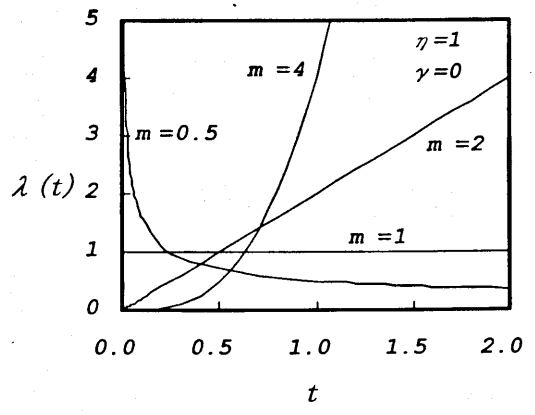
In other words, the characteristic life η is that when the reliability is approx. 36.8%. On the other hand, the potential parameter γ is used to adjust the time difference between the time when the observation began and when the failure mechanism started, if it was caused for any reasons.

Because in general, the potential parameter γ is seldom used, I will use the Weibull distribution whose γ is 0, in Chapter 3 and after.

Fig. 6 Weibull distribution







2.3 Reasons for tendency of failure rate during each failure period

As described in 2.2, the failure rate of electrical components, such as semiconductor devices, follows a bathtub curve comprising an early failure period, a random failure period, and a wear-out failure period.

In the early failure period, the failure rate decreases with time, and in the random failure period, the failure rate is random regardless of time. In the wear-out failure period, the failure rate increases over time. The likely reasons for this pattern are explained in the following.

2.3.1 Causes of early failure

Since semiconductor devices are complicated and minute, they are affected by defects that occur during fabrication. At the end of fabrication, an acceptance test is performed in which acceptable devices that satisfy specified AC, DC and other functions are selected. The ratio of acceptable devices to the total number of devices is called the yield. Although every possible item is subject to measurement to select acceptable devices during the acceptance test, the selected devices may still include defects that are not apparent during acceptance test. When the yield is high, the possibility of acceptable devices having defects is low, but when the yield is low, the possibility is high. When a defective semiconductor device is used, failure may occur because of the defect(Extrinsic Mode).

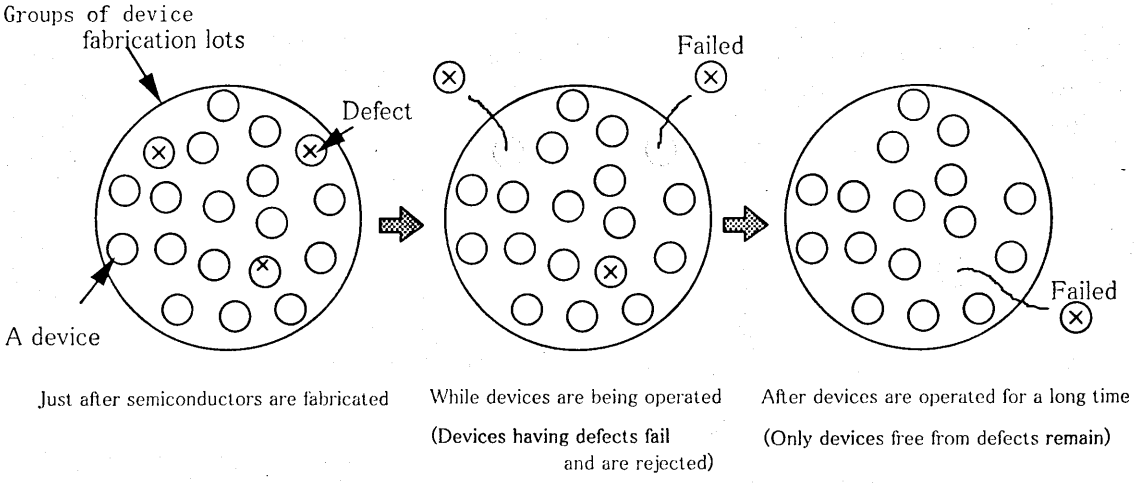
When a small number of acceptable devices having defects are included in a fabrication lot, the failure rate decreases with time, since the semiconductor devices free from defects, that is, low-failure-possibility semiconductor devices remain, after semiconductor devices having defects are rejected because of failure. In this case, the shape parameter m of the Weibull distribution is less than 1.

As shown in Fig. 7, a small number of acceptable devices having defects remain in the fabrication lot, the devices having defects become failures with time during the operation of electronic system that the devices are applied, the failed devices will be rejected (replaced) by repair, and in the long run only highly reliable devices remain.

Defects occurring during fabrication should be eliminated (failure-reduction measures). For example, the device design can be changed, if possible, so that devices are not affected by such defects.

Also, a burn-in period can be used as a screening method, in which devices having defects are made to fail in advance by operating the devices under severe conditions. The failed devices are then rejected during a acceptance test. In this process, the early failure period of semiconductor devices is spend beforehand to lower the early failure rate after shipment. The screening can be stopped or the conditions relaxed, though, if the effectiveness of the failure-reduction measures has been demonstrated.

Fig. 7 Transition of failure occurring in semiconductor fabrication lots during early failure period



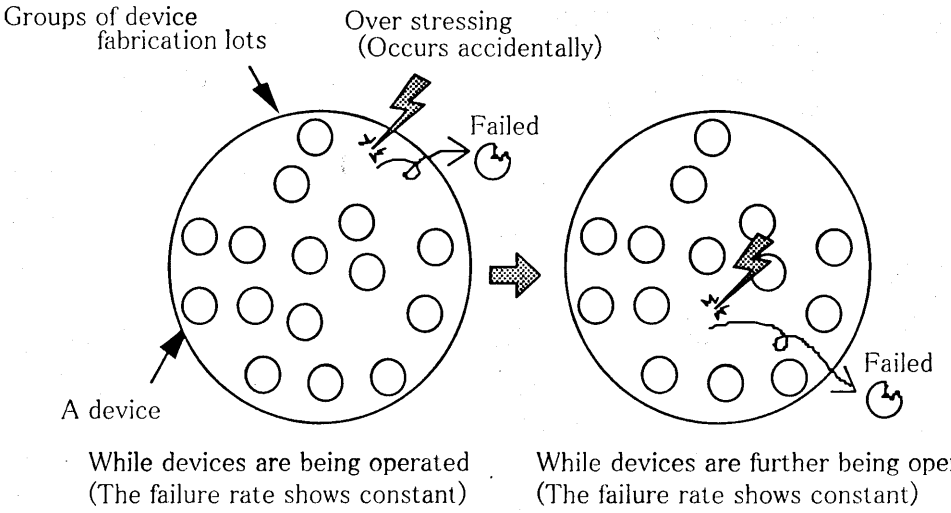
2.3.2 Causes of random failure

The failure rate due to manufacturing defects decreases over time. If the degree of defects is slight, however, the failure rate will have an exponential distribution with a random failure. If defective semiconductor devices can be removed by screening, the failure rate after the screening will become close to the exponential distribution. Therefore, the exponential distribution has been used for calculating the semiconductor failure rate after defective devices are removed. However, slight failure still remains in some semiconductor devices even after the screening. These semiconductor devices eventually fail after being used for a long time, though, so in a strict sense the failure rate in this period can be classified as early failure of a decreasing type.

The random failure in a strict sense is caused by over-stressing, such as soft errors of the memory devices due to alpha particle rays and electrical over-stressing (EOS). Since over-stressing is generated accidentally, the failure rate will become random as shown in Fig. 8. Accordingly, the failure rate depends on the resistance (basic specifications) of each device against over-stressing.

When the failure rate is random, the shape parameter m of the Weibull distribution becomes 1, and the failure rate function shows the characteristics of an exponential distribution.

Fig. 8 Transition of failure occurring in device fabrication lots during random failure period

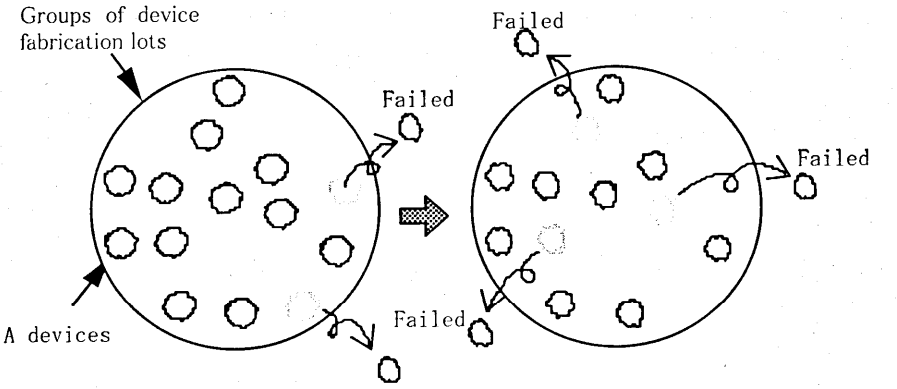


2.3.3 Cause of wear-out failure

Any semiconductor device will eventually fail even if free from defects. This failure occurs due to the expiration of the substantial lifetime. Although the time to failure of each device is different depending on the deviation during fabrication and the stress applied during use, the lifetime of any device gradually and finally will expire, and consequently failure rates gradually increase as shown in Fig. 9.

In general, the wear-out failure period (which ranges from several tens to several hundreds of years) of semiconductor devices is longer than the life of the electronic system in which these devices are applied, and the actual wear-out failure period will depend on the basic specifications of each devices. The durability can be verified by several reliability tests. During the increasing failure-rate period, the shape parameter m of the Weibull distribution exceeds 1. For wear-out failure ($1 < m$), an endurance test that is equivalent to several times to several hundreds of times the life of electronic system is performed using a few samples (several pieces to several tens of pieces). This test confirms, using the failure distribution function, that the failure rate will be sufficiently low during the period of practical use.

Fig. 9 Transition of failure occurring in device fabrication lots during wear-out failure period



2.4 The acceleration factor in reliability test

An acceleration factor related to the actual user environment is needed to calculate the failure rate from the reliability test results. The device of the test time and the acceleration factor represents the assumed working hours under actual conditions. However, since each failure has a different cause (i.e., different physical or chemical reactions), the acceleration factor must be changed depending on the failure mode, even if the testing is the same.

2.5 Lifetime estimation based on test results

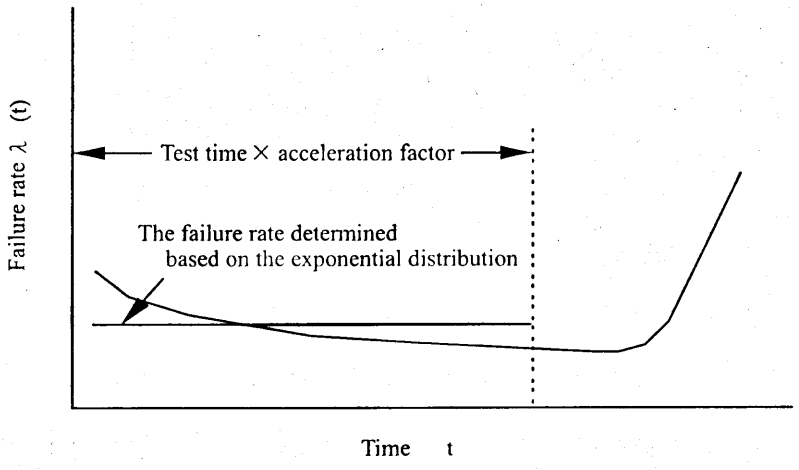
2.5.1 Lifetime estimation based on exponential distribution

Under the assumption that most early failures are eliminated through screening before semiconductor devices are shipped, the failure rate is determined according to equation (14) based on an exponential distribution. The obtained failure rate is the average failure rate from 0 hours to value of "test time by acceleration factor" hours as shown in Fig. 10.

In practice, when no wear-out failure occurs, it is natural to assume a continuation of the early failure time in which the failure rate gradually decreases. Therefore, the early failure rate will be higher than the value obtained from equation (16) and the failure rate at value of "test time by acceleration factor" hours will be lower than the obtained value.

Average failure rate = (Number of total defects)/(Number of total test samples × test time × acceleration factor for the test) ・・・(16)

Fig. 10 Relation between the failure rate obtained from exponential distribution and the transition of the actual failure rate



In general, testing is performed using several tens of samples. This quantity is sufficient for evaluation of wear-out failure, but is insufficient for evaluation of early failure. When the failure rate is determined using equation (16), the accuracy should be improved by adding test data from other devices by the same design rules, the same fabrication process and specifications.

To obtain the mean time between failures (MTBF) of an electronic system, the mean time to failure (MTTF) of the semiconductor devices used in the system is required. Under the assumption that the MTBF and MTTF follow an exponential distribution, the MTTF is the reciprocal of the failure rate.

2.5.2 Estimation of the failure rate transition during assumed period of use based on the Weibull distribution

For the Weibull distribution, the failure rate can be expressed as in equation (11). When m and η are obtained after plotting the test data on the Weibull distribution form, the failure rate at operation time t can be obtained. In this case, the value of η is the device of the η obtained from the test data multiplied by acceleration factor used for the test.

(1) Transition of the early failure rate based on the burn-in data and its acceleration factor

By plotting burn-in data obtained over a period from several hours to several tens of hours on the Weibull distribution form, the values of m and η can be obtained. Accordingly, the failure-rate distribution during the early failure period can be obtained from equation (11) as a function of t. The burn-in data of several thousand to several tens of thousands

of devices for several hours to several tens of hours, is required to obtain the failure rate function. However, the failure rate can be estimated from a small sample size with fewer test hours if the failure rate is high.

(2) Random failure rate

The failure rate in the failure mode that corresponds to random failure rate, such as failure caused by soft errors, is also calculated. Since the failures follow an exponential distribution, the failure rate can be obtained in the same way as in 2.5.1.

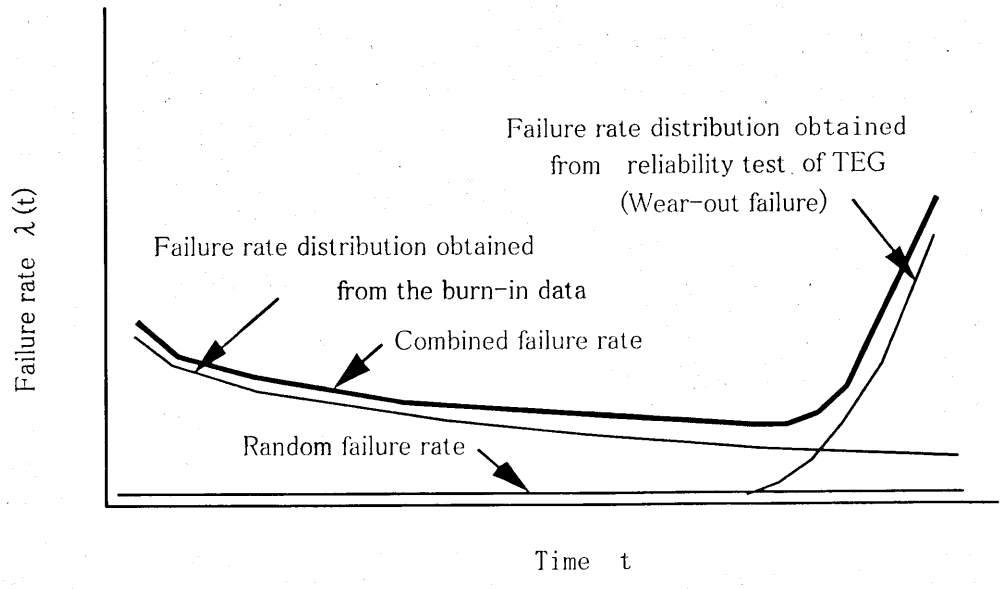
(3) Failure-rate estimation during wear-out failure period

In the case of wear-out failure, the failure distribution can be obtained by using a small number of samples because the failure rate becomes high. In addition, when the reliability test is done for a period of time that is much longer than the life of application system, it confirms that the failure rate during the practical use period is significantly low, according to the failure-rate distribution, because $1 < m$ even if the number of samples is small.

Since the metal layer of actual devices cannot be exposed to a high current to test for failures due to electro-migration, a test resulting in wear-out failure cannot be performed. For this reason, the failure distribution is obtained by a test using a TEG (Test Element Group) with metal layer to ensure that the lifetime obtained from the test result is longer than the target lifetime of the actual device. In addition, because $1 < m$, the test data obtained from a small number of samples can confirm that the failure rate during the actual period of use is sufficiently low.

As shown in Fig. 11, the device lifetime can be estimated by adding the failure-rate distributions obtained from (1) to (3) above.

Fig. 11 The obtained failure rate distribution and the combined failure rate



2.6 Position of long-term test

In general, when the acceleration factor is taken into account, the reliability test is equivalent to several times to several hundreds of times the expected period of actual use. This period is sufficiently long to confirm that no wear-out failure will occur during use. Accordingly, if the test time is doubled or tripled, it will be no more effective from the viewpoint of confirmation of the failure rate in the actual use.

As long as the specifications of the basic structure and the fabrication process for semiconductor devices are not changed, the tendency of wear-out failure to occur (failures intrinsic to semiconductors in general) may not significantly change in the future. Therefore, a long-term test that is equivalent to several times to several hundreds of times the expected period of actual use is sufficient even if the lifetime of actual semiconductor devices is decreased to half. Accordingly, repetition of longer-term tests using other fabrication lots will be no more effective for estimating the failure rate within the period of use.

2.7 Position of tests without acceleration

In tests without acceleration (tests unrelated to the actual environment), failures that are unlikely to occur in actual user environments are artificially created by applying stress that usually is not applied in actual use. This test is not effective for estimating the failure rate under actual conditions of use. Therefore, locating the cause of failures that occur in such tests and resolving the problems are not necessary from the viewpoint of improving semiconductor reliability.

Examples of test methods without acceleration are the saturation-type pressure cooker test (Autoclave test), and the impact test and the acceleration test targeting plastic packages which must be performed for hermetic packages. In EAIJ ED-4701, the autoclave test was eliminated and the scope of testing is clarified.

3. What is an acceleration life test ?

3.1 Principle of acceleration test

While a reliability test attempts to simulate the stress to which a semiconductor device will be subjected in actual use (Refer to Table 1), in certain cases, it will require an extremely long period to actually cause failure of the device under testing. Limited testing time may mean that the device under testing will not reach the failure criteria during the test period. To compensate for the lack of testing time, an accelerated test applies more severe stress than during actual use to accelerate degradation. It enables estimation of life and failure rate, and reduces the time required for evaluation.

The acceleration differs for each failure mechanism. The accelerated test assumes that the failure mode and mechanism do not change by acceleration. When selecting the accelerating stress, the device structure, process, application, and type of failure must be considered carefully. Basically, the acceleration test enhances the failure modes in early failure period and wear-out failure period.

There are two types of accelerated life test methods:

(a) Constant stress method: A constant stress is applied to the sample and the distribution of time to failure for several levels of constant stresses is observed.

(b) Step stress method: The stress applied to the sample is periodically reased in steps and the step that caused failure is determined.

These test methods are used individually or in combination. The degree of acceleration is investigated and used to predict the device life and failure rate.

It is sometimes possible to know the failure limits of the device. In such cases, the test is also called a limit test. Limit tests are used to determine life limits as well as mechanical strength, and resistance to electrical surges and overloads.

A typical method is the temperature accelerated test. The relationship between the constant stress and step stress temperature acceleration methods is illustrated in Fig. 12. Note that the short broken lines connecting the steps of the step stress method are parallel to a long broken line that indicates the life limit. This means that the device deterioration caused by the previous steps accumulates. In normal step stress testing, the steps are spaced so that the effect of previous steps can be ignored, which facilitates analysis of test. A breakdown voltage measurement test of silicon oxide layer is a typical test of step stress method, and shows a good relationship shown in Fig. 12 with TDDB test , which is a constant stress method.

Fig. 12 Accelerated life test (constant stress vs. step stress)

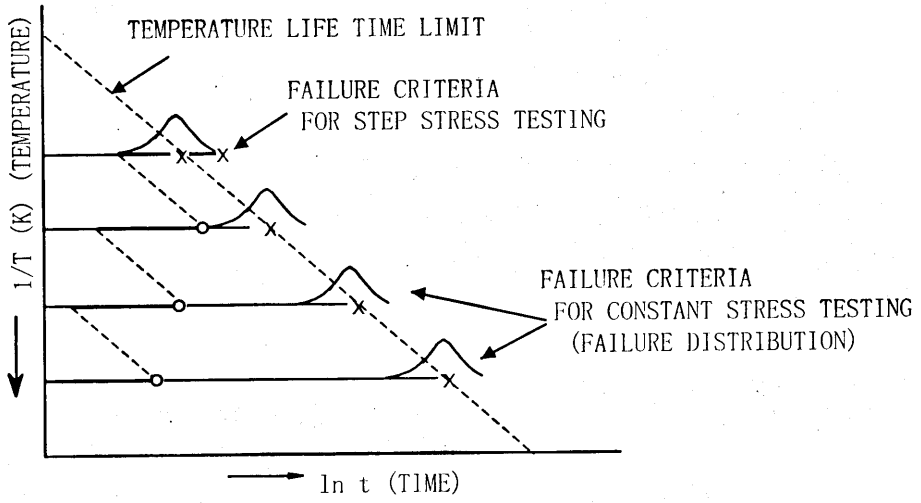


Table 1 An environmental stress and operating stress

Environmental stress		Operating stress	Stress forcing
Natural	Temperature and its drift	Voltage	Steady state / Intermittent
	Humidity and its drift	Current	Time
	Rain, Water	Noise	The number of stress
	Wind	Electric field	Frequency of cycling
	Thunder	Magnetic field	Periodicity
	Pressure(Low, High)	Temperature increasing	Repeat of stress
	Particle, Dust	Local heating	Change of stress
	Mold, Bacterium		Velocity
	Radiant rays		Sequence of stress
	Electromagnetic waves		
	Corrosive atmosphere		
Artificial	Soldering		
	Solvent		
	Shock, Drop		
	Vibration		
	Pull, Bending		

3.2 Acceleration models

In analyzing the data that was obtained by the acceleration test, the various acceleration models are proposed. Here, the representative models are explained.

3.2.1 Arrhenius model

Semiconductor devices depend on chemical or physical change of the substance. The failure reaction model that is used generally is the model that breaks out when harmful chemical, physical reaction for the device goes on and reaches a certain limit. Usually, the semiconductor devices are exposed to an electric stress, heat stress, mechanical stress. In those stress conditions, the semiconductor is most sensitive to temperature. The relation between this temperature stress and reaction rate was found by Arrhenius. And, it is widely utilized in the semiconductor device field as the Arrhenius model. In the empirical chemical reaction thesis of Arrhenius, the reaction rate K is expressed as

$$K = A \cdot \exp\left(-\frac{Ea}{kT}\right) \quad \cdots \quad (17)$$

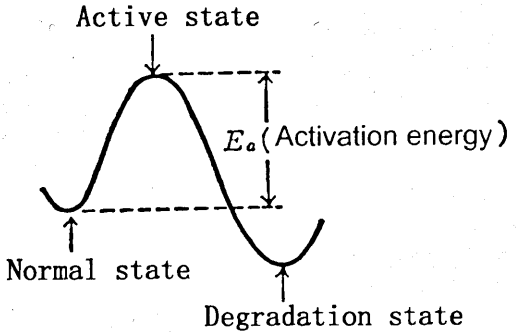
where A = constant,
Ea = activation energy in electron volts(eV),
k = Boltzmann's constant 8.617×10^{-5}(eV/K),
T = absolute temperature of system in kelvins(K)

In the chemical reaction, there is a wall of energy in the midway of the process which goes ahead from normal state to degradation state, as shown in Fig. 13.

To overcome it, necessary energy must be supplied from the outside.
The wall of this energy is called as activation energy.

If it is supposed that the lifetime L is inversely proportional to the reaction rate k, by using this equation the temperature acceleration factor α_T is given by

Fig. 13 Acyivation energy



$$\alpha_T = \frac{L_1}{L_2} = e^{\frac{Ea}{k}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)} \quad \cdots (18)$$

where T1, L1 = Temperature and lifetime of standard condition (e.g. it is a standard use condition.)
T2, L2 = Temperature and lifetime of acceleration condition

From this equation, the acceleration factor clearly is changed by the activation energy Ea. The relation of activation energy and acceleration factor is demonstrated in Fig. 14. Also, the activation energy is the thing peculiar to the activation process of an individual phenomenon. Accordingly, the failure cause can be estimated from activation energy. The failure mechanisms and activation energy of representative semiconductor devices are shown in Table 2.

3.2.2 Eyring Model [1]

There is a failure model that considers the influence of voltage stress and mechanical stress other than temperature. It is the Eyring Model that is developed from the Arrhenius reaction model. Chemistry reaction rate K of the Eyring Model is expressed as

$$K = A \cdot \left(\frac{kT}{h}\right) \cdot e^{-\frac{Ea}{kT}} \cdot e^{\left\{f(s)\cdot\left(C+\frac{D}{kT}\right)\right\}} \quad \cdots (19)$$

where, A, C, D = constant, Ea = activation energy (eV),
k = Boltzmann's constant 8.617×10^{-5} (eV/K),
T = absolute temperature (K), h = Planck's constant,
$f(s)$ = function of stress "s" other than temperature

If the following equations are assumed

$$\Lambda = A\frac{k}{h}, \quad f(s) = \ln s, \quad F = C+\frac{D}{kT}$$

the above equation is approximated to the next equation with the narrow area of T.

$$K = \Lambda\, T\, e^{-\frac{Ea}{kT}}\, s^F \quad \cdots (20)$$

Fig. 14 Relationship between the acceleration factor and activation energy

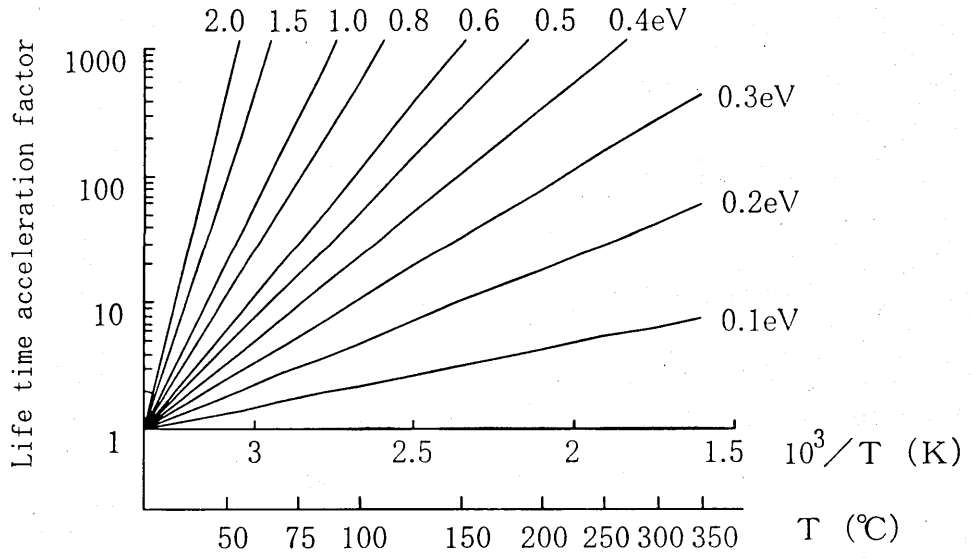


Table 2 Failure mechanism and activation energy of semiconductor devices

Failure mode	Failure mechanism	Evaluation device	activation energy (eV)
Open circuit	Au-Al intermetallic formation	I C	1.0 - 1.05 [2][3]
	Aluminum electromigration	I C	0.55 - 1.0
	Aluminum corrosion (Penetration of water)	I C (Plastic package)	0.8 - 1.2
Short circuit	Dielectric breakdown	MOS I C	0.3 - 1.2
	PN junction breakdown (Al-Si Solid phase reaction)	-	3.5 [5]
	PN junction breakdown (Al-Si Solid phase reaction)	Diode (Gold electrode)	1.4 - 1.6 [2][3][6]
	Gold electromigration (Dendrite)	Transistor(Microwave)	0.6 [7]
Outer lead rupture	Stress-corrosion cracking of KOVAR (Saltiness environment)	I C (KOVAR frame)	0.65 [8]
Current amplification factor decline	Acceleration of the ionic migration by water	Transistor (Plastic package)	0.8 [9]
Leak current incrementation	Formation of the inversion layer	MOS device	0.8 - 1.0 [10][11]
Storage characteristics change	Leakage of Si oxide	MOS IC (EPROM)	0.8 - 1.15 [12][13]
Threshold voltage change	Polarization of phosphorus glass	MOS device	1.0 [14]
	Drift of the Na ion in Si oxide	MOS device	0.68 - 1.93 [4]
	Slow trapping in the Si-Si oxide interface	MOS device	1.0 - 1.3 [2][3][15]

3.2.3 Humidity acceleration models

The acceleration factors of the moisture resistance evaluation are the next.

(a) amount of the moisture quantity. (relative humidity, absolute humidity)
(b) speed of moisture diffusion. (temperature, pressure),
(c) speed of dissolution and chemical reaction. (temperature, electric field, current density)

There are many moisture resistance test method that those factor are considered. However, these tests can not be unified to one test, because many factors influence moisture resistance. Accordingly, many models are reported regarding the acceleration model. The representative models are below.

(1) Vp model: Lifetime L that reaches to the certain accumulation failure rate is a function of water vapor pressure Vp. [16][17]

$$L = A \cdot (V_p)^n \quad \cdots \quad (21)$$

where A = constant
n = -2 (typical value)

(2) RH model1: Lifetime L that reaches to the certain accumulation failure rate is a function of relative humidity RH (%) and temperature T (K). [18]

$$L = A \cdot (RH)^{-n} \times \exp\left(\frac{Ea}{kT}\right) \quad \cdots \quad (22)$$

where A = constant, Ea = activation energy(eV),
k = Boltzmann's constant 8.617×10^{-5}(eV/K),
Ea = 0.8 - 1.2 eV(reference value), n=4.0 - 6.0(reference value)

(3) RH model2 (Lycoudes model): Lifetime L that reaches to the certain accumulation failure rate is a function of relative humidity RH (%) and temperature T (K). [18]

$$L = A \times \exp\left(\frac{B}{RH}\right) \times \exp\left(\frac{Ea}{kT}\right) \quad \cdots \quad (23)$$

where A = constant,
k = Boltzmann's constant 8.617×10^{-5}(eV/K),
Ea = activation energy 0.8 - 1.2 eV(reference value)
B differs largely by failure mode.

3.2.4 Voltage acceleration model [19]

Unless an experimentally validated voltage acceleration model has been derived, the following model is used empirically.

$$K = A \cdot \exp\left[\left(\frac{\beta}{t}\right) \cdot V\right] = A \cdot \exp(B \cdot V) \quad \cdots \quad (24)$$

where K = reaction rate, A = constant
β = electric field coefficient (cm/V),
V = voltage, B = (β/t),
t = gate oxide thickness

From this equation, the voltage acceleration factor α_V is given by

$$\alpha_V = \frac{L_1}{L_2} = \exp[B \cdot (V_2 - V_1)] \quad \cdots \quad (25)$$

where V1, L1 = voltage and lifetime of standard condition.
V2, L2 = voltage and lifetime of acceleration condition.

3.2.5 Degradation models by hot carriers

When the field strength near the drain becomes high in MOSFET, the carriers(electron, hole) that flowed into the high electric field area acquire very high energy by this electric field.

At this time, a part of carriers change to the hot carriers that have higher energy than the electric potential barrier between gate oxide and silicon substrate. And, the hot carriers are injected into the gate oxide. The hot carriers that were injected change to gate current. And those reach the gate electrode. With the process, a part of hot carriers are captured into the gate oxide. Furthermore, unstable (interface state) of the structure is caused in the boundary of oxide and silicon, when the hot carriers were injected into the gate oxide. These electric charge that occurred into the gate oxide forms space charge. This space charge varies characteristics (Vth, gm etc.) of FET. And, this variation is the factor that damages the integrated circuit reliability.

The following models are reported regarding the characteristics degradation by hot carriers.

3.2.5.1 Estimation of DC lifetime

(1) Estimation by exp(1/Vds) model (n-channel, p-channel) [20]

The straight line relation is obtained for both n-channel MOSFET and p-channel MOSFET when the hot carrier degradation time τ is plotted in the linear-logarithm graph as a function of the reciprocal stress voltage Vds. That is, there is a relation expressed as

$$\tau = A \cdot \exp\left(\frac{B}{V_{ds}}\right) \qquad \cdots \quad (26)$$

where A, B = constant B = about 100-200 for n-channel MOSFET

(2) Estimation by substrate current model(n-channel) [21]

In n-channel MOSFET, the straight line relation between the hot carrier degradation lifetime τ and the substrate current Ib under the stress test is obtained in both logarithm graph. This relation is expressed as

$$\tau = C \times I_b^{-m} \qquad \cdots \quad (27)$$

where C , m = constant. M = about 2-4 for n-channel MOSFET.

It is said that the next expression is better in sub-micron n-channel MOSFET of 0.5um or less.

$$\tau \times I_d = D \times \left(\frac{I_b}{I_d}\right)^{-m} \qquad \cdots \quad (28)$$

where D = constant. Id = drain current

It is said that the lifetime can be presented by one straight line using this equation for any n-channel MOSFET with different gate length.

(3) Estimation by gate current model (p-channel) [22][23]

In p-channel MOSFET, the straight line relation is obtained when the gate current Ig is plotted as a function of the hot carrier degradation lifetime τ under the stress test in both logarithm graph. This straight line relation is expressed as

$$\tau = C \times I_g^{-m} \quad \cdots (29)$$

where C , m = constant.

3.2.5.2 Estimation of AC lifetime

(1) Duty method [24]

Duty method is the easiest method to estimate the amount of degradation under an actual operating condition from the relation based on the accelerated degradation test of DC stress. This method is to estimate the degradation based on the assumption that the degradation happens only at the rising time Tr and falling time Tf as much as under a DC worst stress. That is,

$$t(AC) = t(DC)\frac{t_{cycle}}{(t_r + t_f)} \quad \cdots (30)$$

where t(AC) = AC lifetime that reaches to certain degradation.
t(DC) = DC lifetime that reaches to certain degradation.
And t(AC)/t(DC) is called as duty ratio.

As for this method, the calculation is easily performed with enough accuracy, although there is a tendency to overestimate the amount of degradation. Therefore, it is very useful from the practical point of view. But, presumably, the degradation does not take place uniformly during pulse transition. Therefore, one can choose a coefficient which is multiplied to tr and tf as a variation of this method. Also, there is another method in which only one of tr or tf can be chosen for the calculation.

(2) Wavy split plot method [25][26]

The substrate current changes dynamically during AC operation. Therefore the switching process is divided into short periods and we assume that degradation to the same extent as under the DC stress with the same substrate current happens in each short period. After summing up the degradation in short periods, the total degradation during AC operation is obtained. Therefore, lifetime under the AC operation can be shown as follows:

$$t(AC) = \frac{t_{cycle} \times C}{\int_0^{t_{cycle}} [I_b(t)]^m dt} \quad \cdots (31)$$

where $$I_b = a \times I_d \times E_{xd} \times \exp\left(-\frac{b}{E_{xd}}\right)$$

$$E_{xd} = \left[\alpha^2 (V_{ds} - V_{dsat})^2 + E_C^2\right]^{1/2}$$

a, b, α, Ec = adjustable parameter. V_{dsat} = saturation voltage.
Because this expression is not suitable on the high region of a gate-source voltage V_{gs}, V_d-V_{dsat} is assumed to be V_d-0.6V_{dsat} etc. and the term of exponential is substituted for the power of Exd occasionally.

(3) BERT [27]

BERT (Berkeley Reliability Tool) is reliability predictive tool developed by C.H.Hu of University of California, Berkeley. The hot carrier degradation model in BERT is expressed as

$$\Delta D = K t^{n}$$

where ΔD = amounts of the degradation such as Id and Gm.
t = time
n = constant

The lifetime τ of n-channel MOSFET is given by

$$\tau\left[\frac{I_d}{W}\right] = \frac{H}{K}\Delta D^{1/n}\left[\frac{I_b}{I_d}\right]^{-m} \quad \cdots (32)$$

The lifetime τ of p-channel MOSFET is similarly given by

$$\tau = \frac{H}{K}\Delta D^{1/n}\left[\frac{I_g}{W}\right]^{-m} \quad \cdots (33)$$

Although H and m depend on the drain-gate voltage strictly, only H is usually treated voltage-dependent. That is,

H=E(Vds-Vgs)+F or log(H) = E(Vds -Vgs) + F

3.2.6 Degradation models by a slow trap

There are many distortions of the Si-Si connections and many connections of Si-H、Si-OH in the interface of silicon and oxide. As for these connections the bonding strength is weak. Great energy is not needed to disconnect the connections. Therefore, the connections of Si-H or Si-OH that are in the transition region can be broken down by temperature, electric field stress. And the fixed electric charges and interface states are formed to the interface. These are the factors that cause Vth variation.

There are the following acceleration model reports related to a slow trap. [28]

(1) Vth variation of p-channel MOSFET

The voltage acceleration is expressed as

$$L \propto \exp(b \cdot V_a) \quad \cdots (34)$$

where L = Lifetime
b = voltage acceleration factor b=0.8
Va = applied voltage

The temperature acceleration is shown with the Arrhenius model.

$$L \propto \exp\left(\frac{Ea}{kT}\right) \quad \cdots (35)$$

where L = Lifetime
Ea = activation energy Ea=1.0 eV
T = absolute temperature

(2) Vth variation of n-channel MOSFET

It is reported that Nch MOSFET has no voltage dependence and temperature dependence.

3.2.7 Degradation models by TDDB [29][30][31][33][34]

TDDB is the phenomenon that the oxide dielectric breakdown is caused (time-dependent dielectric breakdown), by applying continuous voltage stress or current stress.

The following two models are generally proposed as acceleration models regarding TDDB.

(1) Eox model

This is the model that the lifetime is empirically expressed as the next equation regarding temperature and oxide electric field.

$$\text{(a)} \quad TTF = A \cdot \exp\left(\frac{Ea}{kT}\right) \cdot \exp\left(-\beta \cdot E_{ox}\right) \quad \cdots \quad (36)$$

$$\text{or} \quad \text{(b)} \quad TTF = A \cdot \exp\left(\frac{Ea}{kT}\right) \cdot 10^{-\beta \cdot E_{ox}} \quad \cdots \quad (37)$$

where TTF = time to failure, A = constant,
Eox = oxide electric field(MV/cm),
k = Boltzmann's constant 8.617×10^{-5}(eV/K),
β = electric field acceleration parameter,
Ea = activation energy(eV)

Electric field acceleration parameter β is calculated by using this model. However, as for the β value, there is a big difference by the report. This is showing that the failure model is not simple like the above equation.

The reference value of β and Ea are as follows.

Ea =0.5 eV (Typical) (0.3 - 1.0)
β =1 - 7 for equation (a).
β =0.43 - 3 for equation (b).

(2) 1/Eox model [32]

This is the model that lifetime is expressed as the next equation regarding temperature and the oxide electric field. And this is the model based on the following hypothesis.

When the electric field to the gate oxide is over 5 - 6MV/cm, the carriers are injected into the gate oxide by Fowler Nordheim tunneling effect and electric current flows. And, the holes and electrons that were injected are accelerated by the electric field in the gate oxide and the holes that occurred by causing ionization by collision cause the gate oxide dielectric breakdown.

$$TTF = A \cdot \exp\left(\frac{Ea}{kT}\right) \cdot \exp\left(\frac{B + H}{E_{ox}}\right) \quad \cdots \quad (38)$$

where TTF = time to failure, A = constant,
Eox = oxide electric field (MV/cm),
k = Boltzmann Constant 8.617×10^{-5}(eV/K),
B, H = constant(240MV/cm, 80MV/cm)
Ea = activation energy(eV)

Lifetime estimation by using 1/Eox model gives us an optimistic value of lifetime compared with Eox model estimation. However, the failure model of TDDB is not clear. Accordingly, at present, both models are used.

3.2.8 Temperature cycle acceleration model

The temperature cycle acceleration model adopts the Eyring model generally. The relation between the temperature difference that is added repeatedly and breakdown lifetime (cycle number) is expressed as

$$L = A \cdot (\Delta T)^{-n} \quad \cdots (39)$$

where L = lifetime, A = constant

ΔT = temperature difference, n = temperature difference coefficient

The representative failure modes and the temperature difference coefficient of the semiconductor devices are shown in Table 3.

Table 3 Failure modes and temperature difference coefficients

Failure modes	n	Data/article
Sliding of the Aluminum	6	An internal data of Sub-committee on Semiconductor Devices Reliability of EIAJ
Sliding of the Aluminum	7.5	TOSHIBA CORP. semiconductor reliability handbook
Passivation crack	11	An internal data of Sub-committee on Semiconductor Devices Reliability of EIAJ
Passivation crack	4.4	The assembly and the reliability of the surface mounting LSI package (Hitachi)
Thin film cracking	8.4	IRPS, 1997, p110
Interlayer dielectric cracking	5.5±0.7	IRPS, 1997, p110
Gold wire cracking	5.2	Hitachi semiconductor device reliability handbook
Gold wire cracking	5.3	The assembly and the reliability of the surface mounting LSI package (Hitachi)
Gold wire cracking 25μmΦ	4	IEICE Technical Report R85-16, 1985
Gold wire cracking 30μmΦ	7	IEICE Technical Report R85-16, 1985
Bonding peeling 50μmΦ	7	IEICE Technical Report R85-16, 1985
Fractured-intermetallic bond	4	IRPS, 1990, p252
Chip-Out bond	7	IRPS, 1990, p252
Degradation of the flip chip sealing part	2.1	An internal data of Sub-committee on Semiconductor Devices Reliability of EIAJ
Degradation of soft solder die bond sealing part	3.4	Union of Japanese Scientists and Engineers (JUSE) /Reliability and Maintainability symposium (Jun., 1991)
Package crack	5	TOSHIBA CORP. semiconductor reliability handbook

3.3 Calculation of acceleration factors

The stresses which cause failure are temperature, humidity, voltage, current density, temperature cycling and so on. These stresses promote chemical, physical and electrical phenomena which make semiconductor devices fail.

The reliability tests are performed under these accelerated stresses. The accelerated stress tests enable a decrease in the test duration which takes much more time at the operation condition. This chapter indicates the calculation of acceleration factors between the acceleration condition and the operation condition with some acceleration models.

3.3.1 Temperature acceleration factor

Temperature accelerated tests promote chemical and physical phenomena. These tests cause failures like dielectric breakdown, electromigration and so on.
In general, temperature acceleration can be calculated with the Arrhenius equation. It is as follows:

$$L = A \cdot \exp\left(\frac{Ea}{kT}\right)$$

where: A = constant,
Ea= activation energy(eV),
k = Bolzmann's constant 8.617×10^{-5}(eV/K),
T = temperature in kelvins(K)

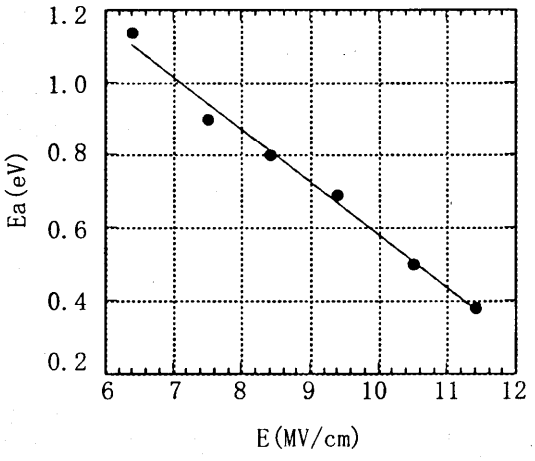
According to this equation, the temperature acceleration(αT) can be calculated between T_1 and T_2 as follows:

$$\alpha_T = \frac{L_1}{L_2} = \exp\left(\frac{Ea}{kT_1}\right) / \exp\left(\frac{Ea}{kT_2}\right)$$
$$= \exp\left(\frac{Ea}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \quad \cdots (40)$$

The representative tests of temperature acceleration are high temperature operation and high temperature storage.

Fig. 15 shows the relation between Activation energy and Electric field. This means Activation energy depends on Electric Field.

Fig. 15 Relation between Ea and Electric field[36]



3.3.2 Voltage acceleration factor

Voltage accelerated tests promote electrical and physical phenomena. These tests cause failures like dielectric breakdown of gate oxide and interlayer where it is assumed that the thickness of interlayer is the same as gate oxide. There are some voltage acceleration models. Some of them are following models:

$$L = A \cdot 10^{-\beta \cdot Eox}$$

where: A = constant
β = electric field coefficient(cm/MV)
Eox= oxide electric field(MV/cm)

$$L = A \cdot \exp(-\beta \cdot Eox)$$

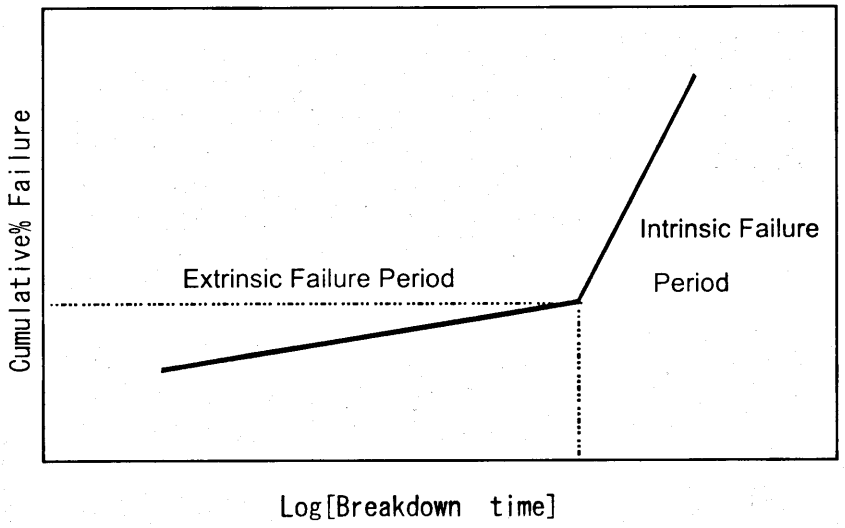
where: A = constant
β = electric field coefficient(cm/MV)
Eox= oxide electric field(MV/cm)

According to these equation, the voltage acceleration(α_E) can be calculated between E_1 and E_2 as follows:

$$\alpha_E = \frac{L_1}{L_2} = 10^{\beta \cdot (E2-E1)} \quad \cdots (41) \qquad \alpha_E = \frac{L_1}{L_2} = \exp(\beta (E_2 - E_1)) \quad \cdots (42)$$

The representative test of voltage acceleration is high temperature operation. Fig. 16 shows the TDDB characteristics. This characteristic is divided into the extrinsic and the intrinsic regions.

Fig. 16 Intrinsic failure and extrinsic failure



In general, voltage acceleration is calculated from the experimental results of TDDB test which is conducted at process developing situation. Fig. 17 and 18 show the different acceleration at the same temperature(225℃) for each region.

Fig. 17 225℃ Extrinsic t50% Vs E-field[37]

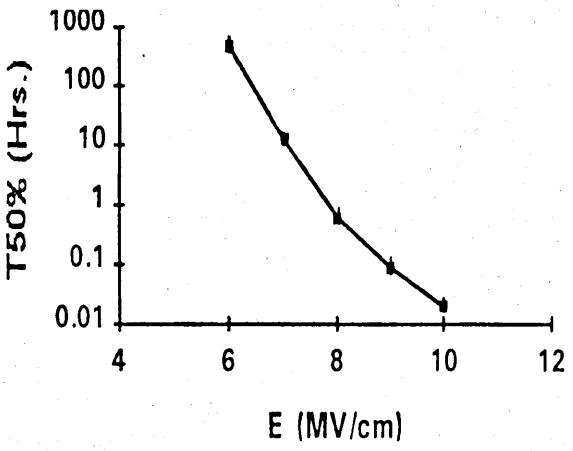
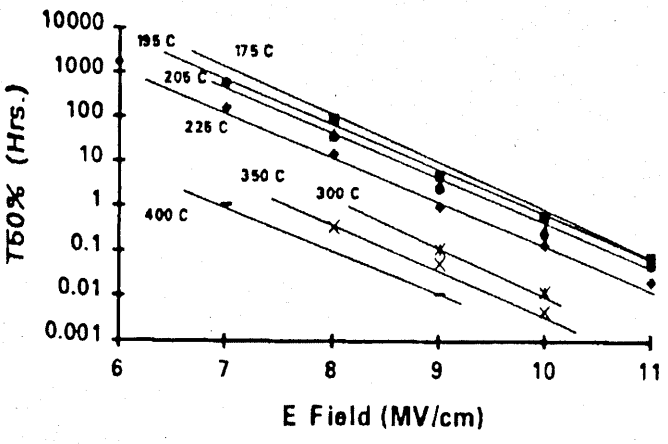


Fig. 18 Intrinsic Field Acceleration Factor[37]



The reason why the data of the intrinsic region is generally used for calculation of the acceleration is that the acceleration of the intrinsic region is lower than that of the extrinsic region.

3.3.3 Temperature cycling factor

Temperature cycling induces mechanical stress, since the composite materials have different thermal coefficients. It causes failures like package cracking, passivation cracking and so on. Temperature cycling acceleration can be calculated with the Eyring model. It is as follows:

$$L = A \cdot \Delta T^{-n}$$

where: A = constant,
ΔT = temperature cycling range,
n = temperature cycling coefficient

According to this equation, the temperature acceleration($\alpha \Delta T$) can be calculated between ΔT_1 and ΔT_2 as follows:

$$\alpha_{\Delta T} = \frac{L_1}{L_2} = \left(\frac{\Delta T_1}{\Delta T_2} \right)^{-n} = \left(\frac{\Delta T_2}{\Delta T_1} \right)^{n} \quad \cdots \quad (43)$$

3.3.4 Humidity acceleration factor

Humidity accelerated tests promote chemical and physical phenomena. They cause failures like metal corrosion and so on. There are some humidity acceleration models. One of them is as follows:

$$L = A \cdot RH^{-n}$$

where: A = constant,
RH = relative humidity,
n = humidity coefficient

According to this equation, the humidity acceleration(αH) can be calculated between RH_1 and RH_2 as follows:

$$\alpha_H = \frac{L_1}{L_2} = \left(\frac{RH_1}{RH_2} \right)^{-n} = \left(\frac{RH_2}{RH_1} \right)^{n} \quad \cdots \quad (44)$$

4. Semiconductor reliability test concept

The semiconductor device is reputed to be one of the longest-lived products in the industry. Therefore, semiconductor devices require different testing techniques from other electric components for the reliability qualification. This chapter discusses inherent reliability test (qualification) concepts for semiconductor devices.

4.1 Semiconductor device reliability test and its failure distribution

Reliability test at the new product development can be classified as the following two stages:

Process reliability test

TEG (Test Element Group) is widely used at the new process development because TEG can easily evaluate process capability.

Reliability test

This test is adopted for qualifying new product by using test vehicles which have similar gate count or die size to the specific die (product) . Sometimes the product itself is used for its qualification.

Both of the above two tests should be accelerated by using appropriate factors in order to reduce test times. These reliability tests have the objective of calculating device lifetime under actual use condition by using accelerated results.

It is noted that the correlation between accelerated tests and customer use conditions should show adequate agreement.

Specifically, semiconductor devices generally show only infant mortality and wear-out region on their bathtub curve. It means semiconductor devices do not have the region of constant failure rate region. We can not see a random failure period during reliability test, especially high temperature operation. However, it is sufficient to assure device reliability by the failure distribution of the reliability test that is performed at infant mortality and wear out region.

(1) Process reliability test

Process reliability tests have the objective of verifying the lifetime margin to the wear out of the new process technology. In addition, these tests also verify design rules.

The accelerated lifetime is defined as the time when the test vehicle shows life limit that means fatal functional failure of the TEG. The functional failures are also defined by gathering parameters data of time-dependent degradation. Gathering parameters should be defined prior to start tests from adequate perspectives. Process reliability tests generally include important items such as EM (Electro Migration), TDDB (Time Dependent Dielectric Breakdown) etc., in order to determine process specific lifetime. Apparently, process reliability test is attributed to define the wear out region $m>1$, therefore this test determines the upper limit of process inherent device lifetime.

(2) Product Reliability test

The reliability test on the semiconductor devices is attributed to predict failure rate or to assure reliability of the products that will be used in the customer field conditions. It is very important to notice the difference between reliability test and process reliability test. The reliability test is performed at infant mortality region. In addition, this test is also performed to identify wear out phenomena $1<m$ during stressing. As for semiconductor devices, wear out mode is seldom seen and it can not be acceptable in the market field (customer usage). The failures of reliability test can be classified as infant mortality, which can be plotted as $m<1$ of the Weibull plot.

The test time (1000 hours) can be assumed as equivalent of over 10 years operation under the customer fields. Ten years lifetime guarantee is quite enough for commercial applications. In case of great reliability required products, reliability test design should be performed under special considerations.

The Failure rate gradually decreases with time during reliability test because it is in the infant mortality (m<1) region. Therefore, for example, failure rate within 1000 hours is always higher than the rate that will be gathered over 1000 hours. It is obvious that excess stress time is meaningless.

4.2 Screening concept

The purpose of this section is to present the reliability screening for products. As described before, a semiconductor device failure rate is interpreted as rapidly declining with time post shipping from a manufacturer.

For MOS IC (see note1) products, most semiconductor suppliers generally set reliability criteria, which is generally described by using a failure rate at the point in time of shipment (see note 2) according to customer demands and each final component use. If MOS IC product's failure rate can not meet a criterion, a supplier usually applies a screening (burn-in) to 100 percent of the products for aging the products decline the failure rate along with bathtub curve within the reliability criteria.

Most semiconductor products usually perform the burn-in test, which have an aim to gather the failure rate distribution data on the introduction of the new fabrication processes. Burn-in test is performed with reading (test) period (e.g. test ->burn-in 8h-> test ->burn-in 16h -> test···) by using at least 1000 pcs or up to 10000 pcs of sample size. The data derived from the burn-in test are classified for each failure mechanism, and then each data is fit to a Weibull distribution to comprehend the failure rate distribution for each mechanism by drawing the Weibull plot.

The reliability criteria are described by using a failure rate at the point in time of shipment, an average failure rate during a year after shipment, or a cumulative percent failure during a year after shipment as described note2. In all cases it is described by a value under actual-use conditions. Therefore it is necessary to comprehend acceleration of the burn-in in order to compare the failure distribution derived from the burn-in test data to the reliability criteria. Since acceleration of the burn-in test depends on each failure mechanism, the failures of the burn-in test are analyzed and classified for each failure mechanism. The most frequent failure modes at the burn-in are gate oxide leakage failure and functional failure induced by metal particles.

Acceleration model of metal particle failure and acceleration factor of metal particle failure are treated as equivalent (see Fig. 19) to that of gate oxide leakage failure. Therefore acceleration model and acceleration factor of the burn-in are used for time-dependent breakdown (TDDB) data, which are obtained at new fabrication process development. In case of using TDDB data as the burn-in acceleration, there are two cases. One is using TDDB data derived from shape parameter $m > 1$ region. The other is using TDDB data derived from shape parameter $m < 1$ region. Shape parameter m derived from the burn-in test data by drawing Weibull plot provides $1 < m$ as a normal case.

Therefore it is more logical to use TDDB data derived from $m < 1$ region than to use TDDB data derived from $m > 1$ region. However TDDB data derived from $m > 1$ region is generally used as acceleration of the burn-in for reducing consumer's risk. It is possible to overestimate the failure rate higher, since acceleration derived from m>1 region TDDB data is lower than that from $m < 1$ region TDDB data.

The burn-in test is usually only performed for new fabrication process development. It is unnecessary to perform it for each new product development, since a new product's failure rate can be estimated by normalizing the chip size, the number of transistors, or the density of transistors.

Each product's burn-in condition is fixed by using previously discussed information

that are the reliability objective, acceleration of the burn-in, and the failure rate distribution derived from the burn-in data. Most semiconductor suppliers perform checking cumulative percent failure occurred in the screening (burn-in) for each specific product's lot after fixing the burn-in conditions (duration of burn-in is from several hours to several 10hours), because prevent outflow of an abnormal lot having a failure rate higher than the reliability objective.

When we predict product reliability, in the past we have used a method that is estimating the average failure rate by using high temperature life test that is long term (e.g. 1000hours) and small sample size (e.g. from 15pcs to 76pcs). However even if it is long term like 1000hours, the point of 1000hours is on the failure distribution (bathtub curve) derived from the burn-in test. Therefore it is effective not only to estimate the average failure rate by using long terms like 1000hours, but also the failure rate distribution by using the burn-in test data.

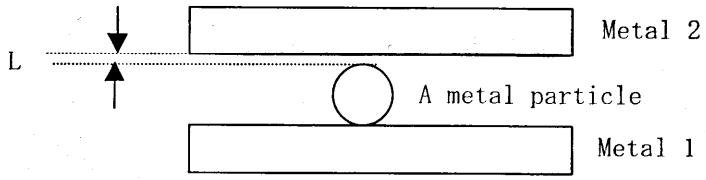
(Note1)

For bipolar IC and discrete components, the average failure rate is generally estimated by using long term's high temperature life test without the burn-in data. For even MOS IC the burn-in test isn't performed according to circumstances.

(Note2)

It is possible to set a reliability objective by using an average during specific terms (e.g. one year) after shipment, or a cumulative percent failure during specific terms (e.g. one year) after shipment without using a failure rate at the point of shipment. It is possible to set the product's burn-in condition according to each reliability criteria.

Fig. 19 A functional failure induced by a metal particle.



Initially the insulating L between Metal 2 and a metal particle provides insulation, and then the insulator is broken by thermal and electric field energy during the burn-in. Since L is unknown, acceleration of burn-in is derived from TDDB data assuming that L is equal to gate oxide thickness.

4.3 Recommended operating range and reliability guarantee

Recommended operating range is established on each semiconductor device, but it should be noted that there is a close relation between reliability and operating temperature/voltage.

In recent years, smallsizing of electronic equipment which uses semiconductor devices brings about heat problems because thermal design of the system becomes very difficult.

For example, thermal stress coefficients are demonstrated as the Table 4 with activation energy of 0.5, 0.6 and 0.7 eV as a function of average temperature 25 to 55 degrees at customer use. The coefficients are normalized at 25degrees as a unity. This table is calculating at the assumption that the recommended operating range is -40 to 85 degrees.

Table 4 The activation energy vs the average temperature on customer using
$\alpha_T = \exp\left(\frac{Ea}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$, Ea=0.5eV, 0.6eV, 0.7eV

	Average 25℃	Average 35℃	Average 45℃	Average 55℃
Ea=0.5eV	1.0	1.9	3.4	5.9
Ea=0.6eV	1.0	2.1	4.3	8.5
Ea=0.7eV	1.0	2.4	5.6	12.1

As shown in Table 4, thermal acceleration factor varies remarkably on operating temperature.

Consequently, it should be noted that device life-time may drastically reduce even though it is used within recommended operating conditions in case of upper limit temperature environment.

It is very important to notice on thermal design implementation with an appropriate derating, in consideration of package and circuit board thermal resistance.

As is the case of the above, the following serves as an example of power supply voltage. The recommended power supply voltage of 2.7 V to 3.6 V, voltage 3 V can be assumed as normalized of unity. Next, Table-5 demonstrates voltage acceleration factor of β of 3.0, 3.5, 4.0, which contrast to supply voltage of 3.0 V to 3.6 V.

Table 5 The electric field coefficient vs the average voltage on customer using
$\alpha_E = \exp(\beta(E_2 - E_1))$, β =3.0, 3.5, 4.0
E (MV/cm) : Electric field strength is calculated from supply voltage and gate oxide thickness.

	Average 3.0 V	Average 3.2 V	Average 3.4 V	Average 3.6 V
β=3.0	1.0	1.8	3.3	6.1
β=3.5	1.0	2.0	4.1	8.2
β=4.0	1.0	2.2	5.0	11.0

Table 5 proves clearly that electrical field stress is strongly affected by β and operation voltage assumption.

It is obvious that reliability assurance is need to keep lower voltage and appropriate temperature even though they are within recommended operating conditions.

For special applications, such as high temp, higher voltage continuous operation should be carefully reliability designed for each custom case.

4.4 The customer operating environment

There are several requirements concerning the operating environment of a device. This section shows a guideline of an operating environment.

The typical ambient temperature is generally between 25 degrees and 55 degrees. If a customer has a special requirement, it is necessary to negotiate a specification individually.

The ambient temperature heats up when operating a device, then the operating ambient temperature plus the heat-up temperature produces the above-mentioned temperature.

The heat-up temperature depends on a the thermal resistance of a package and the electric power dissipation.

The heat-up temperature of a device is :

$$\Delta T = \theta \times Pc \quad \cdots (45)$$

where

ΔT (℃) = heat-up temperature
θ (℃/W) = thermal resistance of a package
Pc (W) = electric power of a device

4.5 Life prediction

The following shows a predictable acceleration rate with a practical condition and a test condition by the above-mentioned failure models.

4.5.1 Temperature & Voltage accelerated life prediction

In case of the temperature & voltage acceleration model, an acceleration rate calculated using 3.3.1(40) & 3.3.2(42) equation is:

$$\text{acceleration rate } a = \alpha_T \times \alpha_E = \exp\left(\frac{Ea}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \times \exp(\beta(E_2 - E_1))$$

$$= \exp\left(\frac{0.5}{8.617\times10^{-5}}\left(\frac{1}{(55+273)} - \frac{1}{(125+273)}\right)\right) \times \exp(3.5(4.2-3.3))$$

$$\fallingdotseq 22.45 \times 23.34$$

$$\fallingdotseq 524.0$$

HTOL1000hours $\fallingdotseq 5.240\times10^5$hours (60years)

where

practical temperature = Ave. 55 ℃
practical electric field = Ave. 3.3MV/cm
test temperature = 125 ℃
test electric field = 4.2MV/cm
k = Bolzmann's constant: 8.617×10^{-5}eV/K

4.5.2 Temperature cycling accelerated life prediction

In case of the temperature cycling acceleration model, an acceleration rate calculated using 3.3.3(43) equation is:

$$\text{acceleration rate } \alpha_{\Delta T} = \left(\frac{\Delta T_2}{\Delta T_1}\right)^n = \left(\frac{\Delta 215}{\Delta 50}\right)^4 \fallingdotseq 341.9$$

T/C(-65℃～150℃) 300 cycles ≒ 1.0257×10^5 cycles
Ave. 5 cycles/day → 2.0514×10^4days (56 years)

where

practical ΔT= Ave. $\Delta 50$℃
test range ΔT=150℃ -(-65℃) = $\Delta 215$℃

4.5.3 Humidity accelerated life prediction

(1) Water vapor pressure acceleration model

In case of the water vapor pressure acceleration model, an acceleration rate calculated using 3.2.3(21) equation is:

$$\text{acceleration rate } \alpha_P = \left(\frac{P_2}{P_1}\right)^n = \left(\frac{4.91 \times 10^4}{0.25 \times 10^4}\right)^2 \fallingdotseq 385.7$$

85℃85%RH 1000hours ≒ 3.857×10^5hours (44 years)

where

practical water vapor pressure = 0.25×10^4Pa (30℃, 60%RH)
test water vapor pressure = 4.91×10^4Pa (85℃, 85%RH)

Note:

It is needed to be careful that the below case makes a mistake on water vapor pressure acceleration model.

For example, 40℃, 90%RH → water vapor pressure = 0.66×10^4Pa
80℃, 20%RH → water vapor pressure = 1.16×10^4Pa

In this case on water vapor pressure : 0.66×10^4Pa(40℃, 90%RH) < 1.16×10^4Pa(85℃, 20%RH)
But actually, 85℃, 20%RH is dry condition.
So in this case, 40℃, 90%RH condition is higher acceleration humidity test than 85℃, 20% RH condition.

(2) Relative humidity acceleration model

In case of the relative humidity acceleration model, an acceleration rate calculated using 3.3.4(44) & 3.3.1 (40) equation is:

$$\text{acceleration rate } a = \alpha_H \times \alpha_T = \left(\frac{RH_2}{RH_1}\right)^n \times \exp\left(\frac{Ea}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

$$= \left(\frac{85}{60}\right)^4 \times \exp\left(\frac{0.8}{8.617\times10^{-5}}\left(\frac{1}{(30+273)} - \frac{1}{(85+273)}\right)\right)$$

$$\fallingdotseq 4.03 \times 110.8$$

$$\fallingdotseq 446.5$$

85℃85%RH 1000hours $\fallingdotseq 4.465\times10^5$hours (51 years)

where

practical temperature & relative humidity = 30℃, 60%RH
test temperature & relative humidity = 85℃, 85%RH
k = Bolzmann's constant: 8.617×10^{-5}eV/K

Fig. 20 shows a relationship of a relative humidity to a temperature with a vapor pressure at 30 degrees, 60%RH.
A temperature increases, then a relative humidity decreases.
It shows the effect of a relative humidity decreases at high temperatures.

So correct life perdiction on humidity environment is possible by using low temperature for field estimation.

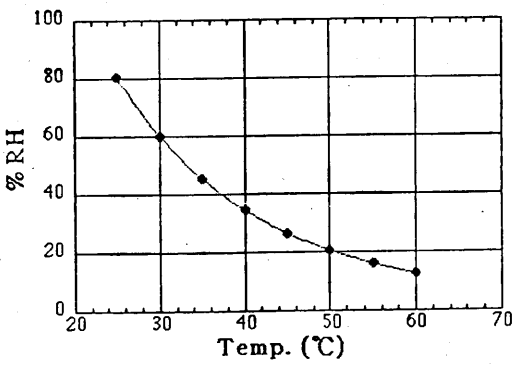
Accordingly, it is understood that 30℃ practical temperature setting is suitable.

As the above, it is possible to predict the life with the acceleration model in short time.

And, it is understood that present 1000 hours test is the excess test to exceed target reliability.

It is best to predict the reliability over the required life based on the use condition as nearly as possible with the same acceleration model.

Fig. 20 RH vs Temp.



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Explanation

1. Purpose of establishment

This technical report presents a way of thinking for semiconductor devices reliability that is not extensively discussed in current textbooks. This report is intended to assist semiconductor reliability evaluation to assure proper usage for the application.

Recently, reliability test has required "excess" conditions by users or customers. We can execute more efficient reliability test by using adequate acceleration and reasonable test time / test stress based on understanding semiconductor inherent reliability characteristics and field conditions.

Writing of this technical report was carried out by the engineer(member of EIAJ Sub-committee on Semiconductor Devices Reliability) who engaged in the reliability business in semiconductor manufacturer for many years, and the report has been based on common-sense industry standards on the reliability of semiconductors.

This report presents a different perspective from current references, and it is thought that it will be very useful for both the semiconductor reliability engineer and the customer. We hope that this report will become useful for many engineers who have interest in reliability field.

2. Evolution of establishment

According to the purpose mentioned above, Sub-committee on Semiconductor Devices Reliability was in charge of the deliberation since June, 1998. We held a meeting every 2 months, and investigated society and world trends widely, based on the latest reliability technology trend. It was published as a guideline in May, 2000.

3. Major contents

First of all, reliability test time for conventional test methods and the technology grounds of the number of stress cycles became an issue. A 1000 hours test such as high temperature operation test and temperature humidity bias test are the examples, the test time can be drastically reduced from the conventional test times if reasonable acceleration factor can be predicted from failure mechanisms. In this guideline, the concrete life calculation method is made clear by "4.5 Life prediction".

And, we discussed that the acceleration failure mechanisms can be roughly classified into two categories: the intrinsic mode and the extrinsic mode. The intrinsic mode is the wear-out failure mode, the inherent characteristic of semiconductor devices which is based on design rules. The extrinsic mode is interpreted in terms of process induced defects (ex. particle). These extrinsic factors restrict the reliability of the inherent characteristic. It should be concluded, from what has been mentioned as two modes of failure, reliability test consuming time can be reduced markedly. Based on this way of thinking, popular "Weibull distribution and bathtub curve" were described in this guideline and it was described an illustration about "the reason of failure tendency in each failure period" from a point of view that was different from a commentary book as before. And, "acceleration life test" was mentioned about the acceleration model and acceleration factor, their tables were quoted from society paper.

Concrete calculation methods are described in this guideline as above, and it is considered that many people including semiconductor buyers can utilize it easily.

4. Committee members

This technical report was discussed mainly by "Sub-committee on Semiconductor Devices Reliability" of the Technical Standardization Committee on Semiconductor Devices / Semiconductor Devices Reliability Group.
Below are listed the members of deliberation of this technical report.

< Technical Standardization Committee on Semiconductor Devices / Semiconductor Devices Reliability Group >

Chairman:	Kazutoshi Miyamoto	Mitsubishi Electric Corp.

< Sub-committee on Semiconductor Devices Reliability>

Chief:	Tetsuaki Wada	Matsushita Electronics Corp.
Vicechief:	Masaki Tanaka	Hitachi, Ltd.
Member:	Hiroo Kozuka / Hideaki Yoshida	Oki Electric Industry Co.,Ltd.
	Osamu Nakayama	Kawasaki Steel Corp.
	Hisahumi Kumagai	Sanken Electric Co.,Ltd.
	Takahiro Asano / Toru Kato	Sanyo Electric Co.,Ltd.
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	Hiroshi Matsushima	Matsushita Electronics Corp.
	Junichi Mitsuhashi	Mitsubishi Electric Corp.
	Seiji Kusuda	Mitsumi Electric Co.,Ltd.
	Koki Ohara	Ricoh Co.,Ltd.
	Takahiro Ito	Rohm Co.,Ltd.