JEITA

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Guide for the Reliability Specification of FLASH Memory

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Guide for the Reliability Specification of FLASH Memory

1. Scope

This guide applies to the reliability specifications and descriptions of flash memory.

2. Overview

Flash memory is based on the fundamental mechanism of an electron that passes through a silicon oxide layer to rewrite the data. The device is subject to dielectric deterioration due to repetitive program/erase cycles and eventually fails to work. This deterioration of the silicon oxide layer affects the quality of flash data and may degrade the data retention with accumulated program/erase cycles, even before the onset of endurance wear-out.

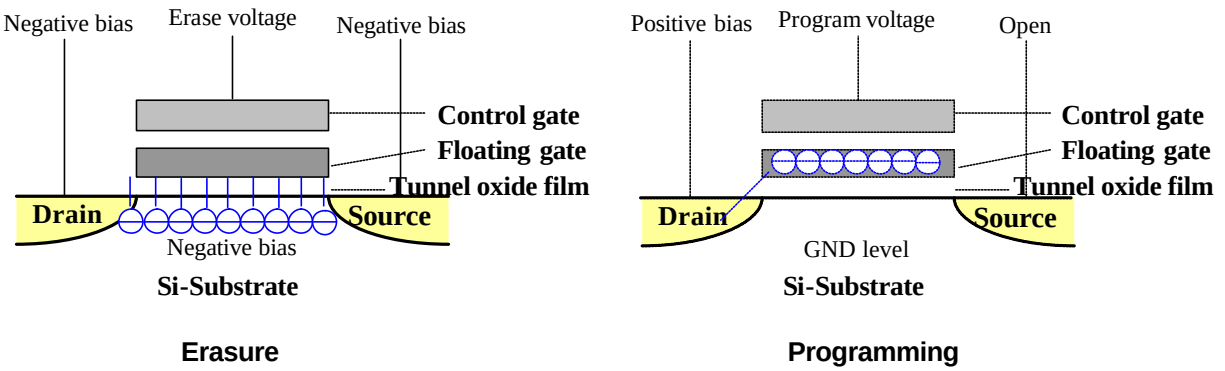
The purpose of this guide is to provide a consistent framework for reliability specifications for flash memory, and to propose the assurance models indicating the relationship between the specification of endurance cycles and those of data retention and disturbs.

3. Reliability concerns

This section describes causes of reliability deterioration of the device. Major reliability concerns for flash memory are the endurance, data retention and disturbs. Any of these failure mechanisms is due to the degradation of oxide layer damaged during the transfer of electrons on and from the floating gate, i.e., tunneling through dielectric layers.

3.1 Programming and erasure mechanisms of flash memory

Figure 1 shows typical biasing conditions of DINIR flash memory during programming and erasure. This guideline explains DINOR type FLASH to an example as a general example. Even if the architecture differs, the fundamental reliability subject is common. Both programming and erasure operation cause electrons to pass through the gate oxide, degrading the quality of oxide layer in proportion to the number of program/erase cycles. Rewriting the data damages the oxide layer and degrades the insulation property between floating gate and silicon substrate, which leads to the reliability failures such as data retention wear-out and enhancing disturbs.

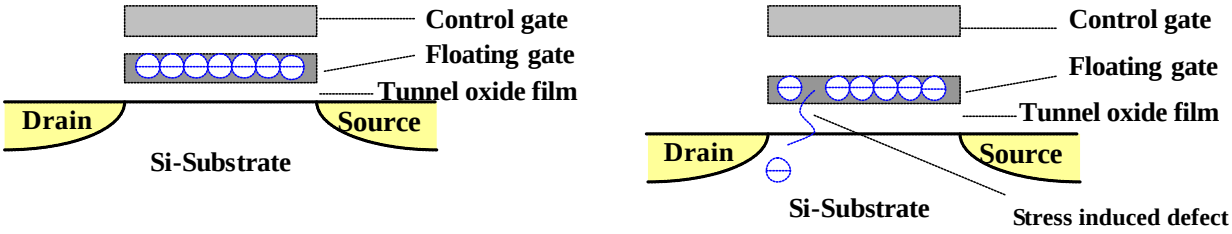


Erasure **Programming**

Figure 1 Example of typical biasing conditions during programming and erasure

3.2 Data retention

Figure 2 illustrates typical data retention conditions and the failure mechanisms. The charge stored on the floating gate changes the threshold voltage (Vt) and sets the memory transistor to a logical "1" or "0". The charge intrinsically does not leak out through the insulation surrounding the floating gate. Repetitive program/erase cycles, however, cause random oxide damage and degrade the insulation property of the layer as described in section **3.1**., allowing charge loss at the floating gate, and eventually leading to the data retention failure.



Data retention condition **Data retention failure**

Figure 2 Data retention failure mechanism

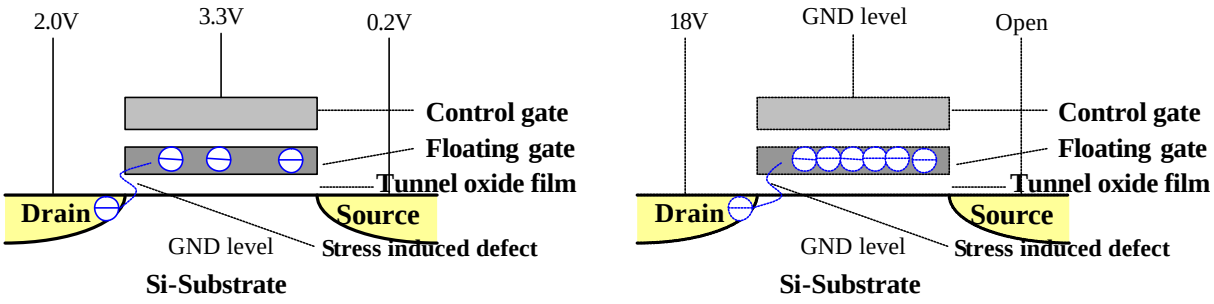
3.3 Disturbs

Schematic illustrations of typical disturb mechanisms are shown in **Figure 3**.

There are two primary disturbs;

- Read disturb, which occurs during read, and
- Program disturb, which occurs during programming.

A disturb is the inadvertent change of the threshold voltage at a memory cell, which results from the transfer f electrons by potentials applied to other cell during read or write operations. The number of data rewrites affects the probability of disturb errors as well as that of data retention errors. Since the probability of the disturbing accesses during program/erase operations depends on the memory architectures, appropriate duty factor, the percentage ratio of the accessed period of the memory cell to the non-accessed period, can be taken into the consideration of failure rates. The voltage conditions which induce disturbs vary by memory architectures, and the values and structures in **Figure 3** should be regarded as a reference.



An example of read disturb **An example of program disturb**

Figure 3 Example of Schematic illustration of disturb mechanisms.

4. Reliability testing methodology for flash memory

This section gives overviews of the testing methodology of endurance, data retention and disturbs which are general qualification requirements for flash memory. The reliability datasheet contains key parameters of the test conditions, such as test patterns, power supply voltages, and ambient temperatures. The reliability test results listed below will also be described in the datasheet:

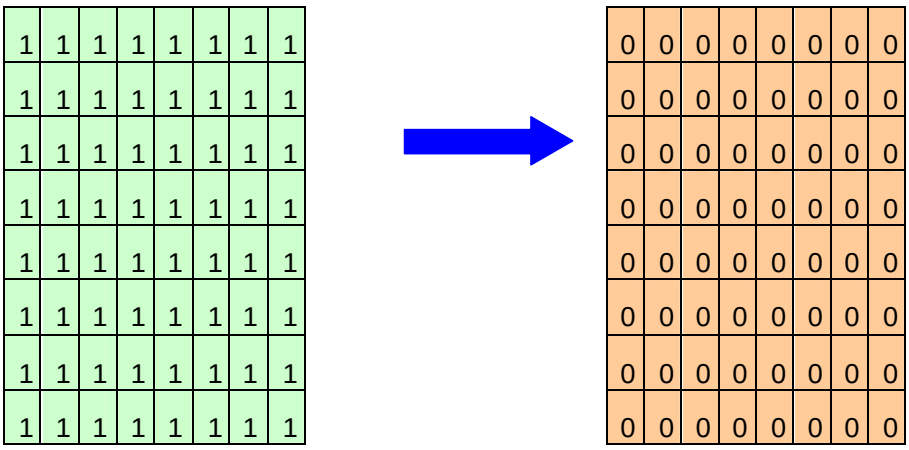
- Endurance test: the number of specified program/erase cycles, cumulative failure rate and specified temperature range
- Data retention bake stress: specified data retention duration, cumulative failure rate and specified temperature range
- Disturb: a number of the disturbing accesses, cumulative failure rate and specified temperature range

A high correlation of the number of endurance cycles with data retention and disturbs suggests the qualification in the manner of combined test conditions.

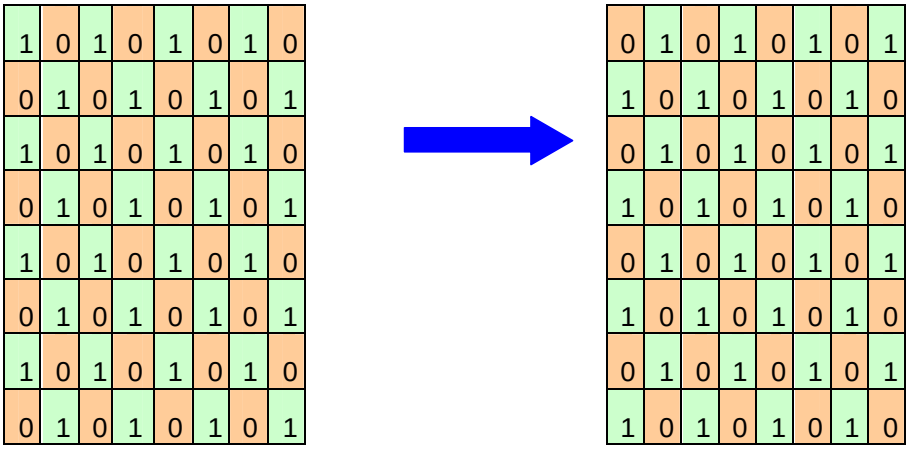
4.1 Endurance

Endurance test is intended to confirm the reliability of flash memory devices which are subjected to repetitive program/erase cycles. In general, the program/erase test cycles extend up to the specified number of endurance cycles. Statistical prediction is also valid in some cases, such as extrapolating the endurance test results of smaller-scale flash memories to the endurance performance of larger-scale memories.

The data in each memory cells must be cycled continuously from “1” to “0” to “1” to “0” during the test, where typical data patterns include the all “0” and all “1” patterns, and the checkerboard pattern.



Galloping “zeros” and “ones”



Flip-flopping checkerboard pattern

Figure 4 Examples of data patterns at endurance test

4.2 Data retention bake stress

The purpose of this test is to define the non-volatility of the data. Samples are generally program/erase cycled as preconditioning prior to going through the extended data retention bake. Pretreatment conditions will be determined in compliance with the concept of the supplier’s reliability test method. Multiple conditions of the program/erase cycles may be required to validate the reliability assurance concept where the specified retention duration is a function of the endurance cycle count.

Relevant data retention bake temperature will be in the range of the field temperature up to 250 deg C, depending on the degrading mechanisms identified.

The endurance-retention assurance model, referring to the **Figure 10** (**Example 4**) in section **8.2**, and its testing methodology are described below as an example.

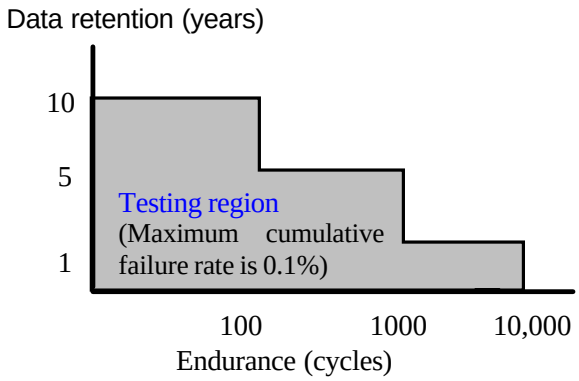


Figure 5 Endurance-retention testing model

Reliability test region on condition for this case is:

(1) Retention specification is 10 years for 1-100 program/erase cycles.

(2) Retention specification is five years for 101-1,000 program/erase cycles.

(3) Retention specification is one year for 1,001-10,000 program/erase cycles.

(1) Test condition #1	Program/erase: 1-100 cycles	Data retention bake at 150 deg C: 2000 hrs
(2) Test condition #2	Program/erase: 101-1,000 cycles	Data retention bake at 150 deg C: 1000 hrs
(3) Test condition #3	Program/erase: 1,001-10,000 cycles	Data retention bake at 150 deg C: 168 hrs

Figure 6 Test concept of data retention bake as a function of endurance

Figure 6 show the corresponding test conditions of program/erase cycles and data retention bake to verify the endurance-retention testing model as described in **Figure 5**. Test conditions of data retention bake is accelerated by using a higher temperature conditions. The apparent activation energy varies from 0.3 eV to 1.5 eV, depending on the failure mechanism that the semiconductor manufacturer identifies.

Given that the apparent activation energy of the failure mechanism is 0.5 eV and that field data retention temperature is 40 deg C, passing the Test condition #1 in **Figure 6** indicates that the projected lifetime is far beyond 10 years in the use condition.

4.3 Read disturb

The purpose of this test is to characterize the disturbs on both the selected and deselected cells in the course of read operations. The test conditions are determined based on the knowledge of the user's

environment and the system characteristics, which affect the probability of the disturb errors. Examining this disturb is generally included in the electrical tests at high or low temperature environments. Samples are subjected to the specified number of program/erase cycles as preconditioning prior to the extended read disturb test, in the same manner as the pretreatment of the data retention bake.

Although suppliers can take duty factor into consideration of read disturb probability, these premises for reliability specification will be stated explicitly in the datasheet.

4.4 Program Disturb

The purpose of this test is to verify whether the contents in deselected memory cells are changed unintentionally, while programming another location. Test conditions vary depending on the programming algorithm which determines the probability of program disturbs in flash memory. Examining the program disturb is generally included in a part of the endurance test. If the extended program/erase cycles enhance the program disturbs, test conditions are designed accordingly.

5. Definition of failure

Even single bit error is defined as a failure in terms of the reliability of the memory device, and it is reflected in the calculation of the cumulative failure rate and/or failure rate.

When memory has redundancy against bit errors, such as a built-in function of error checking and correction (ECC), suppliers can declare the value of failure rate which is compensated by the redundancy benefit. The device of using external ECC is a present practice, original failure rate are preferably shown in the reliability data sheet.

6. Determining application conditions

Typical application conditions such as the frequency of data rewrites and storage duration are determined to specify the reliability of flash memory. Assumption of the use environmental temperature is also important to check the retention without regard to programming frequency.

6.1 Use environmental temperature

Assumption of use environmental temperature depends on the applications per semiconductor suppliers. In general, environmental temperature ranges from room temperature to 55 deg C.

6.2 Frequency of data rewrites

Applications of flash memory are categorized according to the requirements in use conditions, such as the memory for storing program codes and for data storage. The memory for storing program codes will be configured limited times in the beginning of the useful lifetime, and it is required to retain the data for a long time. While, the memory for data storage will be programmed frequently with a limited retention duration between data rewrites. The average storage time tends to be shorter in recent years. Applications scarcely demand both high endurance and high retention time, suggesting that it is practical to specify the relevant retention duration for the endurance cycle count.

6.2.1 For the application which requires initial programming and subsequent long-term data retention;

At the beginning of the useful life, flash memory is expected to face limited times of programming followed by a few data rewrites, but it must put up with long-term retention.

Example: This application includes storing program code in multi-chip-package (MCP).

(a) Data rewrites frequency: Programming and rewrites happen mostly in the beginning of the useful lifetime (10 years in general).

Example: Flash memory with specifications of a 100-cycle maximum of endurance and a 10-year maximum of retention is regarded as programming 100 times in the first month of useful life.

(b) Data retention duration: Data retention duration is regarded as the planned time of use after initial programming.

Example: Data retention duration is regarded as 10 years in this model.

6.2.2 For the application which requires constant data rewrites;

Flash memory is programmed constantly throughout its useful life, where the data retention duration is considered an average programming/erase cycle time.

Example: This application includes image storages for digital steel camera, USB memories, and an optional feature of automotive that memorizes data at every on/off of ignition switch.

(a) Data rewrites frequency: Program/erase occurs evenly over useful lifetime (10 years in general).

Example: Flash memory with the specification of a 10,000-cycle maximum endurance and a 10-year maximum retention is programmed 10,000 times in 10 years.

(b) Data retention duration: Average data retention duration is determined as the averaged program/erase cycle time.

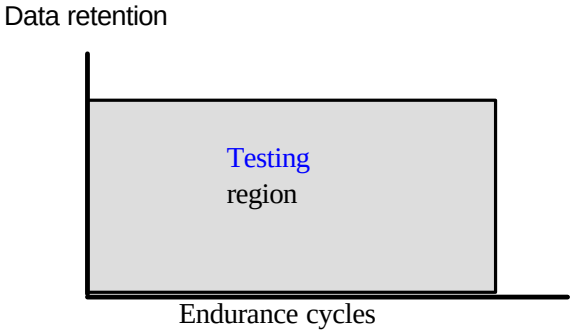
Example: Specifications of 10 years of data retention and 10,000 cycles of endurance give 8.8 hours or more of averaged data retention duration in this model.

7. Reliability description

This section describes reliability testing concepts for endurance and retention. The high correlation between the number of endurance cycles and data retention requires the reliability description in the manner of combined specifications. Even though there are several types of endurance-retention testing models, this guide is not intended to specify the models. Any model is applicable as far as reliability testing concept is clear.

7.1 Retention specification after the maximum specified number of programming cycles

This model is suitable for the flash memory for storing program codes which are programmed limited times in the beginning of the useful life, as is described in section **7.2.1**.

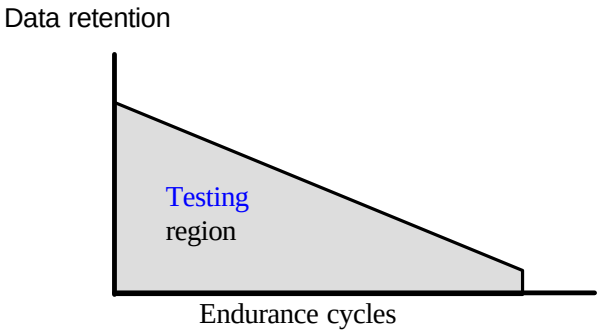


Example 1 :
Reliability specification is a 100-cycle maximum of endurance followed by a 10-year maximum of retention.
Cumulative failure rate: 0.1% maximum

Figure 7 Endurance-retention testing model (Example 1)

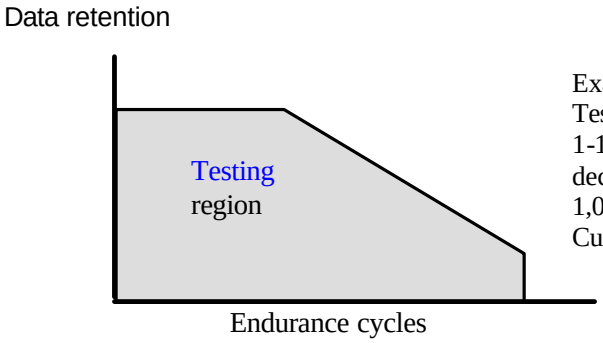
7.2 Retention specification as a function of the number of endurance cycles

This model is suitable for the flash memory used in data storage applications where programming is frequent, as is described in section **7.2.2**.



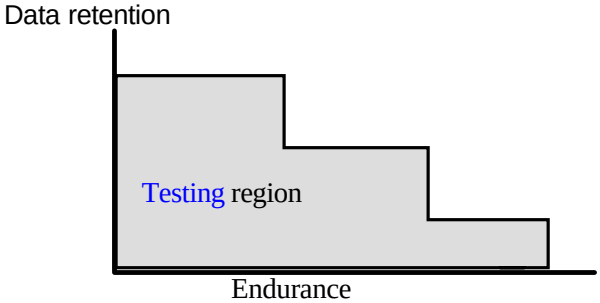
Example 2:
Specified data retention duration declines proportionally with the endurance cycle count.
Endurance testing: 10,000 cycles maximum
Retention specification for the first data write: 10 years maximum
Cumulative failure rate: 0.1% maximum

Figure 8 Endurance-retention testing model (Example 2)



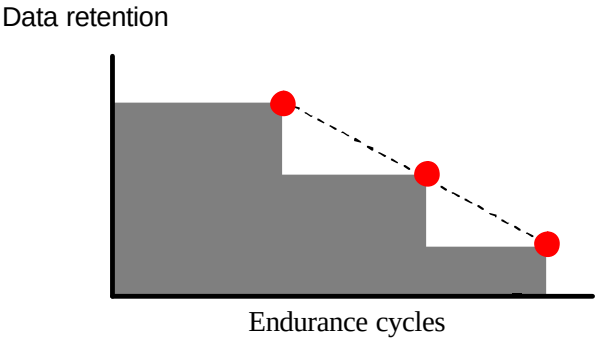
Example 3:
Testing region covers a 10-year data retention for 1-1,000 data rewrites, followed by the proportional declines to the endurance cycle count in the range of 1,001-10,000 cycles.
Cumulative failure rate: 0.1% maximum

Figure 9 Endurance-retention testing model (Example 3)



Example 4:
Data retention specification is 10 years for 1-100 endurance cycles, five years for 101-1,000 cycles, one year for 1,001-10,000 cycles.
Cumulative failure rate: 0.1% maximum

Figure 10 Endurance-retention testing model (Example 4)



Example 5:
The chart shows the specified data points, not the testing region.

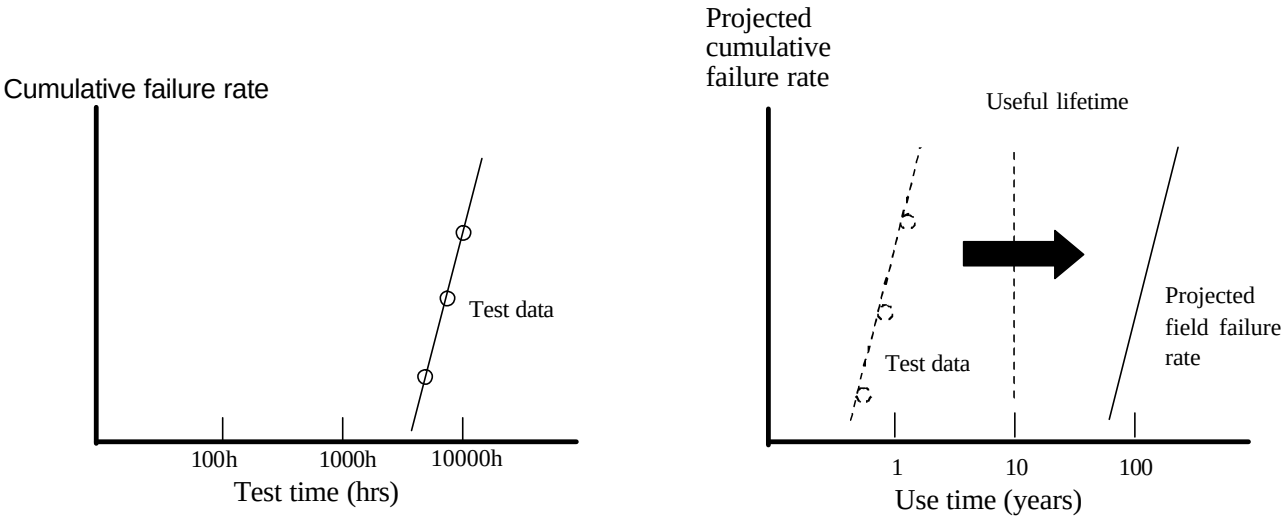
Figure 11 Endurance-retention testing model (Example 5)

8. Prediction of the device reliability

When reliability tests are carried out at increased levels of stress, such as high temperature retention bake stress, reliability datasheet will show the data projected by using acceleration factors or statistical methods. Two cases of reliability predictions are described below as examples.

8.1 Estimating the field lifetime from the accelerated test results

An example shown below implies that the products are free from the wear-out failures for the planned time of use at application conditions.



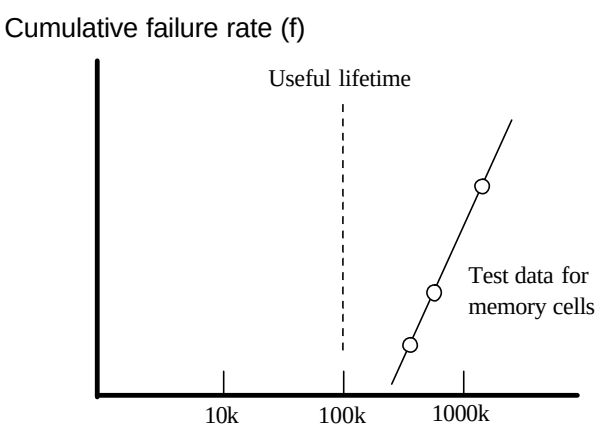
Accelerated retention test results at higher temperature **Projected failure rate at use temperature**

Fig. 12 Estimating the field lifetime from the accelerated test results

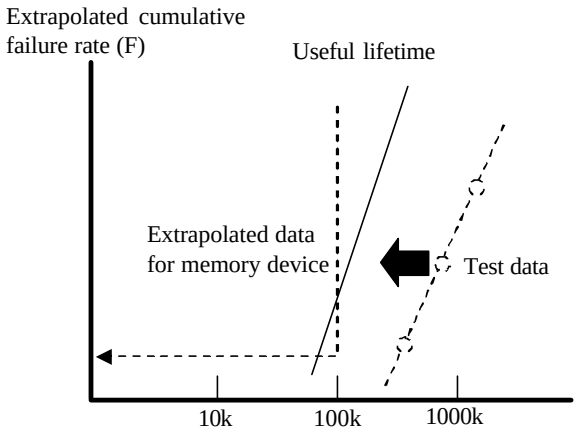
8.2 Extrapolating from the measurements of memory cells to the device endurance

Once failure rate (f) is found from measurement of single memory cell in the array, the total failure rate (F) of the flash memory device which has (n) bits of cell is calculated from the expression:

$$F=1-(1-f)n$$



Endurance test results of memory cell



Cumulative failure rate of memory device extrapolated by statistical method

Fig. 13 Extrapolating from the measurements of memory cells to the device endurance

9. How to achieve higher endurance

Data storage system with flash memory will be designed more reliable by applying advanced programming algorithm for the device. For example, when small segments of the memory device are programmed frequently, the useful lifetime can be lengthened by programming the segments of the memory device segment-by-segment until fully occupied and then by erasing the whole memory cell. **Figure 14** shows the example of repetitive program/erase cycles at the fixed location of segments, where the useful lifetime of a device is determined by the life of this segment. **Figure 15** shows the segment-by-segment programming. All memory contents will be erased after all segments are fully programmed, and another cycle will start. The useful lifetime of the device in this sequence is longer than that shown in **Figure 14**.

Also, designing the system with external ECC will eliminate the single bit error of flash memory, creating more reliable system.

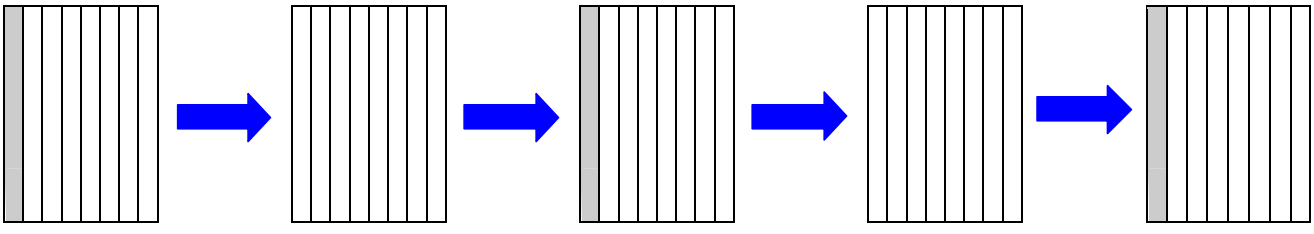


Figure 14 Repetitive program/erase cycles at the fixed location of segments

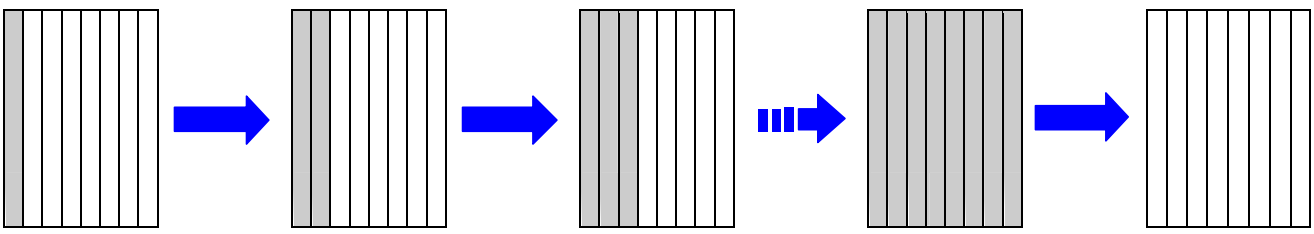
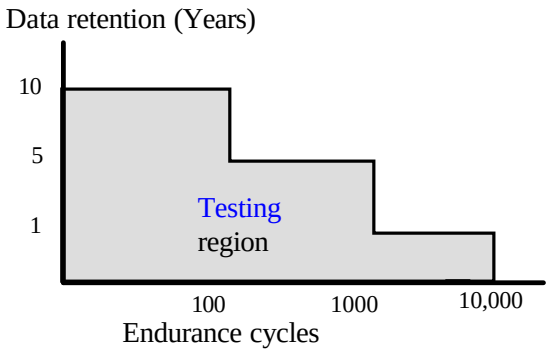


Figure 15 Programming segment-by-segment many times until fully programmed before erasure

10. Example of a reliability datasheet

The below table is a summary of the major concerns which are discussed in this guide. It does not include all necessary information, but shows an image of the reliability description.

<table>
<tr><td>Memory size</td><td>4Mb</td><td rowspan="6">Endurance-retention assurance model
 
</td></tr>
<tr><td>Memory configuration</td><td>128Mb×8bit</td></tr>
<tr><td>Data retention temperature</td><td>40 deg C</td></tr>
<tr><td>Temperature range at program/erase operation</td><td>-20 deg C to 70 deg C</td></tr>
<tr><td>Endurance assurance</td><td>10,000 cycles Maximum</td></tr>
<tr><td>Data retention duration</td><td>10 years Maximum</td></tr>
<tr><td>Reliability specifications</td><td colspan="2">Reliability assurance region on condition that maximum tolerable cumulative failure rate is 0.1% is;
- Retention specification is 10 years for 1-100 program/erase cycles.
- Retention specification is five years for 101-1,000 program/erase cycles.
- Retention specification is one year for 1,001-10,000 program/erase cycles.
Assurance duration extends to 10 years maximum.</td></tr>
<tr><td>Necessity for redundancy design (ECC, etc)</td><td colspan="2">No need.</td></tr>
<tr><td>Statistical inference</td><td colspan="2">Yes, data retention life is estimated from the high temperature-accelerated test.</td></tr>
<tr><td>etc.</td><td colspan="2">etc.</td></tr>
<tr><td></td><td colspan="2"></td></tr>
</table>

Explanatory notes

1. Background of establishment

Flash memory must satisfy two critical reliability requirements that are program/erase cycles and data retention. These requirements are incompatible; increasing number of program/erase cycles results in the deterioration of the data retention duration.

Many flash memories that are available in a market do not clearly indicate the relation between the number of program/erase cycles and the data retention, which has made users misunderstand as if the device could achieve the maximum data retention duration at the maximum number of program/erase cycles. The targeted reliability requirements have also been ambiguous.

Such situation has required the establishment of the guide that reveals the remarks and concerns from the viewpoint of reliability and that provides suppliers with the common assurance policy for the reliability specifications. This guide is aimed at clarifying the way reliability specification is to be described for flash memory and enabling users to make a fair comparison of the reliability data that are provided by different suppliers.

The deliberation started to create this guide in Apr. 2002 in the Subcommittee on Semiconductor Devices Reliability, Group on Semiconductor Devices Reliability, Technical Standardization Committee on Semiconductor Devices. After having deliberations based on the data such as survey results conducted among the flash memory manufacturers, and also having made efforts to harmonize with the policies of **JEDEC** during the joint meetings with **JEDEC JC14** held in the period of Sep. 2002 to Oct. 2005, the Subcommittee completed the final draft in Oct. 2005, and then it was established with the approval of the Group on Semiconductor Devices Reliability.

2. History of deliberations

The Subcommittee summarized the deliberation results as the guide for the reliability specification of the flash memory in this technical report in response to the requirements below. The background in this explanatory notes stated that flash memory was expected to satisfy two critical reliability requirements that are program/erase cycles and data retention. However, it has not been clearly disclosed that the data retention duration correlates with the number of program/erase cycles. Furthermore, it has not been clear what failure rates were the criteria of the assured lifetime in terms of the program/erase cycles or data retention duration and which failure modes were considered to be inclusive in the failure rates, it was, therefore, difficult to make a fair comparison of the reliability data provided by different suppliers.

This guide has concisely summarized the requirements to make a fair reliability comparison of various flash memories under the same conditions, and the reliability concerns that are intrinsic to flash memory. Since reliability test methodologies in each suppliers have been established based on their own know how and were difficult to be standardized as test procedure or reliability specification, this technical report was agreed to remain as a guide.

3. Contents

Explanation was given to the fundamental mechanisms of flash memory, reliability concerns, reliability test methods, differences of various reliability remarks for various applications and fundamental concepts of reliability test conditions that reflect application conditions. It is also noted that statistical method is affective for reliability projection. We believe that this technical report provides users who are even relatively newcomers to flash memory with better understanding which points to remark and which reliability data to request.

4. Members

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