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EIAJ EDR-5202

ASIC performance evaluation guideline

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ASIC performance evaluation guideline

1. Scope

This standard provides a guideline regarding methods to evaluate the performance of unit gates and benchmark circuits of ASIC products . The scope of this standard is mainly applicable to CMOS gate arrays, embedded arrays, cell-based ICs and other digital circuits.

2. Definition of Terms

The main terms used in this standard are defined in the **appendix**.

3. Purpose of Standard

The purpose of this standard is to provide a set of criteria for ASIC selection by clarifying the standard for indicating characteristics through the use of common evaluation conditions.

4. Evaluation Items

This guideline indicates the ASIC performance by evaluating both unit gates and the benchmark circuit.

4.1 Unit gate

This performance shows 2-input NAND gates speed with the unified load condition.

Operation speed (propagation delay time under typical conditions)

Power dissipation (dynamic power dissipation per 1MHz of measured circuit under typical conditions)

4.2 Benchmark circuit

This performance shows the simple sequential circuit speed under actual condition with estimated wire loads.

Maximum operating frequency (the worst case conditions)

Power dissipation (dynamic power dissipation per 1MHz of measured circuit under typical conditions)

5. Evaluation Method

5.1 Unit gate

(1) Evaluation method: Transistor level simulation (e.g. SPICE) shall apply for the evaluation.

(2) Types of gates for measurement: 2-input NAND gates

(3) Evaluation circuit:

Both the circuit configurations shown in **Figure 1-1** and **1-2** are used. Each circuit is configured of a measured gate (G7) and at least 6 stages of waveform shaping gates which are same type (G1 to G6). The figures specified the portion of the propagation delay time measurement. **Figure 2** shows the transistor level equivalent circuit of the 2-input NAND gate. The transistor level circuit includes parasitic resistance and capacitance during library compilation, which are not shown in the figure. The dynamic current (I_{DD}) is measured at point P indicated in the figure.

(4) Load conditions: Simulation is performed under the following two conditions.

(a) Wire length 0 mm + connection of one 2-input NAND gate of the same type as the measured gates.

(b) Wire length equal to metal pitch x 500 + connection of one 2-input NAND gate of the same type as the measured gates. The resistance and capacitance of the wire to be treated as load must be included. However, resistance and capacitance such as VIA can be ignored. The structure immediately under the metal layer is irrelevant. The adjacent and crossing effect shall be ignored in wiring models. The metal pitch refers to the routing grid during automatic routing. If variable metal pitch is used within the same wiring layer, the statistical average metal pitch is used as the metal pitch for that layer. In the case of a product with double layer metal, the wire length is the sum of 250 times the metal pitch of the first layer metal and 250 times the metal pitch of the second layer metal. In the case of a product with triple layer metal or more metal layers, the wire length is the sum of 250 times the metal pitch of the second layer metal and 250 times the metal pitch of the third layer metal.

(5) Measurement conditions: Simulation shall be performed under the following typical conditions.

(a) Supply (power supply) voltage (V_{DD})

More then one typical voltage values can be set providing they are within the specifications.

(b) Temperature

Junction temperature: T_j – 25°C

(c) Process conditions

Typical characteristics shall be used.

(d) Input waveform

The amplitude of the input waveform to the G1 gate in Figure 1 shall be the full swing from 0 V to V_{DD}. Any rise time (t_r) and fall time (t_f) within a specification can be used.

(6) Measurement (evaluation) procedure

(a) According to the evaluation circuits (**Figure 1-1** and **Figure 1-2**), simulation circuits under each load conditions (2 types: (4)-(a) and (4)-(b)) shall be prepared.

(b) The propagation delay time and the dynamic power dissipation shall be measured for each evaluation circuit with specific load conditions by performing simulation.

Note 1: Measurement method for propagation delay time

The propagation delay time of each evaluation circuit (t_{pd1} or t_{pd2}) shall be calculated as the average of the rise propagation delay time (t_{pLH1} or t_{pLH2}) and the fall propagation delay time (t_{pHL1} or t_{pHL2}) ($t_{pd1} = (t_{pLH1} + t_{pHL1})/2$) or ($t_{pd2} = (t_{pLH2} + t_{pHL2})/2$). The propagation delay time (t_{pd}) shall be calculated as the average of t_{pd1} and t_{pd2} ($t_{pd} = (t_{pd1} + t_{pd2})/2$). In the measurement waveform diagram shown in Figure 3, the duty cycle of the input waveform shall be 50%. The measurement frequency and measurement reference voltage (V_{ref}) are not specified particularly. The unit used shall be ps (pico second).

Note 2: Measurement method for dynamic power dissipation

The dynamic power dissipation P_{D1} or P_{D2} of each evaluation circuit shall be calculated as the average for one cycle (product of supply voltage and average current). Dynamic power dissipation P_D shall be calculated as the average of P_{D1} and P_{D2} ($P_D = (P_{D1} + P_{D2})/2$). The duty

cycle of the input waveform shall be 50%, and the measurement frequency shall be 1 MHz. The unit used shall be μ W/MHz/gate.

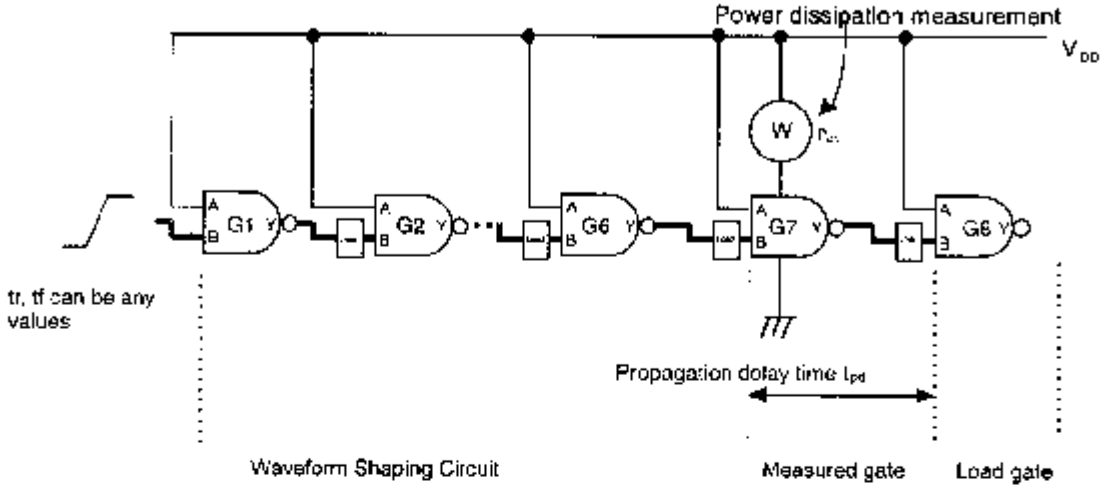


Figure 1-1. Propagation Delay Time & Power Dissipation Measurement Circuit-1

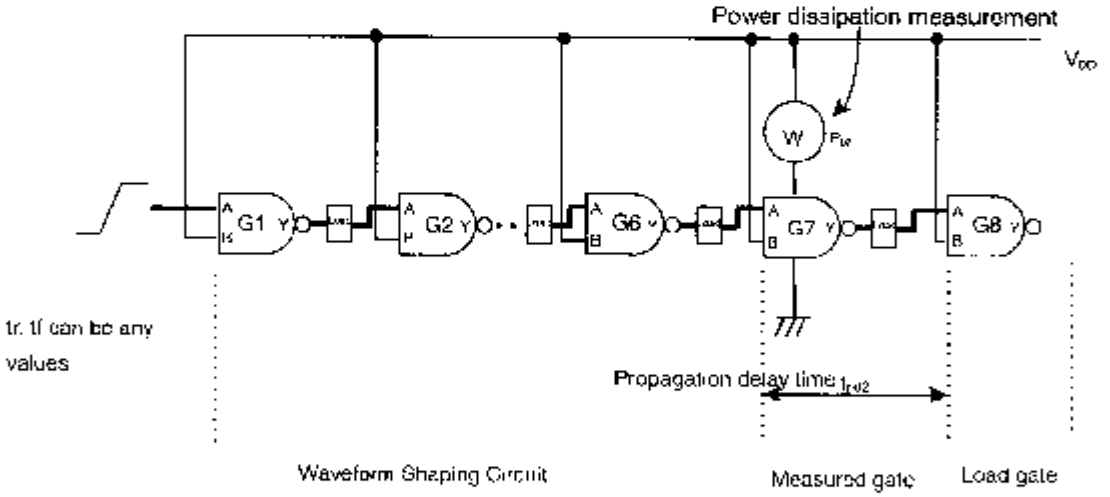


Figure 1-2. Propagation Delay Time & Power Dissipation Measurement Circuit-2

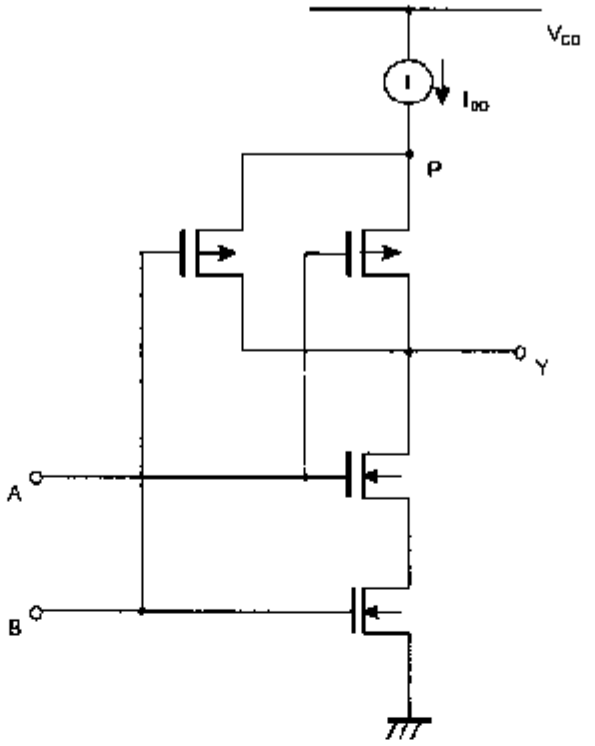
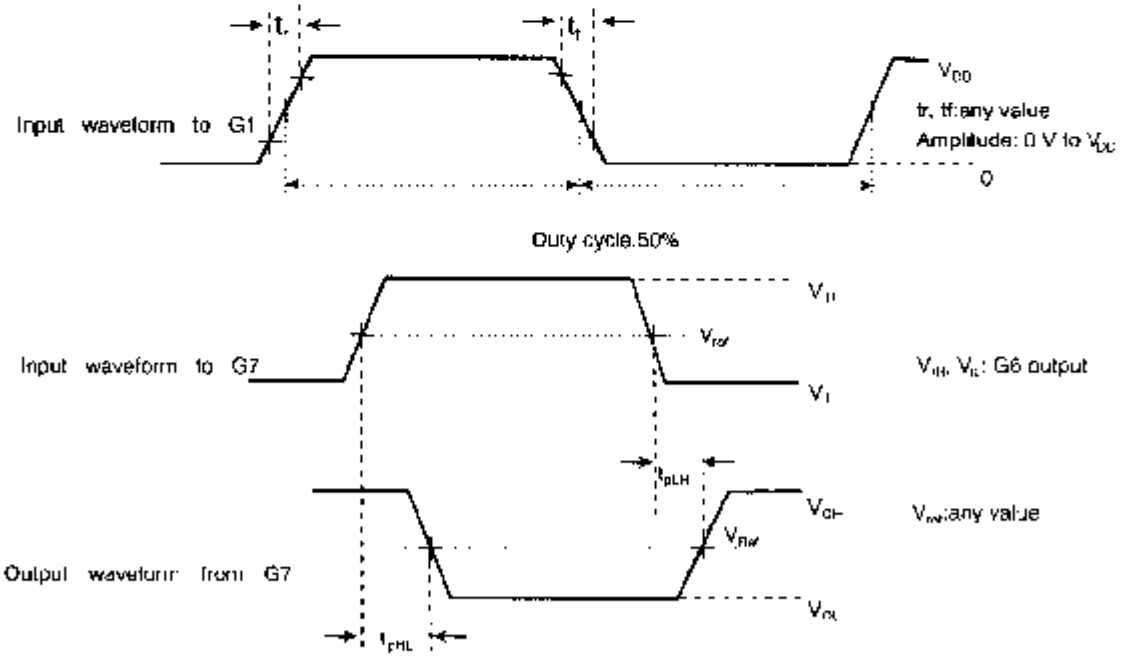


Figure 2. Equivalent Circuit for Transistor Level



For example, propagation delay time t_{pd} is obtained as follows:
$t_{pd1} = (t_{pLH} + t_{pHL})/2$

Figure 3. Measurement Waveform

5.2 Benchmark circuit

(1) Evaluation method

Evaluation (measurement) shall be performed using gate-level simulation.

Note: Customers can obtain the same results using the ASIC vender library.

(2) Evaluation circuit

Figure 4 shows the circuit configuration. The evaluation circuit consists of NAND gates, NOR gates, D-F/Fs, and inverters. All gates have the same drivability type as the 2-input NAND gate used in the unit gate evaluation. Similar to the unit gate evaluation circuit, the clock signal has to go through the waveform shaping circuit before the signal is supplied to the CK terminal of each F/F. The circuit between F/F1 and F/F2 is a 16-stage gate chain. Each unit stage has a 2-input NAND gate and a 2-input NOR gate. Both inputs are connected in parallel. The unit stage connection of NAND gate and NOR gate shall be incorporated in the chain alternately, as shown in **Figure 4**.

Note: That D01 to D18 are the gates added as fan-out load. Those gates can not be removed.

(3) Load conditions

The estimated wire length model regularly provided by the ASIC vendor shall be applied. The estimated wire length model shall be equivalent to 10,000 usable gates. If this model is not available, a model whose die size is more than 10,000 usable gates can be used. For the waveform shaping circuit, the same model has to be chosen.

(4) Measurement conditions

Simulation shall be performed under the worst case condition at which the delay time becomes the maximum value. The clock skew at the CK terminal of each F/F can be ignored.

(a) Supply voltage (V_{DD})

The supply voltage at which the specification guarantees the operation and the delay time becomes the maximum value shall be used. Several supply voltages can be defined.

(b) Temperature

The junction temperature at which the specification guarantees the operation and the delay time becomes the maximum value shall be used.

(c) Process condition

The worst case process condition shall be used.

(d) Input waveform

The voltage swing of the clock signal (CLK) in **Figure 4** is rail to rail between 0V and V_{DD}. Any slew of the clock signal can be used. A 50% duty cycle is assumed. The data input (D_{in}) is required to have a waveform which keeps the set-up time (t_{su1}) necessary for the normal operation of F/F1.

(5) Measurement procedure

(a) Prepare the circuit schematics for simulation referring to the evaluation circuit shown in **Figure 4**.

(b) Measure the maximum frequency by simulation. Measure the dynamic power dissipation as a typical value under the similar typical conditions used in the unit gate evaluation. The dynamic power dissipation may not be obtained on the customer side.

Note 1: Maximum operating frequency

The maximum operating frequency is defined as the inverse of the minimum operating cycle time that keeps the set-up time constraint of F/F2. If the operating frequency is dependent on the logical level of the data input (D_{in}), the lower frequency shall be chosen as the maximum operating frequency.

Note 2: Dynamic power dissipation

Measure the dynamic power dissipation of two D-F/Fs (F/F1 and F/F2) and the 16-stage chain which consists of 2-input NAND gates and 2-input NOR gates between two D-F/Fs in **Figure 4.** The waveform shaping circuit (G1 to G6) and load gates (D17 and D18) should be excluded from the power measurement. Calculate the typical power dissipation by using a transistor level or gate-level simulator.

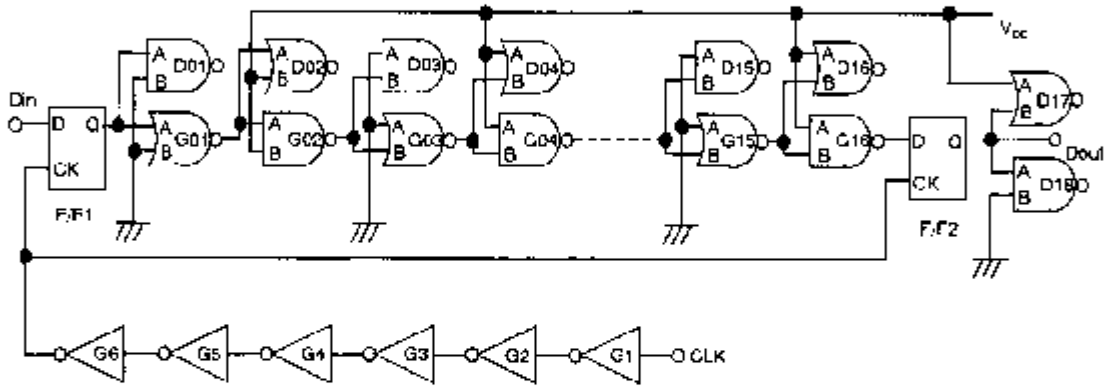


Figure 4. Benchmark Circuit

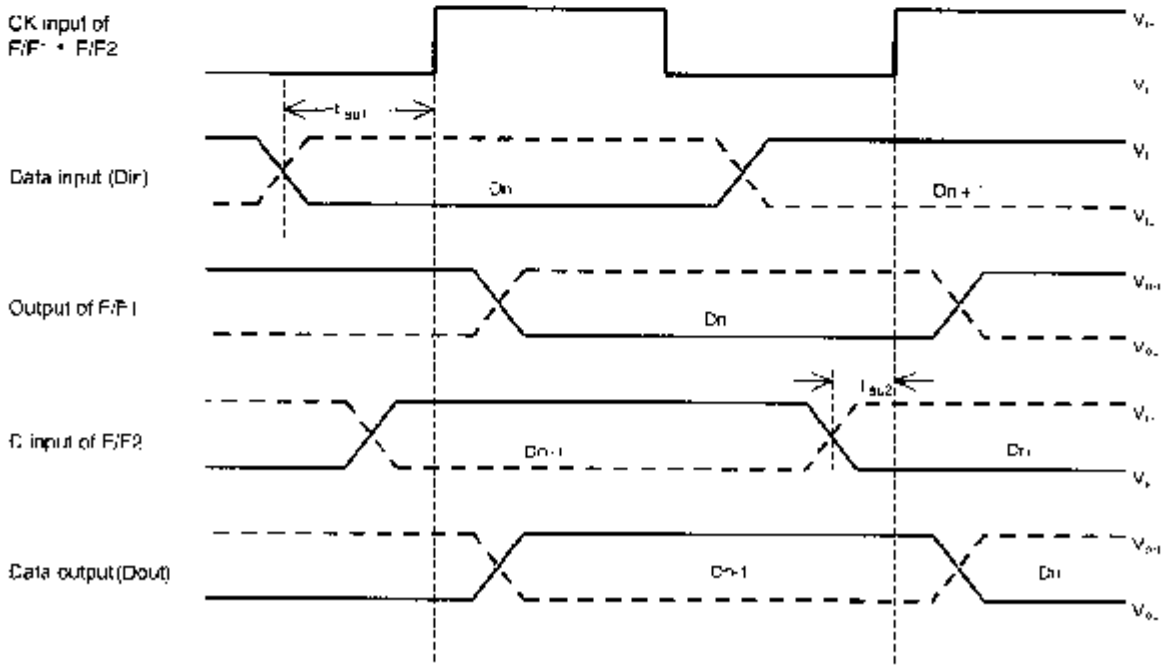


Figure 5. Measurement Waveform

6. Characteristics indication standard

When indicating the name of an EIAJ standard (**EDR-5202**), etc., in literature introducing ASIC products, incidental conditions for each characteristic shall be indicated.

6.1 Unit gate

Propagation delay time	(typical condition)
Dynamic power dissipation	(typical condition)
Indication of gate drivability	(cell name and drivability type or relative value for drivability for standard gate)
Supply voltage	

6.2 Benchmark circuit

Maximum operating frequency (worst case condition)

Indication of gate drivability	(cell name and drivability type or relative value for drivability for standard gate)

Measurement conditions

The dynamic power dissipation under typical (typ.) conditions and the name of the power calculation tool used to obtain it shall be indicated as reference.

7. Example

Unit gate	EIAJ standard **EDR-5202** compliant	
2-input NAND	Load condition (a) (without wire loads)	Load condition (b) (with wire loads)
Propagation delay time (typ.)	100 ps	150 ps
Dynamic power dissipation (typ.)	1 μW/MHz/Gate	1.2 μW/MHz/Gate
Indication of gate drivability	2NAND2 *1	2NAND2 *1
	*1 (Use gate with drivability double that of standard gate)	
Supply voltage	3.3 V	3.3 V

Benchmark circuit	EIAJ standard **EDR-5202** compliant
Maximum operating frequency (worst)	150MHz
Indication of gate drivability	Use gate with drivability double that of standard gate
Supply voltage	3.0 V
Junction temperature	T_j = 125°C
Product name for evaluation	
[Reference values]	
Dynamic power dissipation (typ.) under typical conditions	30 μW/MHz (supply voltage: 3.3 V)

Method to obtain dynamic power dissipation calculation with SPICE (or gate level power calculation tool)

Appendix Definition of Terms

Amplitude	The electric potential difference between the high level and the low level of a pulse signal.
Application Specific IC (ASIC)	LSI configured by integrating required functions to support specific purposes. A standardized cell library and design environment are provided to shorten the development time. Gate Arrays, Embedded Arrays, and Cell Based ICs are representative ASICs.
Automatic Routing	Generating physical wire on an LSI in automatic method based on the circuit information (net list).
Benchmark Circuit	Reference circuit prepared for comparing and evaluating the electrical characteristics (performance) of electronic (electric) components.
Cell Based IC	LSI that uses standard cell libraries, which are structured in a hierarchical manner. Also called Standard Cell.
Cell Name	Element name that is used to describe a logic circuit used in an ASIC.
Delayed Flip-flop (D-F/F)	A logical memory element that replaces the logical value held until then with the logical value of a previously added data input when the clock signal changes to the active edge, and that keeps holding its logical value during all other states.
Drivability	Drive strength of output. Determined by the size of the transistors of the cell output circuit.
Drivability Type	Type of the drive strength. Indicates the drive strength type, such as standard, power etc., based on the drive strength of the basic gate.
Duty Cycle	The ratio of the high level time interval and low-level time interval of an input or output signal during 1 cycle.
Dynamic Power Dissipation	The dynamic power dissipation is obtained by integrating over time the supply current (current waveform) that flows in a measurement circuit over a given period of time, averaging the result over time and then multiplying it with the supply voltage.
Embedded Array	LSI that includes gate array area and macro cell(s) for Cell Based IC, such as CPU, memory, and/or analog macro cells.
Estimated Wire Length Model	Estimated wire length model that is used for evaluating the characteristics of ASICs prior to automatic layout.
Fall Time (tf)	The time interval determined by two reference voltages specified within the falling interval of a pulse.
Gate Array	LSI for which only the wiring needs to be done according to the product design, on a common master with basic elements laid over it in a regular pattern that is independent of any product design.
Inverter	A type of logical operation element that has one input and one output. It inverts and then outputs the logical level of the input signal.
Junction Temperature (T_j)	Temperature of PN junction. Unit is degrees Celsius (°C).

Library	Data set, such as functions and electrical specifications, that is used for ASIC design.
Maximum Operating Frequency	For a measurement circuit, the maximum clock frequency for which acquisition of output status changes expected under the specified operating conditions is guaranteed.
Metal Pitch	The minimum distance of wire to wire used in Automatic Routing.
NAND Gate	A type of logical operation element that has several inputs and one output. It outputs a logical "L" only if a logical "H" is fed to all its inputs, and outputs a logical "H" if a logical "L" is fed to one or more of its inputs.
NOR Gate	A type of logical operation element that has several inputs and one output. It outputs a logical "L" when a logical "H" is fed to one or more inputs, and outputs a logical "H" only if a logical "L" is fed to all of its inputs.
Process Condition	Condition indicating variation in process characteristics. Typical characteristics of process conditions are the characteristics existing during fabrication under standard conditions.
Propagation Delay Time	For a given circuit to be measured, assuming an input signal for which conditions have been set that enable changes of the output signal, the propagation delay time is the time that elapses from when the input signal level passes a specified voltage until when the output signal level passes a specified voltage.
Propagation Delay Time, high-to-low-level output	For a given circuit to be measured, assuming an input signal for which conditions have been set that enable changes of the output signal level from "H" to "L", the propagation delay time is the time that elapses from when the input signal level passes a measurement reference voltage until when the output signal level passes a measurement reference voltage.
Propagation Delay Time, low-to-high-level output	For a given circuit to be measured, assuming an input signal for which conditions have been set that enable changes of the output signal level from "L" to "H", the propagation delay time is the time that elapses from when the input signal level passes a measurement reference voltage until when the output signal level passes a measurement reference voltage.
Reference Voltage	Voltage that determines the measurement point for switching characteristics.
Rise Time (t_r)	The time interval determined by two reference voltages specified within the rising interval of a pulse.
Setup Time	Required minimum time at F/F for securing the data signal that is to be read before the clock signal level changes.
Simulation	Method based not on the actual physical structures but on software run on a computer, which is used to verify whether a circuit operates as intended with regard to functions and performance, and to analyze circuit operation.
Supply Voltage (V_{DD})	Supply voltage for which operation of an element is guaranteed to be within the specification range.

Typical Condition (typ.)	Typical operating condition or characteristic indicated in a catalog or data sheet. Generally, process conditions consist of standard characteristics, the supply voltage is a reference voltage value, and the junction temperature is T_j=25°C.
Typical Value (typ.)	Value under standard operating condition for which the operation of an element is guaranteed.
Unit Gate	Basic component element or unit logical gate of Gate Array or Cell Based IC. (For example, 2-input NAND gate)
Variable Metal Pitch	Routing pitch that is not fixed in the same metal layer when performing Automatic Routing.
Waveform Shaping Circuit	Circuit connected in series to several logic gates such as inverters, NANDs, and NORs, so as to cancel the dependence of first-stage gate input waveform on the output waveform of the last-stage gate.
Worst Case Condition	The condition whereupon the process conditions, supply voltage, and junction temperature cause the device to incur the longest propagation delay time.

EXPLANATORY NOTES

1. Objectives of Establishment

As there has been no standard method to indicate the basic performance of ASIC products, each ASIC vendor has been using its own method. Recently, both ASIC users and vendors have been strongly requesting the establishment of a standard for ASIC performance evaluation. In response to this, the EIAJ Semiconductor Standardization Committee/Integrated Circuit Group decided to investigate this kind of standardization and set up the ASIC Standardization Project group, which produced this ASIC Performance Evaluation Guideline. The purpose of this guideline is to provide a set of criteria for ASIC selection by clarifying performance-indicating standards based on common evaluation conditions.

2. Process of Discussion

The EIAJ Semiconductor Standardization Committee/Integrated Circuit Group held preliminary discussions in May and July 1996, resulting in the decision by the EIAJ Semiconductor Standardization Committee to formally promote this standardization. Following this decision, the ASIC Standardization Project Group was established and met once a month for discussions on how to realize this standardization, finally deciding to adopt a simulation method.

The points of discussion were as follows.

1) Unit gate evaluation method
2) Benchmark circuit evaluation method

A draft of this guideline in Japanese was provided in June 1998, and a draft in English became available in December 1998. The finalized guideline is due to be approved by the EIAJ Semiconductor Standardization Committee/Integrated Circuit Group in May 1999.

3. Discussion point

This guideline is quite new, so there were many points of discussion, the main 4 of which were as follows.

(1) An evaluation method without dependency on the silicon process generation

Evaluation conditions i.e. power supply voltage, temperature, and wire load, able to be defined by a common method that can be used beyond the silicon process generation were set.

(2) Wire load at unit gate evaluation

To allow for the use of gate arrays, embedded arrays, and cell-based ICs, the pros and cons of two wire load conditions; one without wire load and the other with wire load were discussed, as was a wire metal pitch that can realize a wire load not dependant on the silicon process generation.

(3) Benchmark circuit

Several kinds of circuits were initially investigated, including a popular benchmark circuit in an ASIC technology journal, which was later abandoned due to property problems.

Finally, the circuit introduced here was chosen.

(4) Power dissipation

The purpose of evaluation, what kind of simulator to use, and an evaluation method that included the calculation method and accuracy of that simulator were discussed.

4. Members of discussion

This guideline has been discussed by ASIC Standardization Project Group which belongs to Group on Integrated Circuits of Technical Standardization Committee on Semiconductor Devices.
The members are listed below.

<Technical Standardization Committee on Semiconductor Devices>

Chairman	Mitsutoshi Ito	NEC Corporation

<Group on Integrated Circuits>

Chief Examiner	Motoo Nakano	FUJITSU LIMITED

<ASIC Standardization Project Group>

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Sub-leader	Hiroaki Sato	NEC Corporation
Member	Osam Ohba	KAWASAKI STEEL CORPORATION
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