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Design guideline of integrated circuits for Thin Small Outline Package (Type I) (TSOP(I))

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Technical Standardization Committee on Semiconductor Device Package

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EIAJ Technical Report

Design Guideline of Integrated Circuits for Thin Small Outline Packages (Type I) (TSOP (I))

1. Scope of application

This technical report applies to the outline drawings and dimensions of the thin small outline packages (type I) (hereinafter referred to as the TSOP (I)) which are classified as the form B under the EIAJ ED-7401A (Basic Items Related to the Rules for the Semiconductor Package Outline (Integrated circuits and Individual Semiconductors)).

2. Terminology

The terms used in this technical report shall conform to those defined in the EIAJ ED-7401A. The new terms not included therein shall be defined in the text of this report.

3. History

Recently, the outline and thickness of the integrated circuits for the memory application have been drastically reduced in order to cope with newly launched very thin electronic equipment such as the IC card. The general rules for the outline aim at promoting the standardization of the TSOP (I) dimensions and to assure the compatibility among them of which uses have been increased.
The design values, or the concept by the design center, are showed in the fullest extent possible in order to increase the role as the standardization index upon specifying the respective dimensions.

4. Definition of the TSOP (I)

A package that satisfies all the following requirements; the maximum mounting height of 1.20 mm, maximum linear distance of 0.80 mm between the pins, leads extending to the two directions from the shorter sides of the package, and the leads with a flat surface extending toward outside to enable the package being mounted on the surface of the printed circuit board.

5. Designation of the pin numbers

The method to designate the pin numbers shall conform to the specifications included in the EIAJ ED-7401A.

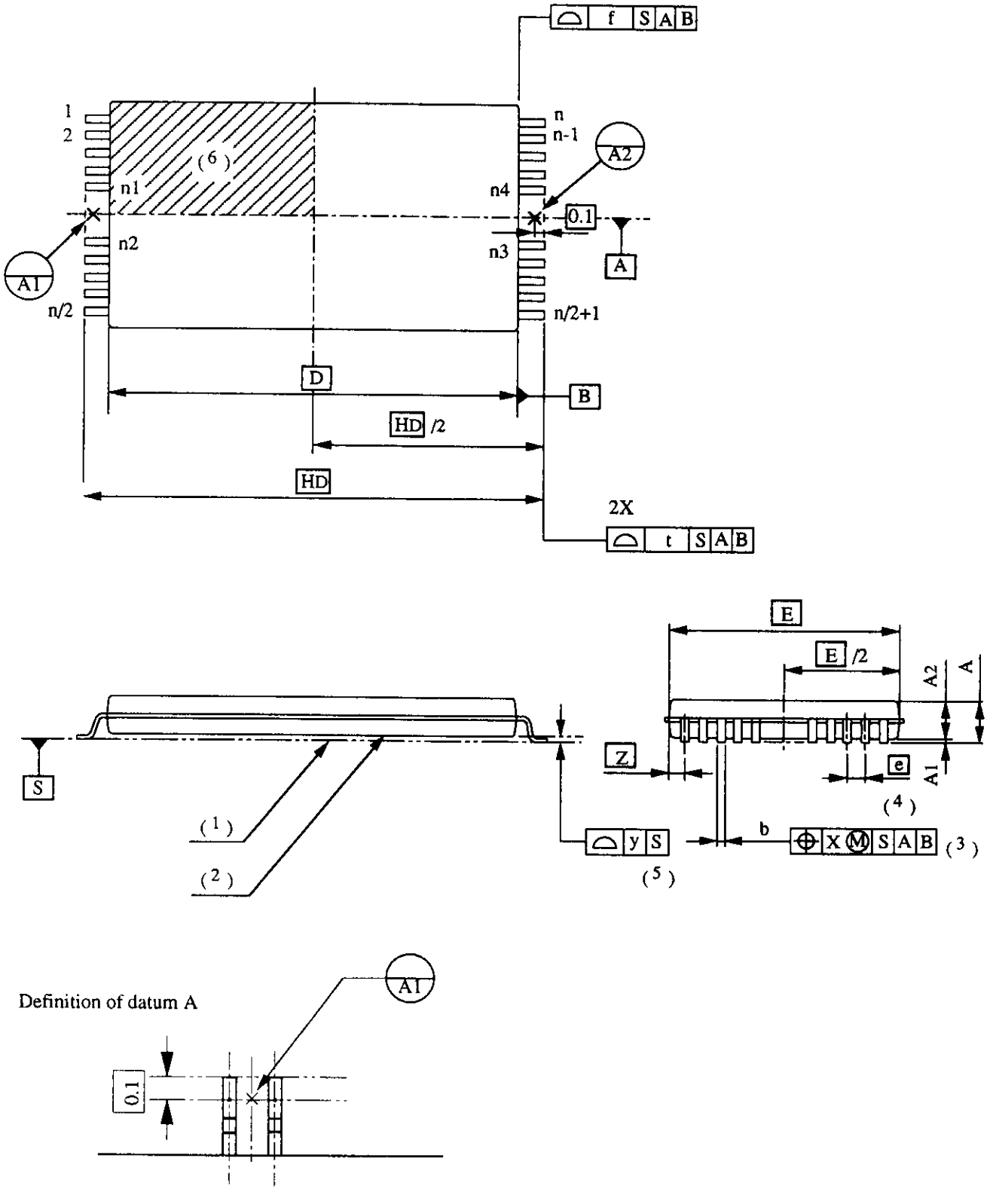
6. Nominal dimensions

The outermost dimensions of the package (Reference codes: E x ED) shall be used as the nominal dimensions in this technical report.

7. REFERENCE CHARACTERS AND DRAWING

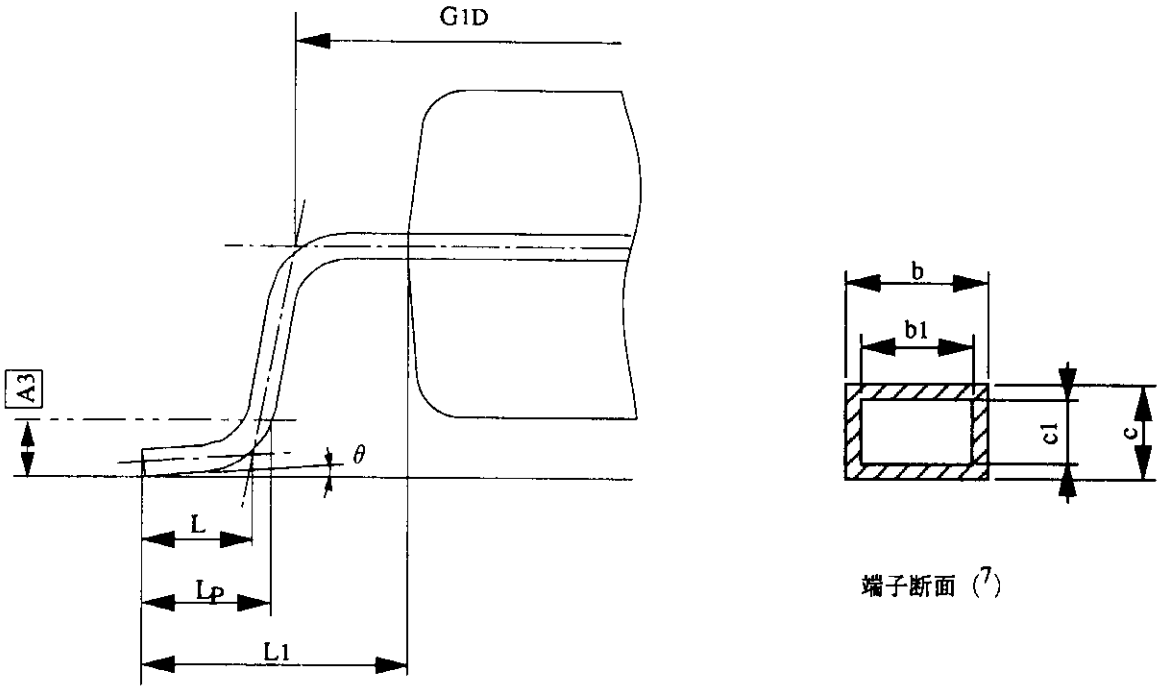
7.1 Outline Drawings

Figure 1



The center of facing side of adjacent leads
at a position 0.1mm inside top of the leads.

Figure 2

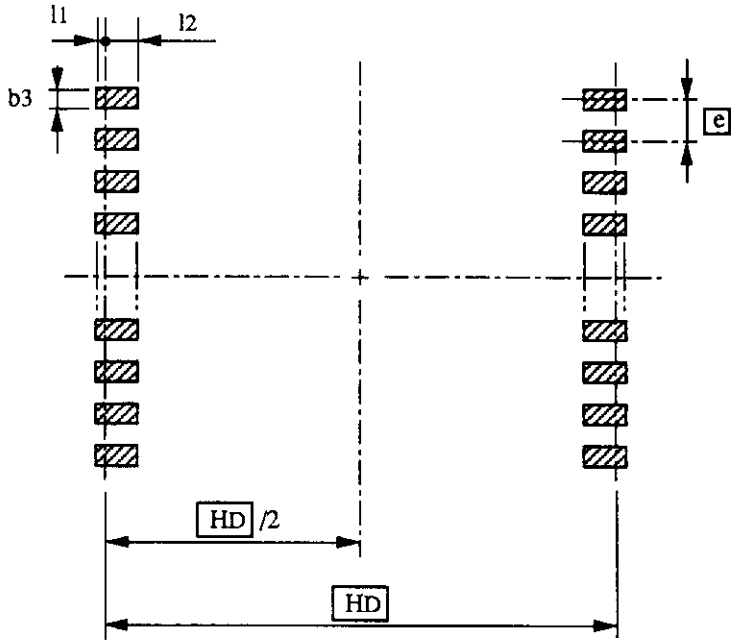


Note
(1) The mounting surface , with which a package is in contact.
(2) The base surface , which is in parallel with the mounting surface and links the lowest points , except the stand - off.
(3) The maximum mounting conditions apply to the positional tolerance of the terminals. (For the maximum body conditions , refer to ISO 2692/ JIS B 0023.)
(4) Specifies the true geometric position of the terminal axis.
(5) Specifies the vertical shift of the flat part of each terminal form the mounting surface.
(6) Shows the allowable position of the index mark , which must be included in the shaded area entirely.
(7) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

Remarks : Range where terminals to be soldered exist

The range where the terminals to be soldered can exit is shown in Figure 3 as reference for foot print design.

Figure 3



l1 max = t / 2

l2 max = Lp max + t / 2

b3 max = b max + x

8. OUTER DIMENSION

8.1 GROUP 1

Table 1

Unit mm

Description	Symbol	Standard	Recommended Values	Remarks
Nominal dimensi-ons	E × HD	E × HD 6×14 8×14 14×20 6×16 8×16 6×18 8×18 6×20 8×20 10×14 12×14 10×16 12×16 10×18 12×18 10×20 12×20	———	
Package width	E	E = 6 + 2k k = 0,1,2,3,4 k | E 0 | 6.00 1 | 8.00 2 | 10.00 3 | 12.00 4 | 14.00	———	(1) Dimension E does not include resin fines and gate remainders. (2) It is recommended that upper and lower cavities be equal. If they are differnt, the larger dimension shall be regarded. (3) Mold protrusion is less than 0.20mm.
Package length	D	D = HD − 2L1 nom	———	(1) Dimension D does not include resin fines and gate remainders. (2) It is recommended that upper and lower cavities be equal. If they are differnt, the larger dimension shall be regarded.

Table 1 (Continued)

Unit mm

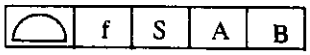
<table>
<tr><th>Description</th><th>Symbol</th><th>Standard</th><th>Recommended Values</th><th>Remarks</th></tr>
<tr><td>Tolerance of package edge</td><td>f</td><td>(1) Tolerance of package edge shall be specified in the outline drawing.
 
(2) The symbol f shall be replaced with any of the values shown below.
<table><tr><th>f</th></tr><tr><td>0.10</td></tr></table></td><td>——</td><td></td></tr>
<tr><td>Package height</td><td>A2</td><td><table><tr><th>min</th><th>nom</th><th>max</th></tr><tr><td>0.95</td><td>1.00</td><td>1.05</td></tr></table></td><td>——</td><td>(1) Bend of package is included.</td></tr>
<tr><td>Overall width</td><td>HD</td><td>HD = 14 + 2h
h = 0,1,2,3
<table><tr><th>h</th><th>HD</th></tr><tr><td>0</td><td>14.00</td></tr><tr><td>1</td><td>16.00</td></tr><tr><td>2</td><td>18.00</td></tr><tr><td>3</td><td>20.00</td></tr></table></td><td>——</td><td></td></tr>
<tr><td>Seated height</td><td>A</td><td><table><tr><th>min</th><th>nom</th><th>max</th></tr><tr><td></td><td></td><td>1.20</td></tr></table></td><td>——</td><td>(1) Bend of package is included.</td></tr>
<tr><td>Stand-off height</td><td>A1</td><td><table><tr><th>min</th><th>nom</th><th>max</th></tr><tr><td>0.05</td><td>0.10</td><td>0.15</td></tr></table></td><td>——</td><td></td></tr>
<tr><td>Standard height of soldered points</td><td>A3</td><td>A3 = 0.25</td><td>——</td><td></td></tr>
<tr><td>Length of soldered part</td><td>Lp</td><td><table><tr><th>min</th><th>nom</th><th>max</th></tr><tr><td>0.45</td><td>0.60</td><td>0.75</td></tr></table></td><td>——</td><td></td></tr>
</table>

Table 1 (Continued)

Unit mm

<table>
<tr><th>Description</th><th>Symbol</th><th>Standard</th><th>Recommended Values</th><th>Remarks</th></tr>
<tr><td rowspan="2">Terminal width</td><td>b</td><td>
<table>
<tr><th>e</th><th>min</th><th>nom</th><th>max</th></tr>
<tr><td>0.65</td><td>0.17</td><td></td><td>0.32</td></tr>
<tr><td>0.50</td><td>0.17</td><td></td><td>0.27</td></tr>
<tr><td>0.40</td><td>0.13</td><td></td><td>0.23</td></tr>
<tr><td>0.30</td><td>0.09</td><td></td><td>0.175</td></tr>
</table>
<table>
<tr><th rowspan="2">e</th><th colspan="2">b nom</th></tr>
<tr><th>Pb/Sn Solder plating</th><th>Pd plating</th></tr>
<tr><td>0.65</td><td>0.24</td><td>0.22</td></tr>
<tr><td>0.50</td><td>0.22</td><td>0.20</td></tr>
<tr><td>0.40</td><td>0.18</td><td>0.16</td></tr>
<tr><td>0.30</td><td>0.14</td><td>0.12</td></tr>
</table>
</td><td></td><td rowspan="2">(1) b1 denotes the material width of a lead frame.
(2) b denotes the width of a plated terminal.
(3) b1 and b apply to the ranges of 0.1 and 0.25 from the end of a terminal.
(4) Values b apply to Pb/Sn solder plated terminal. The standard thickness of the solder layer shall be 0.010+0.010 -0.005
(5) As Pd platig, it is very thin so terminal width is bnom=b1nom</td></tr>
<tr><td>b1</td><td>
<table>
<tr><th>e</th><th>min</th><th>nom</th><th>max</th></tr>
<tr><td>0.65</td><td>0.17</td><td>0.22</td><td>0.27</td></tr>
<tr><td>0.50</td><td>0.17</td><td>0.20</td><td>0.23</td></tr>
<tr><td>0.40</td><td>0.13</td><td>0.16</td><td>0.19</td></tr>
<tr><td>0.30</td><td>0.09</td><td>0.12</td><td>0.15</td></tr>
</table>
</td><td>——</td></tr>
<tr><td rowspan="2">Terminal thickness</td><td>c</td><td>
<table>
<tr><th>e</th><th>min</th><th>nom</th><th>max</th></tr>
<tr><td>0.65</td><td>0.09</td><td></td><td>0.20</td></tr>
<tr><td>0.50</td><td>0.09</td><td></td><td>0.20</td></tr>
<tr><td>0.40</td><td>0.09</td><td></td><td>0.20</td></tr>
<tr><td>0.30</td><td>0.09</td><td></td><td>0.20</td></tr>
</table>
</td><td>(1) Pb/Sn Solder plating
c nom
= 0.170
0.145
0.120
(2) Pd plating
c nom
= c1 nom</td><td rowspan="2">(1) c1 denotes the material width of a lead frame.
(2) c denotes the width of a plated terminal.
(3) c1 and c apply to the ranges of 0.1 and 0.25 from the end of a terminal.
(4) Values c apply to Pb/Sn solder plated terminal. The standard thickness of the solder layer shall be 0.010+0.010 -0.005
(5) As Pd platig, it is very thin so terminal width is cnom=c1nom</td></tr>
<tr><td>c1</td><td>
<table>
<tr><th>e</th><th>min</th><th>nom</th><th>max</th></tr>
<tr><td>0.65</td><td>0.09</td><td></td><td>0.16</td></tr>
<tr><td>0.50</td><td>0.09</td><td></td><td>0.16</td></tr>
<tr><td>0.40</td><td>0.09</td><td></td><td>0.16</td></tr>
<tr><td>0.30</td><td>0.09</td><td></td><td>0.16</td></tr>
</table>
</td><td>c1 nom
= 0.15
0.125
0.10</td></tr>
</table>

Table 1 (Continued)

Unit mm

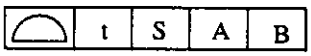
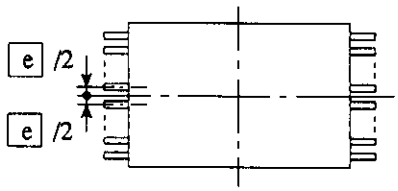
Description	Symbol	Standard	Recommended Values	Remarks
Angle of terminal flat portions	θ	min: 0° / nom: 3° / max: 8°	———	
Terminal pitch	e	e = 0.65, 0.50, 0.40, 0.30	———	
Tolerance of terminal center position	x	e: 0.65 / x: 0.13; e: 0.50 / x: 0.10; e: 0.40 / x: 0.07; e: 0.30 / x: 0.065	———	
Coplanarity	y	e: 0.65 / y: 0.10; e: 0.50 / y: 0.10; e: 0.40 / y: 0.08; e: 0.30 / y: 0.05	———	
Positional tolerance of terminal tips	t	(1) The tolerance of the terminal tips shall be specified in the outline drawing.  (2) The character x shall be replaced with any of the values shown below. t: 0.20	———	
Standard number of terminal	n	E / e: 0.65 / 0.50 / 0.40 / 0.30: 6.00: 16 / 24 / 28 / 36; 8.00: 24 / 32 / 40 / 52; 10.00: 28 / 40 / 48 / 64; 12.00: 36 / 48 / 60 / 76; 14.00: 40 / 56 / 68 / 88	———	(1) While complying with the specifications for the arrangement of terminals and on assumption that ZE = 0.2, express the maximum number of terminals that can be accommodated in the standard package width of E by n.

Table 1 (Continued)

Unit mm

Description	Symbol	Standard	Recommended Values	Remarks
Terminal layout		Terminal shall be arranged shown below.  The terminal center is deviating from the package center by e /2.	—	

2. Group 2

Table 1 (Continued)

Unit mm

Description	Symbol	Standard	Recommended Values	Remarks
Width between first bent part of terminal	G1D	L1 nom: 0.80 — G1D nom: D + 0.40	——	(1) Used for designing a test socket, tray,etc.
Package over hang	Z	Z = (E - (n/2 - 1) × e) / 2	——	(1) Resin burrs or residual gates are not included.
Length of flat part of terminal	L	min: — / nom: 0.50 / max: —	——	
Terminal length	L1	min: — / nom: 0.80 / max: —	——	

9. Individual standard

The format for the individual standard is shown below. The format shown below shall be used when a TSOP (I) package is to be proposed, established, or issued as an individual standard.
Note that the type of outline shall be indicated in accordance to the EIAJ ED-7401-2 "Name and Code of the Semiconductor Devices (Integrated Circuit)".

Serial Number				
External Type.		TSOP(I) XXX - P - XXXX - X.XX		
Reference Symbol		min	nom	max
Group 1	E		✓	
	D		✓	
	f			✓
	A2	✓	✓	✓
	HD		✓	
	A			✓
	A1	✓	✓	✓
	A3		✓	
	Lp	✓		✓
	b	✓		✓
	b1	✓	✓	✓
	c	✓		✓
	c1	✓		✓
	θ	✓	✓	✓
	e		✓	
	x			✓
	y			✓
	t			✓
	n		✓	
	n1		✓	
	n2		✓	
	n3		✓	
	n4		✓	
Group 2	GID		✓	
	ZE		✓	
	(L)		✓	
	(L1)		✓	

Explanatory notes

1. Purpose of establishment

This technical report is established to show the design guideline when developing the industry norms and related parts for the thin small outline package type (I) (hereinafter referred to as the TSOP (I)), which is a revision of the EIAJ ED-7402-3.

2. History of the review

A thin and small TSOP (I), being as the integrated circuit for the IC card application, was firstly launched by a domestic manufacturer in 1987, which drew the industry's attention. Since the outline of this type was expected to be rapidly and widely applied to the IC cards and memory modules in the future, it was necessary to standardize the TSOP (I) at an earliest date possible. For this purpose, it was decided in a hurry to standardize the outline for the TSOP (I) integrated circuits at the third Semiconductor Committee meeting held in June, 1987 since this subject was not included in the original business plan. Accordingly, the concrete reviews were commenced upon presentation of the draft standard prepared by the secretary company at the forth Committee meeting held in July, 1987.

Except for the methods how to group the overall length and linear pin distance, the reviews progressed smoothly due to the new package outline. The final review was completed at the tenth Committee meeting held in March, 1988, and the standard was established and issued as the EIAJ IC-74-2-II. Subsequently, it was established and issued as the EIAJ ED-7402-3 based on the approval given by the fourth Semiconductor Package Special Committee (the antecedent of the Semiconductor Package Standardization Committee) meeting after partial revisions in the contents, form, and standard number thereof.

However, since the inconsistency between the standard and the general rules became notable due to the diversifications and increased demands for the package, a proposal was made to review the standard at the seventeenth Semiconductor Package Special Committee meeting, which was decided to be reviewed by the Plastic Package Subcommittee.

Upon revision of the standard, the actual reviews were made by the Plastic Package Subcommittee (the antecedent of the Semiconductor Package Standardization Committee) newly started in April, 1995 based on the positioning of the design guideline newly established in the same period. Thereafter, the final draft of the standard was approved by the Semiconductor Package Standardization Committee during the review made in March, 1996, which was established and issued as a new design guideline.

3. Background for the dimensional specifications

3.1 Basic philosophy: Considerations are made to assure the consistency with the JEDEC upon the revision of the standard, and to clarify its objectives being as the design guideline.

3.2 Background for the dimensional specifications

(1) Mounting height (A): The specification for the maximum height, A max., was changed from 1. 27 mm to 1.20 mm in view of the fact that the package will be used for the IC cards of JEIDA (Japan Electronic Industry Development Association) standard.

(2) Linear pin distance: The dimensions of 0.40 mm and 0.30 mm were added to [e] to cope with the increased number of the pins and reduced pitch.

(3) Pin widths (b) and (b1): With regard to the surface treatment of the pin, the palladium plating (hereinafter referred to as the Pd plating) was added to the conventional solder plating which was believed to increase in the future. The "b nom" specification after the surface treatment was set to the target value of 0.01 mm for the solder plating, and the same nominal width as that of the lead frame material was adopted since the plating thickness of the Pd was as small as a few micron meters.

(4) Pin thicknesses (c) and (c1): After the review, it was noted that it was difficult to standardize the nominal pin thickness due to the actual results and variety of know-how possessed among the respective manufacturers. Accordingly, only the minimum and maximum values were specified for both c and c1.

(5) Pin length (L1), soldered length (LP), and flat pin length (L): The length of 0.60 mm as recommended by the JEDEC was adopted for the LpNOM. Only the nominal values were specified for L and L1 in view of the fact that the package is designed based on the Lp dimension.

4. Members of discussion

This technical report has been discussed by the Prastic Package Subcommitee of Technical Standardization Commitee on Semiconductor Device Package and QFP project group. The members are as shown below.

<Technical Standardization Committee on Semiconductor Device Package >

Chairman :	Hisao Kasuga	NEC Corp.

<Prastic Package Subcommittee >

Chief :	Yasushi Otsuka	Sony Corp.
Sub-chief :	Masanori Yoshimoto	Fujitsu Ltd.
member :	Tsutomu Kashiwagi	ENPLAS Corp.
	Etsuo Yamada	OKI Electric Industry Co. , Ltd.
	Ahn Ki John	Samsung Electronics Japan Co., Ltd.
	Hideyuki Iwamura	SANYO Electric Co. , Ltd.
	Katsuyuki Tarui	SHARP Corp.
	Hideto Odagiri	SUMITOMO 3M Ltd.
	Akinori Hara	SEIKO EPSON Corp.
	Toshihiko Nojiri	Sony Corp.
	Toshiharu Sakurai	Toshiba , Corp.
	Kenji Kanesaka	Nippon Steel Semiconductor Corp.
	Masayuki Yoshida	IBM Japan , Ltd.
	Tsukasa Ito	AMP Japan , Ltd.
	Morio Nakao	Texas Instruments Japan Ltd.
	Koichi Takekawa	NEC Corp.
	Nobuo Sato	Nippon Motorola Ltd.
	Hideki Tanaka	Hitachi , Ltd.
	Osamu Hirohashi	Fuji Electric Co., Ltd.
	Shigeki Sakaguchi	Matsushita Electronics Corp.
	Yasuhito Suzuki	MITSUBISHI Electric Corp.
	Nanahiro Hayakawa	Yamaichi Electronics Co. , Ltd.
	Junji Ishida	Unitechno Inc.
	Hiromori Okumura	Rohm Co., Ltd.