

Technical Report of Electronic Industries Association of Japan

EIAJ EDR-7313

Design guideline of integrated circuits for Thin Small Outline Package (Type II) (TSOP(II))

Established in April, 1996

Prepared by

Technical Standardization Committee on Semiconductor Device Package

Published by

Electronic Industries Association of Japan

2-2, Marunouchi 3-chome, Chiyoda-ku, Tokyo 100, Japan Printed in Japan

EIAJ Technical Report

Design Guideline of Integrated Circuits for Thin Small Outline Package (Type II) (TSOP (II))

1. Scope of application

This technical report applies to the outline drawings and dimensions of the thin small outline packages (type II) (hereinafter referred to as the TSOP (II)) which are classified as the form B under the EIAJ ED-7401A (Basic Items Related to the Rules for the Semiconductor Package Outline (Integrated circuits and Individual Semiconductors)).

2. Terminology

The terms used in this technical report shall conform to those defined in the EIAJ ED-7401A. The new terms not included therein shall be defined in the text of this report.

3. History

The "General Rules for the Outline of the Integrated Circuit" for the thin and small outline package (type II, hereinafter referred to as the TSOP (I)) was established as EIAJ ED-7402-3 in April, 1991 in order to cope with thin electronic equipment such as the memory card. However, since the leads were provided on the shorter side of the package with the TSOP (I), it was necessary to often increase the package size due to the electrode position of the LSI chip or size. Accordingly, the TSOP (II) was required in addition to the TSOP (I) that had the different lead outlet, which was established and issued as EIAJ ED-7402-4 in December, 1991.

This design guideline aims at the standardization of the outline dimensions to the fullest extent possible and to assure the compatibility among the respective products.

4. Definition of the TSOP (I)

A package that satisfies all the following requirements; the maximum mounting height of 1.20 mm, maximum linear distance of 1.27 mm between the pins, leads extending to the two directions from the longer sides of the package, and the leads with a flat surface extending toward outside to enable the SOJ bodysize package being mounted on the surface of the printed circuit board.

5. Designation of the pin numbers

The method to designate the pin numbers shall conform to the specifications included in the EIAJ ED-7401A.

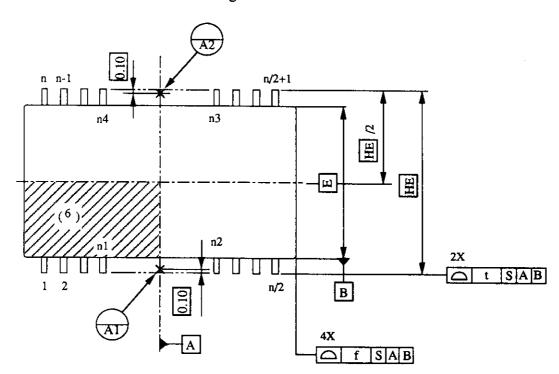
6. Nominal dimensions

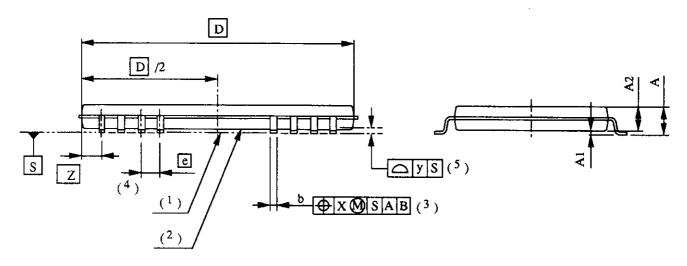
The width dimensions of the package (Reference codes: E) shall be used as the nominal dimensions in this technical report.

7. REFERENCE CHARACTERS AND DRAWINGS

7.1 Outline drawings

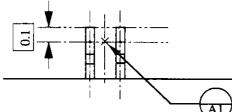
Figure 1





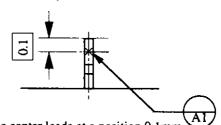
Definition of datum A

(1) For even number of leads on packafge side.



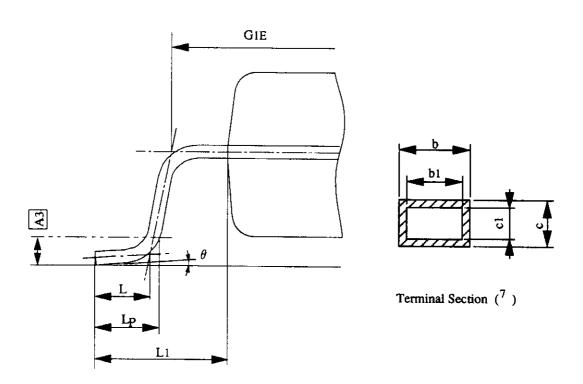
The center of facing side of adjacent leads at a position 0.1mm inside top of the leads.

(2) For odd number of leads on a package side.



The center leads at a position 0.1mm inside top of leads.

Figure 2



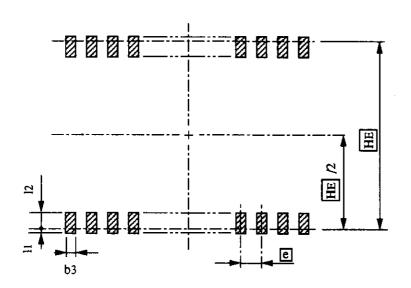
Note

- (1) The mounting surface, with which a package is in contact.
- (2) The base surface, which is in parallel with the mounting surface and links the lowest points, except the stand off.
- (3) The maximum mounting conditions apply to the positional tolerance of the terminals. (For the maximum body conditions, refer to ISO 2692/ JIS B 0023.)
- (4) Specifies the true geometric position of the terminal axis.
- (5) Specifies the vertical shift of the flat part of each terminal form the mounting surface.
- (6) Shows the allowable position of the index mark, which must be included in the shaded area entirely.
- (⁷) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

REMARKS: RANGE WHERE TERMINALS TO BE SOLDERED EXIST

The range where the terminals to be soldered can exit is shown in Figure 3 as reference for foot print design.

Figure 3



 $11 \max = t/2$

 $12 \max = Lp \max + t/2$

 $b3 \max = b \max + x$

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8. OUTER DIMENSION

8.1 Group 1

Table 1

Description	Symbol	Standard	Recomemended Values	Remarks
Nominal dimensi-ons	E	a) Soft Metric E nom = 50mil × k k = 6,7,8 E nom = 300mil 350mil 400mil b) Hard Metric E nom = 11.5 + 1.5 h h = 0,1,2,3 E nom = 0115 0130 0145 0160		Less than 400mil are applied Soft Metric package. More than 11.50mm are applied Hard Metric package.
Package width	Е	7.62 8.89 10.16 11.50 13.00 14.50 16.00		(1) Mismatch of the upper and lower dies and resin burrs are not included. (2) It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
Package length	D	a) Soft Metric D = {(N/2-1)× e } + 2ZD nom e = 1.27mm ZD nom = 0.95mm b) Hard Metric D = {(N/2-1)× e } + 2ZD nom e = 1.25mm ZD nom = 1.00mm		(1) Mismatch of the upper and lower dies and resin burrs are not included. (2) It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded. (3) Mold protrusion is less than 0.20mm.

Table 1 (Continued)

Description	Symbol	Standard	Recommended Values Remarks
Tolerance of package edge	f	(1) Tolerance of package edge shall be specified in the outline drawing. f S A B (2) The symbol f shall be replaced with any of the values shown below. f 0.20	
Package height	A2	min nom max 0.95 1.00 1.05	(1) Bend of packag is included.
Overall width	НЕ	HE = E + 2L1 nom a) Soft Metric L1 nom = 0.80 b) Hard Metric L1 nom = 1.00	
Seated height	A	min nom max 1.20	(1) Bend of packag is included.
Stand-off height	A1	min nom max 0.05 0.10 0.15	
Standard height of soldered points	A3	A3 = 0.25	
Length of soldered part	Lp	min nom max 0.45 0.60 0.75	

			T	able 1 (C	Continue	ed)				Unit mm
Description	Symbol			Stan	dard			R	Recommended Values	Remarks
		a) Soft Me 1.27 1.00 0.80 0.65 0.50	min 0.35 0.35 0.25 0.17 0.17	nom	0.50 0.50 0.40 0.32 0.30	_	a) Soft e 1.27 1.00	b n Pb/Sn Solder plating 0.42 0.42	0.40 0.40	 (1) b1 denotes the material width of a lead frame. (2) b denotes the width of a plated terminal. (3) b1 and b apply to the ranges of 0.1 and 0.25 from the end of a
Terminal width	ъ	b) Hard M			0.50	_	0.80 0.65 0.50	0.32 0.24 0.22	0.30 0.22 0.20	terminal. (4) Values b apply to Pb/Sn solder plated terminal. The standard
		1.25 1.00 0.80	min 0.35 0.35 0.25	nom	0.50 0.50 0.40	-	e	b r Pb/Sn Solder	Pd	thickness of the solder layer shall be 0.010+0.010 -0.005
		0.65 0.50	0.23 0.17 0.17		0.40 0.32 0.30	_	1.25 1.00 0.80 0.65 0.50	0.42 0.42 0.32 0.24 0.22	0.40 0.40 0.30 0.22 0.20	(5) As Pd platig, it is very thin so terminal width is bnom=blnom
Terminal		a) Soft Mer e 1.27 1.00 0.80 0.65 0.50	min 0.35 0.35 0.25 0.17	0.4 0.4 0.2	40 30 22	max 0.45 0.45 0.35 0.27 0.23	-			
width	bl	b) Hard M	etric min 0.35	\rightarrow		max 0.45	-		••••	
; ;		1.00 0.80 0.65 0.50	0.35 0.35 0.25 0.17 0.17	0.4 0.2 0.2	40 30 22	0.45 0.45 0.35 0.27 0.23	_			
										[

Table 1 (Continued)

Description	Symbol			Standard		Recommended Values	Remarks	
		a) Soft Met	ric				/4\	
		е	min	nom	max	(1) Pb/Sn Solder	(1) c1 denotes the material width	
		1.27	0.09		0.20	plating	of a lead frame.	
		1.00	0.09		0.20	c nom	(2) c denotes the	
		0.80	0.09		0.20	= 0.170	width of a plated	
		0.65	0.09		0.20	0.145 0.120	terminal.	
		0.50	0.09		0.20	0.120	(3) c1 and c apply to the ranges of	
	С	b) Hard Me	etric			(2) Pd plating	0.1 and 0.25 from the end of a	
		е	min	nom	max	с пот	terminal. (4) Values c apply	
		1.25	0.09		0.20	= c1 nom	to Pb/Sn solder	
		1.00	0.09		0.20		plated terminal.	
		0.80	0.09		0.20		The standard thickness of the	
		0.65	0.09		0.20		solder layer shall	
		0.50	0.09		0.20		be	
Terminal thickness		a) Soft Metr	ic			0.010+0.010 -0.005 c1 nom (5) As Pd platig,		
	c1		min	nom	max	c1 nom = 0.15	is very thin so terminal width is	
				nom		0.125	Cnom = Clnom	
		1.27	0.09		0.16	0.10	chom – crhom	
		1.00	0.09		0.16			
		0.80	0.09		0.16			
		0.65	0.09		0.16			
		0.50	0.09		0.16			
		b) Hard Me	tric	,	 			
		e	min	nom	max			
		1.25	0.09		0.16			
		1.00	0.09		0.16			
		0.80	0.09		0.16			
		0.65	0.09		0.16			
		0.50	0.09		0.16			
Angle of erminal flat portions			nin	nom				
	θ		0°	3°	max 8°			
					0			
		May be sele			•			
		a) Soft M	etric	b) 1	Hard Metric			
Terminal	е	e =	1.27		e = 1.25			
pitch			1.00		1.00			
			0.80		0.80			
			0.65		0.65			
1			0.50		0.50			

Table 1 (Continued)

Description	Symbol			Standa	Recommended Values	Unit mm Remarks				
_ 50011PHO11										
		a) Soft Metric b) Hard Metric						(1) The concept of the maximum		
		e	х		e		x		mounting	
Tolerance of terminal	v	1.27	0.25		1.2	.5	0.25		condition (MMC) shall be applied.	
center	X	1.00	0.20		1.0	I .	0.20		onan or approor	
position		0.80	0.16	,	0.8	- 1	0.16			
		0.65	0.13		0.6	5 (0.13			
,		0.50	0.10	<u> </u>	0.5	0 (0.10			
		a) Soft Metri	c	b) Hard N	letri c				
		e	у			e	y			
Coplanarity	v	1.27			1.:	25	0.10			
Cobiananth	y	1.00		•		00	0.10			
		0.80	0.10	D .	0.3	80	0.10			
		0.65			0.0	65	0.10			
		0.50			0.5	50	0.08			
Positional tolerance of terminal tips	t .	(2) The chara	t S A B (2) The character x shall be replaced with any of the values shown below. t 0.20							
	a) Soft Metric		c						The number of	
						е				terminals are set as
		D	1.27	1.00	0.80	0.65	0.50		follows:	
		10.79	16	20	26	32	40		e = 1.27	
		12.06	18	24	28	36	46		The maximum	
		13.33	20	26	32	38	50		number of termina	
Canadand		14.60	22	28	36	42	56		on assumption tha	
Standard number of	n	15.87	24	30	38	46	60		$\boxed{Z} = 0.95$	
terminal	11	17.14	26	34	42	50	66			
		18.41	28	36	44	54	70		e = 1.00/0.80	
		19.68	30	38	48	58	76		0.65/0.50	
		20.95	32	40	50	62	80			
		22.22	34	44	54	66	86		The maximum	
		23.49	36	46	58	70	90		number of termina	
		24.76	38 40	48	60	74	96		on assumption that $Z = 0.50$	
		26.03 27.30	40 42	52 54	64 66	78 82	102 106		<u> </u>	
		28.57	42 44	56 56	70	82	112			
t t		20.37	7*	J J U	/	00	1.14	1		

Table 2 (Continued)

Description	Symbol			Standa	rd			Recommended Values	Remarks	
		b) Hard Metric								The nominal body overhang must be:
	:			Теп	ninal Pite	ch				
		D	1.25	1.00	0.80	0.65	0.50		$e = 1.25$ $Z = 1.00$ $e = 1.00$ $Z \ge 0.80$	
		13.25		T	1				e = 0.80 Z≥0.65	
		14.50	20 22	24 26	30 34	38	50		e = 0.65 Z≥0.50	
		15.75	24	30	38	42 46	56 60		0.50	
		17.00	26	32	40	50	66			
Standard		18.25	28	34	44	54	70			
number of	n	19.50	30	36	46	58	76			
terminal		20.75	32	40	50	62	80			
		22.00	34	42	52	66	86			
		23.25	36	40	56	70	90			
		24.50	38	46	60	74	96			
		25.75	40	50	62	78	100			
		27.00	42	52	66	82	106			
	}	28.25	44	54	68	84	110			
		29.50	46	56	72	88	116			
		30.75	48	60	74	92	120			
				•			•			

2. Group 2

Table 2 (Continued)

Description	Symbol	Standard		Recommended Values	Remarks
Width between first bent part of terminal	G1E	a) Soft Metric L1 nom			(1) Used for designing a test socket, tray, etc
Package over hang	Z	Z = (D - (n/2 - 1))	×[e])/2		(1) Resin burrs or residual gates are not included.
Length of flat part of terminal	L	min nom 0.50	max		
Terminal length	L1	a) Soft Metric min nom 0.80 b) Hard Metric min nom 1.00	max		

9. Individual standard

The format for the individual standard is shown below. The format shown below shall be used when a TSOP (I) package is to be proposed, established, or issued as an individual standard.

Seria	l Nuber							
External Type.		TSOP(II) XXX - P - XXXX - X.XX						
External Type. Reference Symbol		min	nom	max				
	E		✓					
	A2	<u> </u>	V	V				
	f			V				
	HE		✓					
	Α			V				
	A1	V	✓	V				
	A3		✓					
	Lp	✓		✓				
	b	✓		V				
_	b1	✓	V	V				
ď.	С	✓		V				
Group 1	cl	✓		V				
	θ	V	✓	V				
	е		V					
	х			V				
	у			V				
	t			V				
	n		V					
	n1		V					
	n2	W a ng and the control of the contro	✓					
	n3		V V					
	n4		✓					
	G1E		V					
up 2	Z		✓					
Group 2	L							
	LI		✓					

Explanatory notes

1. Purpose of establishment

This technical report is established to show the design guideline when developing the industry norms and related parts for the thin small outline package type (II) (hereinafter referred to as the TSOP (II)), which is a revision of the EIAJ ED-7402-4A.

2. History of the review

EIAJ ED-7402-3 has been standardized and being used for the thin and small outline package (type I) (hereinafter referred to as the TSOP (I)) for the outline of the integrated circuits to cope with thin electronic equipment such as the memory card. However, the needs for the TSOP (II) arose due to the popularization of the memory card for which it was difficult to cope with the TSOP (I).

Accordingly, a proposal to standardize the TSOP (II) was made at the first Semiconductor Outline Committee (the antecedent of the Semiconductor Package Special Committee) meeting held in 198 9, and a decision was made at the same meeting to included it in the business plan for the year. As the result, a draft for the general rules was submitted by the secretary company at the second Committee meeting to commence the review thereof.

In addition, the basic dimensions, including the adoption of the nominal width as the package width, were decided in addition to the approval of the basic philosophy at the same Committee meeting.

After the reviews stated above, the final draft was approved by the ninth Semiconductor Outline Committee meeting held in 1989, which was later established and issued as the EIAJ ED-7402-4.

Thereafter, however, it was pointed out at the second Semiconductor Package Special Committee (the antecedent of Plastic Package Subcommittee) that the EIAJ ED-7402-4 established in February, 1990 was not sufficient due to the expansion in the TSOP (II) products. Accordingly, the draft was reviewed and discussed by the Plastic Package Subcommittee (the antecedent of the Plastic Package Subcommittee) meeting, approved by the ninth Semiconductor Package Special Committee meeting held in December, 1991, and issued as the EIAJ ED-7402-4A. However, since the inconsistency between the standard and the general rules became notable due to the diversifications and increased demands for the package, a proposal was made to review the standard at the seventeenth Semiconductor Package Special Committee meeting, which was decided to be reviewed by the Plastic Package Subcommittee.

Upon revision of the standard, the actual reviews were made by the Plastic Package Subcommittee (the antecedent of the Semiconductor Package Standardization Committee) newly started in April, 1995 based on the positioning of the design guideline newly established in the same period. Thereafter, the final draft of the standard was approved by the Semiconductor Package Standardization Committee during the review made in March, 1996, which was established and issued as a new design guideline.

3. Background for the dimensional specifications

3.1 Basic philosophy: Considerations are made to assure the consistency with the JEDEC upon the revision of the standard, and to clarify its objectives being as the design guideline.

3.2 Dimensional background

- (1) Nominal dimension and package width (E): These dimensions were decided based on the SOJ package which is compatible as the memory package. At the EIA/EIAJ/JWG2 (the technical association conference with the JEDEC) held at Kobe in May, 1993, a proposal was made by the JEDEC to adopt the hard metric group (0 or 5 at the second digit after the decimal point) as the package width for the SOJ packages. After the repeated reviews made by the EIAJ, a decision was made to adopt the hard metric group for the packages exceeding 400 mils in the width during the EIA/EIAJ task force meeting held at San Francisco in November. Then, the EIAJ made a proposal to lineup the TSOP (II) in the same philosophy as that of the SOJ at the EIA/EIAJ/JWG2 (San Diego conference) held in June, 1995, which was approved at the conference. Accordingly, the soft metric group (millimeter value converted from the inch value) is conventionally specified for the packages up to 400 mils in width and the hard metric group for those with the width of greater than 400 mils.
- (2) Package length (D) and (D1): The package length (D) is calculated in order to cope with the fixed body and variable pitch. The calculation is made either using e = 1.27 mm as the datum for the soft metric group or e = 1.25 mm for the hard metric group which was decided at the above mentioned conference.
- (3) Mounting height (A): The specification for the maximum mounting height was changed from 1. 27 mm to 1.20 mm in view of the fact that the package is also used for the IC cards of JEIDA (Japan Electronic Industry Development Association) standard.
- (4) Linear pin distance: e = 0.50 mm was added to cope with the increased pin quantity. In addition, the linear pin distance of e = 1.25 mm was adopted in place of e = 1.27 mm for the hard metric group.
- (5) Pin widths (b) and (b1): With regard to the surface treatment of the pin, the palladium plating (hereinafter referred to as the Pd plating) was added to the conventional solder plating which was believed to increase in the future. The "b nom" specification after the surface treatment was set to the target value of 0.01 mm for the solder plating, and the same nominal width as that of the lead frame material was adopted since the plating thickness of the Pd was as small as a few micron meters.
- (6) Pin thicknesses (c) and (c1): After the review, it was noted that it was difficult to standardize the nominal pin thickness due to the actual results and variety of know-how possessed among the respective manufacturers. Accordingly, only the minimum and maximum values were specified for both c and c1.
- (7) Pin length (L1), soldered length (LP), and flat pin length (L): The nominal dimension L1 of 1.0 0 mm was adopted for the hard metric group in view of the solderability to the board. The nominal Lp dimension of 0.60 mm was adopted which was recommended by the JEDEC. Only the nominal values were specified for L and L1 in view of the fact that the package is designed based on the Lp dimension.

4. Members of discussion

This technical report has been discussed by the Prastic Package Subcommittee of Technical Standardization Committee on Semiconductor Device Package and QFP project group. The members are as shown below.

< Technical Standardization Committee on Semiconductor Device Package >

Chairman: Hisao Kasuga NEC Corp.

< Prastic Package Subcommittee >

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Ahn Ki John Samsung Electronics Japan Co., Ltd.

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