EIAJ EDR-7316A

JEITA

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EIAJ EDR-7316A

Design guideline of integrated circuits for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (FBGA / FLGA)

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EIAJ EDR-7316A

Provisional Standard of Electronic Industries Association of Japan

Design guideline of integrated circuits for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (FBGA/FLGA)

1. Scope of Application

This standard provides for the common outline drawings and dimensions for all types of structure and composed materials of Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array(hereinafter called FBGA and FLGA) which terminal pitch is less than and equal to 0.80mm, which packages are classified as Form-D in **EIAJ ED-7300**. (Manual for the preparation of outline drawings of Package).

2. Definition of the Technical Terms

The definition of the technical terms used in this design guideline is in conformity with **EIAJ ED-7300**, and the definition of technical terms appearing a new are given within the text of this design guideline.

(1) Flanged Type

The type that package body size (Body length and width) consists of own flange that is composed around Chip.

(2) Type of Real Chip Size

The type that package body size (Body length and width) consists of own Chip size.

3. Background

In recent years, the demand for rectangular area array style packages has been increasing according to Multi function and High performance of electrical equipments. The objective of this Design-guide is to standardize Outline and to get interchangeability of rectangular FBGA and rectangular FLGA.

4. Definition of Package

4.1 Definition of FBGA and FLGA

In the packages in which the metal Balls or metal Bumps or metal Lands are positioned in an array on Base plane of the package as the external terminals, making it possible to surface mount to the printed circuit board, the packages with metal Balls which terminal pitch is less than and equal to 0.80mm is defined as FBGA, and the packages with metal Bumps which terminal height is less than and equal to 0.1mm or metal Lands and which terminal pitch is less than and equal to 0.80mm is defined as FLGA.

4.2 Definition of material designation

FBGA and FLGA packages are classified according to the following two Material designations.

(1) Plastic type (P-FBGA, P-FLGA)

Plastic type is classified to Packages that consist of printed circuit board.

(2) Tape type (T-FBGA, T-FLGA)

Tape type is classified to Packages that consist of tape substrate.

(3) Ceramic type (C-FBGA, C-FLGA)

Ceramic type is classified to Packages that consist of Ceramic substrate.

5. Numbering of the Pins

The index is positioned at the lower left corner of the package body when it is viewed from the seating plane. A row that is the closest to the index corner is named, A, and as the row moves further away from the index the rows are named, B, C, ... AA, AB, ... Also, a column that is the closest to the index corner is numbered 1, and as the column moves further away to the right, they are numbered 2, 3,.....

The terminals of FBGA and FLGA are named by these combinations A1, B1,..... In naming the rows, the letters I, O, Q, S, X, and Z should not be used.

6. Definition of Package length and width

The index is positioned at the lower left corner of the package body when it is viewed from the seating plane. A vertical direction side is classified as package length(D) and A horizontal direction side(E) is package width. Both "Length > Width" and "Width > Length" are possible.

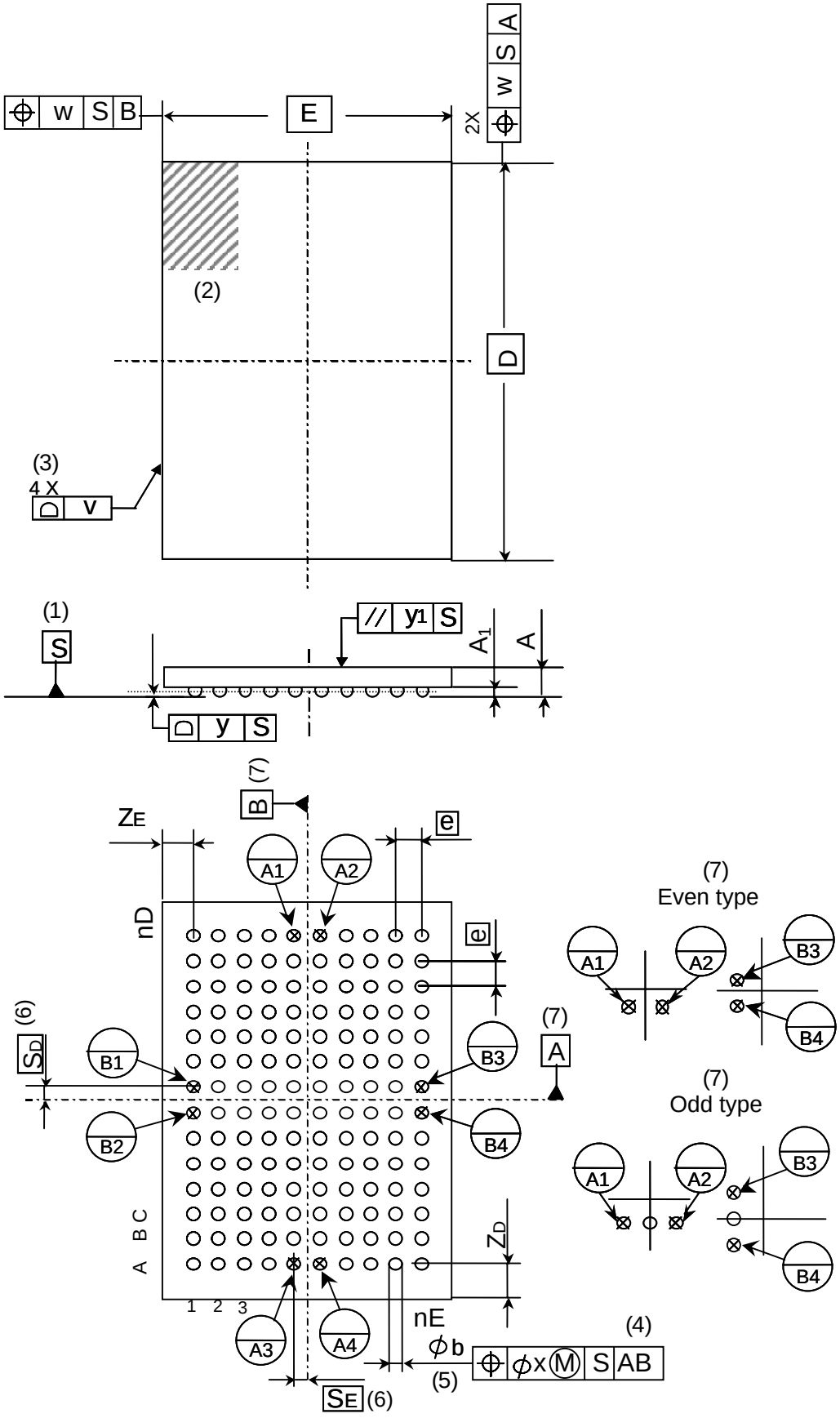
7. Nominal Dimensions

See **9.1** Group1 Nominal dimension.

8. Reference Symbols and Schematics

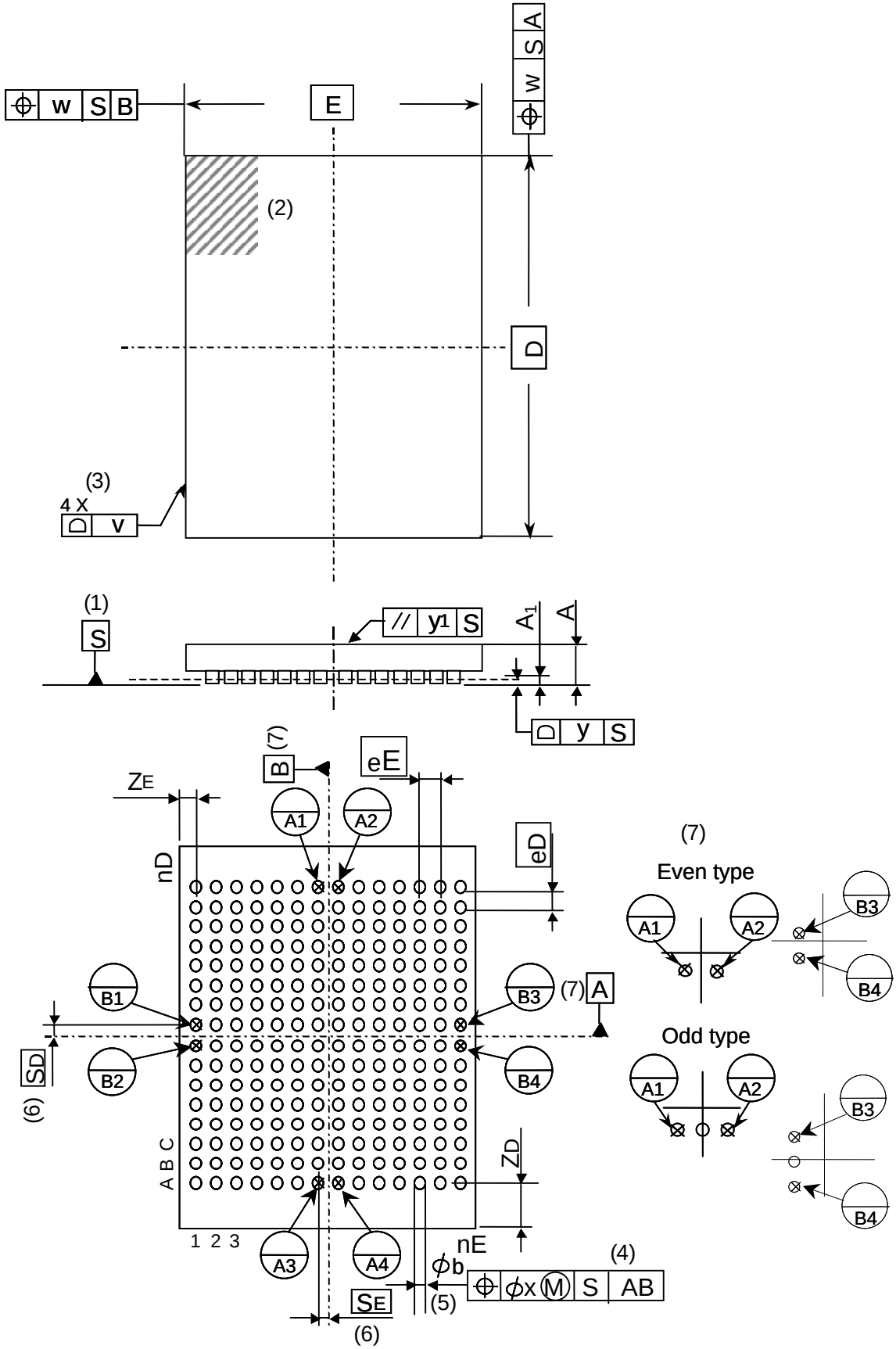
8.1 Outline drawings of FBGA

Figure 1



8.2 Outline drawings of FLGA

Figure 2



Notes: ([1]) Indicates seating plane. Seating plane is defined by the plane that the carrier contacts to the its mount surface.

([2]) Shows the allowable position of Index mark area, which is based on the IEC standard and basically 1/16 with package bodysize where corner of A1, however in case of small package bodysize, it less than 1/4 with package bodysize where corner of A1. It must be included in the shaded area entirely.

([3]) Tolelance of package lateral Profile bilateral tolerance zone (v) is applied to four sides of the package body.

([4]) The positional tolerance of terminal (x) is applied to all terminal.

([5]) Terminal diameter (b) is the maximum terminal profile.

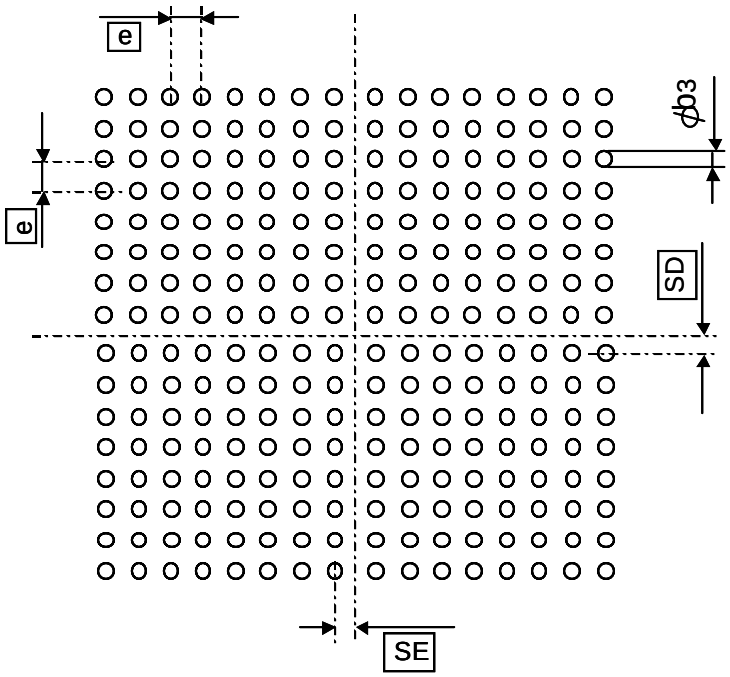
([6]) SD and SE are stipulated the position of the closest terminal with respect to datum lines A and B.

([7]) Datum A and B are the orthogonal axes defined by the centers of opposite sides of a package.

Appendix - Terminal land area:

The zone that the terminals can be projected is shown in **Figure 3.**

Figure 3



9. Overall Dimensions

9.1 Group 1

Table 1

unit:mm

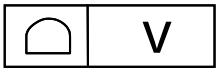
Name	Reference Symbol	Stipulation	Recommended value	Supplement
Nominal dimension	D X E	**(1) Flanged Type** Combination of one digit below decimal point of package width E and package length D is regarded as Nominal dimension. **(2) Type of Real Chip Size** Combination of two digits below decimal point of package width E and package length D is regarded as Nominal dimension.	-	-
Package length	D	**(1) Flanged Type** Package length: Dnom 0.50 carving from 1.50 to 21.00 However, in case of square type (D=E), 0.50 carving from 1.50 to 14.00 1.00 carving from 15.00to 21.00 **(2) Type of Real Chip Size** Package length: Dnom Minimum is 1.50. Maximum is 21.00.	-	-
Package width	E	**(1) Flanged Type** Package length: Enom 0.50 carving from 1.50 to 21.00 However, in case of square type (D=E), 0.50 carving from 1.50 to 14.00 1.00 carving from 15.00 to 21.00 **(2) Type of Real Chip Size** Package length: Enom Minimum is 1.50. Maximum is 21.00.	-	-
Tolerance of package lateral profile	v	**(1)** Tolelance of package lateral profile shall be specified in the outline drawing.  **(2)** Reference symbol "v" shall be replaced as below. v = 0.15	-	(1) Include burrs

Table 1 (continued)

unit:mm

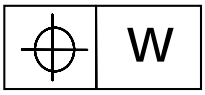
<table>
<tr><th>Name</th><th>Reference Symbol</th><th>Stipulation</th><th>Recommended value</th><th>Supplement</th></tr>
<tr><td>Package center offset</td><td>w</td><td>(1) Package center offset shall be specified in the outline drawing.
 
(2) Reference symbol "w" shall be replaced as below.
<table><tr><th>e</th><th>w</th></tr><tr><td>0.80</td><td>0.20</td></tr><tr><td>0.65</td><td>0.20</td></tr><tr><td>0.50</td><td>0.20</td></tr><tr><td>0.40</td><td>0.15</td></tr></table></td><td>-</td><td>The valve is derived from the manufacturing ability of the suppliers.</td></tr>
<tr><td>Mounting height</td><td>A</td><td><table><tr><th></th><th>$A_{max.}$</th></tr><tr><td>XFBGA/XFLGA</td><td>0.50</td></tr><tr><td>UFBGA/UFLGA</td><td>0.65</td></tr><tr><td>WFBGA/WFLGA</td><td>0.80</td></tr><tr><td>VFBGA/VFLGA</td><td>1.00</td></tr><tr><td>TFBGA/TFLGA</td><td>1.20</td></tr><tr><td>LFBGA/LFLGA</td><td>1.70</td></tr><tr><td>FBGA/FLGA</td><td>2.00</td></tr></table></td><td>-</td><td>(1) Include heat slug
(2) Include Package warpage and tilt</td></tr>
<tr><td>Stand-off height</td><td>A_1</td><td>(1) FBGA
<table><tr><th>e</th><th>$b_{nom.}$</th><th>$A_{1min.}$</th><th>$A_{1nom.}$</th><th>$A_{1max.}$</th></tr><tr><td>0.80</td><td>0.50</td><td>0.35</td><td>0.40</td><td>0.45</td></tr><tr><td></td><td>0.45</td><td>0.30</td><td>0.35</td><td>0.40</td></tr><tr><td>0.65</td><td>0.40</td><td>0.28</td><td>0.33</td><td>0.38</td></tr><tr><td>0.50</td><td>0.30</td><td>0.20</td><td>0.25</td><td>0.30</td></tr><tr><td>0.40</td><td>0.25</td><td>0.15</td><td>0.20</td><td>0.25</td></tr></table>(2) FLGA
$A_{1max.}$=0.10</td><td>-</td><td>-</td></tr>
<tr><td>Terminal pitch</td><td>e</td><td>e = 0.80
0.65
0.50
0.40</td><td>-</td><td>-</td></tr>
</table>

Table 1 (continued)

unit:mm

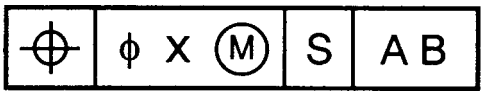
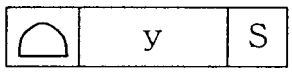
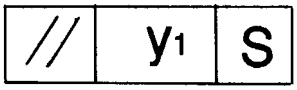
<table>
<tr><th>Name</th><th>Reference Symbol</th><th>Stipulation</th><th>Recommended value</th><th>Supplement</th></tr>
<tr><td>Terminal diameter</td><td>b</td><td>(1) FBGA
<table><tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr><tr><td>0.80</td><td>0.45</td><td>0.50</td><td>0.55</td></tr><tr><td></td><td>0.40</td><td>0.45</td><td>0.50</td></tr><tr><td>0.65</td><td>0.35</td><td>0.40</td><td>0.45</td></tr><tr><td>0.50</td><td>0.25</td><td>0.30</td><td>0.35</td></tr><tr><td>0.40</td><td>0.20</td><td>0.25</td><td>0.30</td></tr></table>(2) C-FLGA
<table><tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr><tr><td>0.80</td><td>0.45</td><td>0.50</td><td>0.55</td></tr><tr><td>0.65</td><td>0.35</td><td>0.40</td><td>0.45</td></tr><tr><td>0.50</td><td>0.25</td><td>0.30</td><td>0.35</td></tr><tr><td>0.40</td><td>0.20</td><td>0.25</td><td>0.30</td></tr></table>(3) P-FLGA
<table><tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr><tr><td>0.80</td><td>0.35</td><td>0.40</td><td>0.45</td></tr><tr><td>0.65</td><td>0.28</td><td>0.33</td><td>0.38</td></tr><tr><td>0.50</td><td>0.20</td><td>0.25</td><td>0.30</td></tr><tr><td>0.40</td><td>0.15</td><td>0.20</td><td>0.25</td></tr></table></td><td><table><tr><th>e</th><th>$b_{nom.}$</th></tr><tr><td>0.80</td><td>0.50</td></tr><tr><td>0.65</td><td>0.40</td></tr><tr><td>0.50</td><td>0.30</td></tr><tr><td>0.40</td><td>0.25</td></tr></table>-
-</td><td>-
-</td></tr>
<tr><td>Positional tolerance of terminal</td><td>x</td><td>(1) Positional tolerance of terminal shall be specified in the outline drawing.
 
(2) Reference symbol "x" shall be replaced as below.
<table><tr><th>e</th><th>x</th></tr><tr><td>0.80</td><td>0.08</td></tr><tr><td>0.65</td><td>0.08</td></tr><tr><td>0.50</td><td>0.05</td></tr><tr><td>0.40</td><td>0.05</td></tr></table></td><td>-</td><td>-</td></tr>
<tr><td>Terminal coplanarity</td><td>y</td><td>(1) Terminal coplanarity shall be specified in the outline drawing.
 
(2) Reference symbol "y" shall be replaced as below.
<table><tr><th>e</th><th>y</th></tr><tr><td>0.80</td><td>0.10</td></tr><tr><td>0.65</td><td>0.10</td></tr><tr><td>0.50</td><td>0.08</td></tr><tr><td>0.40</td><td>0.08</td></tr></table></td><td>-</td><td>-</td></tr>
</table>

Table 1 (continued)

unit:mm

Name	Reference Symbol	Stipulation	Recommended value	Supplement
Parallelism of package top surface	y_1	(1) Parallelism of package top surface shall be specified in the outline drawing.  (2) Reference symbol "y_1" shall be replaced as below. $y_1 = 0.20$	-	-
Center terminal position in D-direction	S_D	SD When MD is an odd number $S_D = 0$ When MD is an even number $S_D = e/2$	-	-
Center terminal position in E-direction	S_E	When ME is an odd number $S_E = 0$ When ME is an even number $S_E = e/2$	-	-
Terminal array		Terminal positions are designated by Terminal pitch e, Matrix size MD, ME, and Center terminal positions S_D, S_E	-	-
Number of Terminals	n	(1) FBGA/FLGA n max. = M_E max x M_D max M_E max - 1 x M_D max M_E max x M_D max –1 M_E max - 1 x M_D max –1 See **Table 3** for FBGA/FLGA. (2) FLGA n max. = M_E max +1 x M_D max M_E max x M_D max +1 M_E max +1 x M_D max +1 See **Table 3** for FLGA	-	“n” is "M_E , M_D” in the table.
Matrix size in D-direction	M_D			
Matrix size in E-direction	M_E			

9.2 Group 2

Table 2

unit:mm

Name	Reference Symbol	Stipulation	Recommended value	Supplement
Overhang in D-direction	Z_D	$Z_D = \{D_{nom.} - (M_D - 1) \times e\}/2$	-	-
Overhang in E-direction	Z_E	$Z_E = \{E_{nom.} - (M_E - 1) \times e\}/2$	-	-
Terminal diameter on terminal land area	b_3	$b_3 = b_{max.}+x$	-	-

Table 3 Compile table of D/E, M_D /M_E, n max Combination

Table 3-1 e = 0.80mm pitch FBGA/FLGA

D or E		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (For FLGA)
Flanged Type	Real Chip Size Type			
1.50	1.50~1.98	-	-	2
2.00	1.99~2.78	2	-	3
2.50				
3.00	2.79~3.58	3	2	4
3.50				
4.00	3.59~4.38	4	3	5
4.50	4.39~5.18	5	4	6
5.00				
5.50	5.19~5.98	6	5	7
6.00	5.99~6.78	7	6	8
6.50				
7.00	6.79~7.58	8	7	9
7.50				
8.00	7.59~8.38	9	8	10
8.50	8.39~9.18	10	9	11
9.00				
9.50	9.19~9.98	11	10	12
10.00	9.99~10.78	12	11	13
10.50				
11.00	10.79~11.58	13	12	14
11.50				
12.00	11.59~12.38	14	13	15
12.50	12.39~13.18	15	14	16
13.00				
13.50	13.19~13.98	16	15	17
14.00	13.99~14.78	17	16	18
14.50				
15.00	14.79~15.58	18	17	19
15.50				
16.00	15.59~16.38	19	18	20
16.50	16.39~17.18	20	19	21
17.00				
17.50	17.19~17.98	21	20	22
18.00	17.99~18.78	22	21	23
18.50				
19.00	18.79~19.58	23	22	24
19.50				
20.00	19.59~20.38	24	23	25
20.50	20.39~21.00	25	24	26
21.00				

Table 3-2 e = 0.65mm pitch FBGA/FLGA

D or E		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (For FLGA)
Flanged Type	Real Chip Size Type			
1.50	1.50~1.73	-	-	2
2.00	1.74~2.38	2	-	3
2.50	2.39~3.03	3	2	4
3.00				
3.50	3.04~3.68	4	3	5
4.00	3.69~4.33	5	4	6
4.50	4.34~4.98	6	5	7
5.00	4.99~5.63	7	6	8
5.50				
6.00	5.64~6.28	8	7	9
6.50	6.29~6.93	9	8	10
7.00	6.94~7.58	10	9	11
7.50				
8.00	7.59~8.23	11	10	12
8.50	8.24~8.88	12	11	13
9.00	8.89~9.53	13	12	14
9.50				
10.00	9.54~10.18	14	13	15
10.50	10.19~10.83	15	14	16
11.00	10.84~11.48	16	15	17
11.50	11.49~12.13	17	16	18
12.00				
12.50	12.14~12.78	18	17	19
13.00	12.79~13.43	19	18	20
13.50	13.44~14.08	20	19	21
14.00				
14.50	14.09~14.73	21	20	22
15.00	14.74~15.38	22	21	23
15.50	15.39~16.03	23	22	24
16.00				
16.50	16.04~16.68	24	23	25
17.00	16.69~17.33	25	24	26
17.50	17.34~17.98	26	25	27
18.00	17.99~18.63	27	26	28
18.50				
19.00	18.64~19.28	28	27	29
19.50	19.29~19.93	29	28	30
20.00	19.94~20.58	30	29	31
20.50				
21.00	20.59~21.00	31	30	32

Table 3-3 e = 0.50mm pitch FBGA/FLGA

D or E		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (For FLGA)
Flanged Type	Real Chip Size Type			
1.50	1.50~1.95	2	-	3
2.00	1.96~2.45	3	2	4
2.50	2.46~2.95	4	3	5
3.00	2.96~3.45	5	4	6
3.50	3.46~3.95	6	5	7
4.00	3.96~4.45	7	6	8
4.50	4.46~4.95	8	7	9
5.00	4.96~5.45	9	8	10
5.50	5.46~5.95	10	9	11
6.00	5.96~6.45	11	10	12
6.50	6.46~6.95	12	11	13
7.00	6.96~7.45	13	12	14
7.50	7.46~7.95	14	13	15
8.00	7.96~8.45	15	14	16
8.50	8.46~8.95	16	15	17
9.00	8.96~9.45	17	16	18
9.50	9.46~9.95	18	17	19
10.00	9.96~10.45	19	18	20
10.50	10.46~10.95	20	19	21
11.00	10.96~11.45	21	20	22
11.50	11.46~11.95	22	21	23
12.00	11.96~12.45	23	22	24
12.50	12.46~12.95	24	23	25
13.00	12.96~13.45	25	24	26
13.50	13.46~13.95	26	25	27
14.00	13.96~14.45	27	26	28
14.50	14.46~14.95	28	27	29
15.00	14.96~15.45	29	28	30
15.50	15.46~15.95	30	29	31
16.00	15.96~16.45	31	30	32
16.50	16.46~16.95	32	31	33
17.00	16.96~17.45	33	32	34
17.50	17.46~17.95	34	33	35
18.00	17.96~18.45	35	34	36
18.50	18.46~18.95	36	35	37
19.00	18.96~19.45	37	36	38
19.50	19.46~19.95	38	37	39
20.00	19.96~20.45	39	38	40
20.50	20.46~20.95	40	39	41
21.00	20.96~21.00	41	40	42

Table 3-4 e = 0.40mm pitch FBGA/FLGA

D or E		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (For FLGA)
Flanged Type	Real Chip Size Type			
1.50	1.50~1.70	2	-	3
2.00	1.71~2.50	3	2	4
2.50	2.51~2.90	5	4	6
3.00	2.91~3.30	6	5	7
3.50	3.31~3.70	7	6	8
4.00	3.71~4.10	8	7	9
4.50	4.11~4.90	10	9	11
5.00	4.91~5.30	11	10	12
5.50	5.31~5.70	12	11	13
6.00	5.71~6.10	13	12	14
6.50	6.11~6.90	15	14	16
7.00	6.91~7.30	16	15	17
7.50	7.31~7.70	17	16	18
8.00	7.71~8.10	18	17	19
8.50	8.11~8.90	20	19	21
9.00	8.91~9.30	21	20	22
9.50	9.31~9.70	22	21	23
10.00	9.71~10.50	23	22	24
10.50	10.51~10.90	25	24	26
11.00	10.91~11.30	26	25	27
11.50	11.31~11.70	27	26	28
12.00	11.71~12.50	28	27	29
12.50	12.51~12.90	30	29	31
13.00	12.91~13.30	31	30	32
13.50	13.31~13.70	32	31	33
14.00	13.71~14.50	33	32	34
14.50	14.51~14.90	35	34	36
15.00	14.91~15.30	36	35	37
15.50	15.31~15.70	37	36	38
16.00	15.71~16.50	38	37	39
16.50	16.51~16.90	40	39	41
17.00	16.91~17.30	41	40	42
17.50	17.31~17.70	42	41	43
18.00	17.71~18.50	43	42	44
18.50	18.51~18.90	45	44	46
19.00	18.91~19.30	46	45	47
19.50	19.31~19.70	47	46	48
20.00	19.71~20.50	48	47	49
20.50	20.51~20.90	50	49	51
21.00	20.91~21.00	51	50	52

10. Individual Outline Drawing Standard Registration

To propose new outline for individual standard, necessary information in Form 5 of Technical Standardization committee on Semiconductor Device package administrative provisions is made an entry and proceeded by standard preparation procedure. In which time, (*) mark in the package dimension table shown below will be entered in dimensions or letters.

Table 5

	Reference Number			
	Outline Type	O– O FBGA O O O– O O. O O x O O. O O– O O. O O O– O FLGA O O O– O O. O O x O O. O O– O O. O O		
	Reference Symbol	min.	Nom.	max.
Group 1	D		*	
	E		*	
	v			*
	w			*
	A			*
	A_1	*	*	*
	e		*	
	b	*	*	*
	x			*
	y			*
	y_1			*
	n		*	
	M_D		*	
	M_E		*	
	Terminal array	* See Note below		
Group 2	S_D		*	
	S_E		*	
	Z_D		*	
	Z_E		*	
	b_3			*

Note

In "Terminal array" selection, the array types are selected from Full matrix, Staggered matrix, and peripheral X row matrix. X is natural number. For the other array placements, they will be defined or illustrated when each type is registered for individual outline drawing standard.

Comments

1. Objective of Establishment

This provisional standard is intended to provide the industrial standards for rectangular fine pitch BGA and LGA(to be called FBGA/FLGA hereinafter) and the design guidelines in developing and producing the FBGA/FLGAs and its related parts

2. Background

In early 1995, the Society for the Study of CSPs(its antecedents of the Society for the Study of Next Generational Packages) was established under the Mounting Technical Committee on Semiconductor Device Packages and had investigated CSPs, possibility of standardizing their external dimensions, and so on.

The standardization of CSPs had been proceeded at the Technical Standardization Committee on Semiconductor Device Packages based on the report from the Society for the Study of CSPs, and the furthermore investigations for its standardization have been done at Area Array Package Committee since October 1995.

Based on **EIAJ EDR-7315A** (to be called "Design guideline of BGA"), the deliberation on the square types of fine pitch BGA and LGA was done first with the object of eliminating confusion caused by no their standards as much as possible as the market needs of FBGA and FLGA were increasing rapidly and **EIAJ EDR-7316**(to be called "Design guideline of integrated circuits for FBGA/FLGA " hereinafter) was issued in April 1998 after the deliberation at the Area Array Package Committee.

In the 2nd half of 1990's, the market needs of FBGA and FLGA for memory use are raised, and the standardization of package outlines of rectangular FBGA/FLGA is required without delay. The deliberation on this had started at the Area Array Package Committee in November 1998. Its deliberation had been proceeded based on the FBGA/FLGA Design Guideline(**EIAJ EDR-7316**) with its correction and/or addition. The practical activities were completed at the Area Array Package Committee by May 1999, and the final draft of the provisional standard which was valid by March 2001 was approved by Semiconductor Package Standardization Committee, and it was issued as **EIAJ EDX-7316**. Related Committee brought forward problems of difference of these standards(**EIAJ EDR-7316, EDX-7316**). So these standards had unified and **EIAJ EDR-7316A** is published in April 2002.

3. Background of the Dimension

(1) Datum

Datum was determined by the terminals, because it was an important parameter during package mounting, especially for fine pitch packages. However, as it is necessary to get a consensus of opinion of JEDEC, datum A, B definition determined centers of opposite sides of a package is adapted.

(2) Nominal dimension

Defined as the numerical representation of the package length against the package width, considering up to one decimal place of the actual dimensions for Flanged type packages. In the case of Real chip size type packages, it is defined as the numerical representation of the package length against the package width, considering up to two decimal places of the actual dimensions, which is necessary to express the CSP concept. Also, it is defined D X E as same as JEDEC standard.

(3) Background on the revision of package length and width (D , E) definition

Based on **EIAJ EDR-7315A** " Integrated circuit design guide: Ball grid array" the vertical direction defines the package width(D), while the horizontal direction defines the package length(E), upon the condition that the package index is located on the lower left side from the package bottom view. The following two problems arose from this definition.

a) When we apply this to the trend of rectangular type BGA package in the market, statements such as " Package width is larger than the package length "will be opposed by" Package length is larger than the package width "

b) This definition of package length and package width contradicts the JEDEC design guide.

In order to avoid confusion in the industry, we opted to change the definition of the vertical direction as the package length(D) and the horizontal direction to be the package width(E) upon the condition that the package index is located on the lower left side from the package bottom view. Also, we did not define to correlate package length and package width according to size.

Since ball layout is defined in a standard, size correlation of package length and package width shall be reversed by a normal ball matrix and memory chip size.

(4) Package length and width (D , E)

Maximum size was defined to be 21mm, which is the same as in the FBGA/FLGA design guide. Minimum size was defined to be 1.5mm, which will allow possibility of further minimizing the package size.

(5) Mounting height (A)

The values of the maximum mounting height were selected from **EIAJ ED-7303B**. This technical report is added Amax=1.00, 0.80, 0.65, 0.50mm (code : V, W, U, X), newly.

(6) Stand-off height (A1)

(a) FBGA : Stand-off height (A1) was defined to express min., nom. and max. values. It was considered for socket which is used for Auto mounter and testing. The recommended nom. value is 50% ofthe package terminal pitch, which is the same as in the FBGA/FLGA design guide.

However, in the case of 0.45mm ball diameter with 0.8mm pitch, which was added as a ball diameter option, stand-off height is defined at 0.35mm.

(b) FLGA : There are two terminal type for FLGA - flat type and bump type. Stand-off height was defined to be less than 0.10mm to distinguish from FBGA package.

(7) Terminal pitch(e)

Algorithm of 80% reduction was applied as the conventional packages.

The basic pitch is 1.00mm. The other pitches defined for this design guideline are 0.80/0.65/0.50/0.40mm.

(8) Terminal diameter (b)

(a) FBGA : The preferable terminal diameter is defined as 60% of terminal pitch, the same as the design guideline of FBGA/FLGA. In the case of 0.8mm pitch, Ö 0.45mm and Ö 0.40mm were considered to add to this design guideline, because Ö 0.50mm might be difficult for manufacturing. The subcommittee decided to add Ö 0.45 mm as an option, and not to add Ö 0.40mm, after the feasibility study of routing of circuit and socket.

(b) FLGA : Basically, it provided as well as FBGA based on 60% of the pitch, however 50% of terminal pitch was applied for plastic packages. In case of the ball diameter in FBGA to be 60% of the pitch, the land diameter of the ball installation part becomes 50% of the pitch when sharing of package substrate of FBGA and FLGA, and degree of freedom of the patterning was considered. In a ceramic type, to secure temperature cycle characteristic when mounting, the size of 60% of the terminal diameter was needed, because the coefficient of linear expansion difference with the printed circuit board.

(9) Parallelism of package top surface (y_1)

Taking into account the limitation of the pick-up of the automatic mounter specified parallelism of top surface.

(10) Terminal coplanarity (y)

Considering the result discussed with subcommittee and with JEDEC, the coplanarity of the design guideline of FBGA/FLGA was adapted.

(11) Positional tolerance of terminal (x)

About 10% of terminal pitch is specified.

(12) Tolerance of package lateral profile and center offset (v, w)

The tolerance of package lateral profile v and center-offset w were specified at the same value of the design guideline of FBGA/FLGA.

(13) Stipulation for the number of terminal matrixes (M_E, M_D)

The following definition was adapted from the design guideline of FBGA/FLGA. The maximum number for terminal matrixes (hereafter referred to as maximum terminal matrixes) Mmax. ($M_D$max.and $M_E$max.) was set as an integer which satisfied the inequality noted below, and this integer was stipulated as the standard number of terminal matrixes.

$M_D max \leq (D - bmax - v - w - x - 2 (E.C.)) / e + 1$

$M_E max \leq (E - bmax - v - w - x - 2 (E.C.)) / e + 1$

D , E	: Package length and width
bmax	: Max.terminal diameter(bnom+terminal diameter tolerance)
v	: allowable value for package end
w	: allowable value for package center position
x	: allowable value for terminal position
E.C.	: Edge clearance (0.11mm)
e	: Terminal pitch

Also for D , E, the $M_D$max and $M_E$max determined as shown above, and the same figure with one row less (offset by one half-pitch), indicated that ($M_D$max -1) by ($M_E$max -1), were added to the stipulation as standard terminal matrixes. Furthermore ($M_D$max +1) by ($M_E$max +1) only for FLGA were added, if E.C. ³0 is satisfied.

(14) Background of calculation that number of terminal matrix

(a) Maximum number of terminal matrix(Mmax):

At first, Mmax is though assumed the number in the range where the terminal edge does not begin to see the package edge which can be maximum arranged. There is a demand by which the structure of the tray is assumed to be terminal non-contact to FBGA. Need the area (edge clearance) where some ball does not exist between the terminal edge and the package edge to prevent the transformation of the ball by the contact of an unexpected ball or the dropout at handling by the maker and the user. that was proposed from semiconductor packing sub-committee and **JEDEC JC-11**, and it was assumed that this was adopted. As for tolerance of package lateral profile (v), it was put in consideration to be able to do the position match in the package externals at the present stage and decided the numerical value in the user. Moreover, a permissible value of package center offset was (w) decided from the ability value in mounting.

(b) Offset by one half-pitch maximum number of terminal matrix (Mmax-1)

It provided for Mmax as a number of standard terminal matrix, also it provided for Mmax-1 as a number of standard terminal matrix as same as Mmax. The number of terminal matrix of both the even number and the odd number of all package externals provided in this design guide can be selected by providing for both Mmax and Mmax-1 as a number of standard terminal matrix.

Moreover, in case of FLGA, there was no ball. So a part of package externals was assumed to admit (Mmax+1) in the combination from being able multi array (Mmax+1) from Mmax when pitches were combined by one row about FLGA because there was no ball.

Because the array of a lot of one row was able to be done more than Mmax when pitches were combined, a part of package externals was assumed to admit (Mmax+1) in the combination.

(15) The 1 pin display

The example of the concrete way of displaying about the 1 pin display for the automatic mounting machinery to recognize the direction of the package using the terminal, the way of adding one terminal to the corner part with the most internal circumference and the way of removing one terminal of A1 and so on were thought of. However, to prescribe the index display to have standardized on and for it to have been unified didn't result in an arrangement for the following reason. There are the package, which is depopulation terminals in 4 corners already, and the package that the space, which arranges a terminal in the corner part with the most internal circumference, isn't provided for. Also, the point that the user doesn’t unify a request to the 1 pin display, too, is the reason. However, actually, in the form according to this, a 1 pin display is implemented.

(16) Package overhang (Z_E, Z_D)

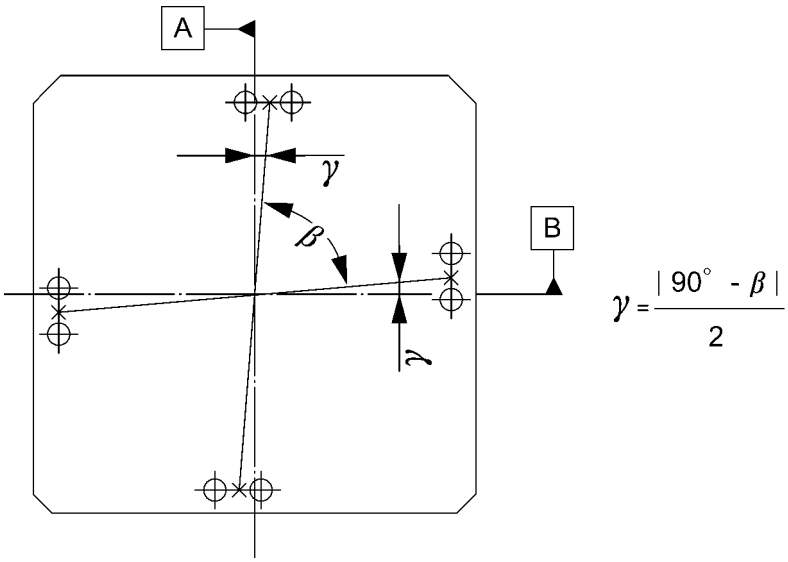
At former **EIAJ EDR-7316**, the package overhang was true geometrical position $\boxed{Z_E}$, $\boxed{Z_D}$. When there was comment from Holland that contradiction of the notation of the package outline drawing in the stage of the IEC standardization. In this technical report, it didn't make a true geometrical position notation Z_E, Z_D.

4. Datum A and B definition

So far the method for calculate the datum A and B was using ball positions. However, as it is necessary to get a consensus of opinion of JEDEC, datum A and B definition determined centers of opposite sides of a package is adapted.

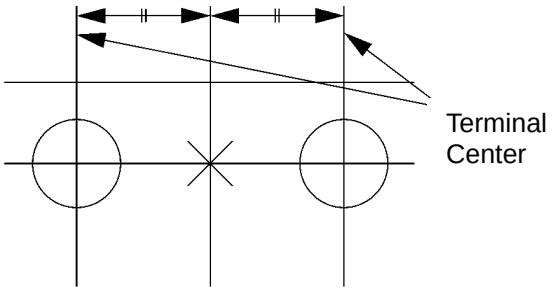
Centers of opposite sides of a package, which are defined below, shall be connected together. An angle âu subtended by the two crossing lines shall be obtained. A difference |90° -âu | of the angle âu from 90° shall be equally distributed to the sides to obtain orthogonal axes. The orthogonal axes are depicted as datum lines A and B of the package.

Explanation Figure 1

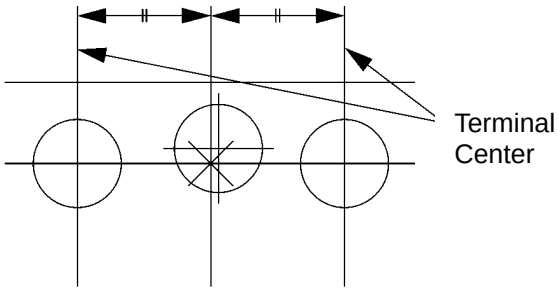


Definition of the center of sides

Explanation Figure 2 For an even number



Explanation Figure 3 For an odd number



5. Review committee members.

This technical report has been reviewed mainly by IC Package Sub-Committee and Project Group of Semiconductor Package Standardization Committee.

A detailed discussion of the standard started PJ, and executed a special committee in addition.

The members are as shown below.

<Technical Standardization Committee on Semiconductor Device Package>

Chairman	SONY CORP.	Kazuo Nishiyama

<IC Package Sub-committee>

Chief	MITSUBISHI ELECTRIC CORP.	Kazuya Fukuhara
Co- Chief	HITACHI LTD.	Yoshinori Miyaki
	FUJITSU LTD.	Hiroshi Inoue
	TOSHIBA CORP.	Yasuhiro Koshio
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	ELPIDA MEMORY, INC.	Fumitake Okutsu
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	KYOCERA CORP.	Akihiko Funahashi
	SANYO ELECTRIC CORP.	Hideyuki Iwamura
	SANYO ELECTRIC CORP.	Kiyoshi Mita
	SUMITOMO 3M CORP.	Akiko Tsubota
	SEIKO EPSON CORP.	Yoshiaki Emoto
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	NEC CORP.	Kenichi Kurihara
	NEC CORP.	Kaoru Sonobe
	IBM JAPAN, LTD.	Tsuneo Kobayashi
	TEXAS INSTRUMENTS JAPAN LTD.	Takayuki Ohuchida
	HITACHI CABLE LTD.	Tadashi Kawanobe
	FUJITSU LTD.	Kaoru Tachibana
	FUJI ELECTRIC CO., LTD.	Osamu Hirohashi
	MELCO INC.	Tsuneo Watanabe
	YAMAICHI ELECTRIC CO., LTD.	Noriyuki Matsuoka
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	MITSUBISHI ELECTRONIC CORP.	Kazuya Fukuhara
	NEC CORP.	Kaoru Sonobe
	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.	Toshiyuki Fukuda
	HITACHI LTD.	Yoshinori Miyaki