JEITA EDR-7316C

Standard of Japan Electronics and Information Technology Industries Association

Design guide for semiconductor packages Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (FBGA/FLGA)

Introduction

In order to better address increasing requirements for smaller electronics devices with higher functionality and better performances, this design guide intends to standardize the outline dimensions of FBGA and FLGA, which are reduced-pitch versions of BGA and LGA. “Wafer Level CSP” is also categorized as FBGA or FLGA with the smallest body sizes and finer terminal pitches in this design guide.

This document is intended for better design guide to the standard package outlines, providing the nominal values for all dimensions wherever possible.

1. Scope

This Design guide for semiconductor packages defines the general outline drawings, dimensions and tolerances for Fine-pitch Ball Grid Array (FBGA) packages and Fine-pitch Land Grid Array (FLGA) packages without regard to the package structures or materials. Being reduced-pitch version of Ball Grid Array (BGA) packages and Land Grid Array (LGA) packages, FBGA and FLGA are categorized as Form-D in “Recommended practice on standard for the preparation of outline drawings of semiconductor packages”, **JEITA ED-7300**, with the terminal pitch of 0.8 mm or less.

2. Normative references

JEITA ED-7300 Recommended practice on standard for the preparation of outline drawings of semiconductor packages

JEITA ED-7302 Manual for integrated circuits package design guide

JEITA ED-7303 Name and code for integrated circuits package

3. Terminology

General terminology complies with **JEITA ED-7300**, while specific terminology is defined in section **4.** and the following sections.

4. Definition of package

4.1. Definition of FBGA and FLGA

Among packages whose each bottom contains an array pattern of metal balls, bumps, or lands that function as outer terminals and enables surface mount on the printed wiring board, the packages whose terminal pitch is 0.8 mm or less and the stand-off height of the metal balls is more than 0.1 mm are referred to as FBGA, and the packages whose terminal pitches are 0.8 mm or less and the stand-off heights of the metal bumps or lands are 0.1 mm or lower are referred to as FLGA.

4.2. Definition of package structures

(1) Flanged Type

A package whose body size (package length and width) is defined by the package component which extends outward beyond the perimeter of the die forming a flange is referred to as a “Flanged type”. (There are two Flanged Types; one is literally flanged around the plastic cap and the other is separated by dicing the package and its body size is determined simultaneously.

The standard was classified with Level 1 and Level 2 according to the customer demand.

The latter has body dimensions with tighter tolerances; therefore, dimension tolerances are categorized to Level 1 and Level 2 and specified in this design guide.)

(2) Real Chip-Size Type

A package whose body size (package length and width) is defined to coincide as closely as possible with a specific die size is referred to as a “real chip-size type”. Future change in die size will result in the alteration of body size.

(3) Wafer Level Chip-Size Package (Wafer Level CSP)

A real chip-size type FBGA or FLGA whose traces are re-routed from the die pads to the on-chip area array footprints for package terminals in a wafer fabrication process is referred to as “Wafer Level CSP”.

5. Terminal position numbering

When a package is viewed from the terminal side with the index corner in the bottom left corner position, terminal rows are lettered from bottom to top starting with A, then B, C…, AA, AB, etc., while terminal columns are numbered from left to right starting with 1. Terminal positions are designated by a row-column grid system and shown as alphanumeric identification, e.g., A1, B1, or AC34.

The letters I, O, Q, S, X and Z are not used for naming the terminal rows.

6. Definitions of package length and width

When a package is viewed from the terminal side with the index corner in the bottom left corner position, body size in the vertical direction is designated “package length (D)” and one in the horizontal direction is designated “package width (E)” without regard to the relation of the dimension.

7. Code of package nominal dimension

See **Table 1** in section **10.1**.

8. Package types and its terminal pitch

Package type		Flanged type						Real chip-size type (WLCSP)						
		FBGA			FLGA			FBGA			FLGA			
Material		P	T	C	P	T	C	P	T	C	S	P	T	C
Pitch	0.4-0.8	○	○	○	○	○	○	○	○	○	○	○	○	○
	0.3	○	○		○			○			WLCSP	○		
	0.25										WLCSP			

9. Symbols and drawings

9.1 FBGA outline

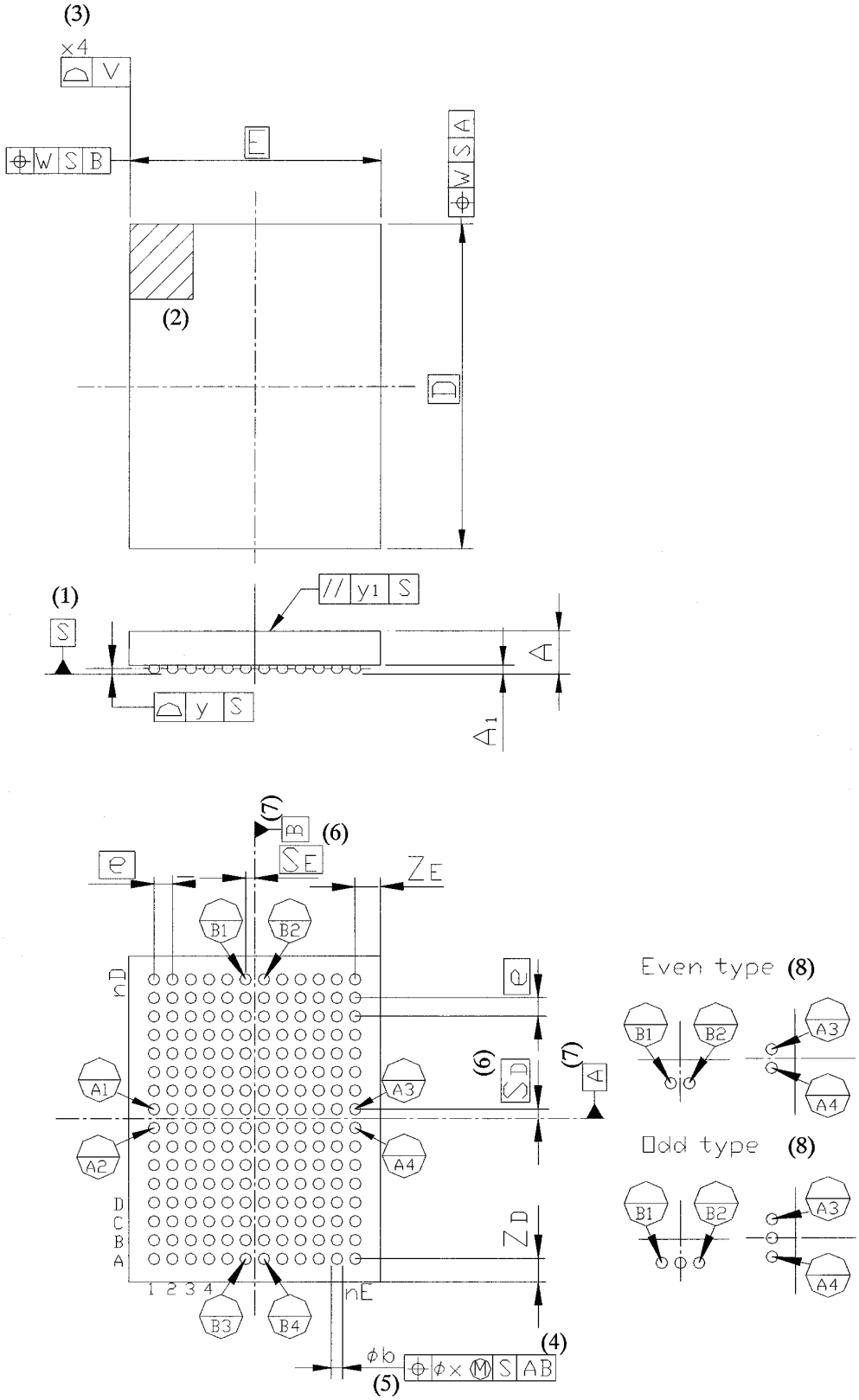


Figure 1

9.2 FLGA outline

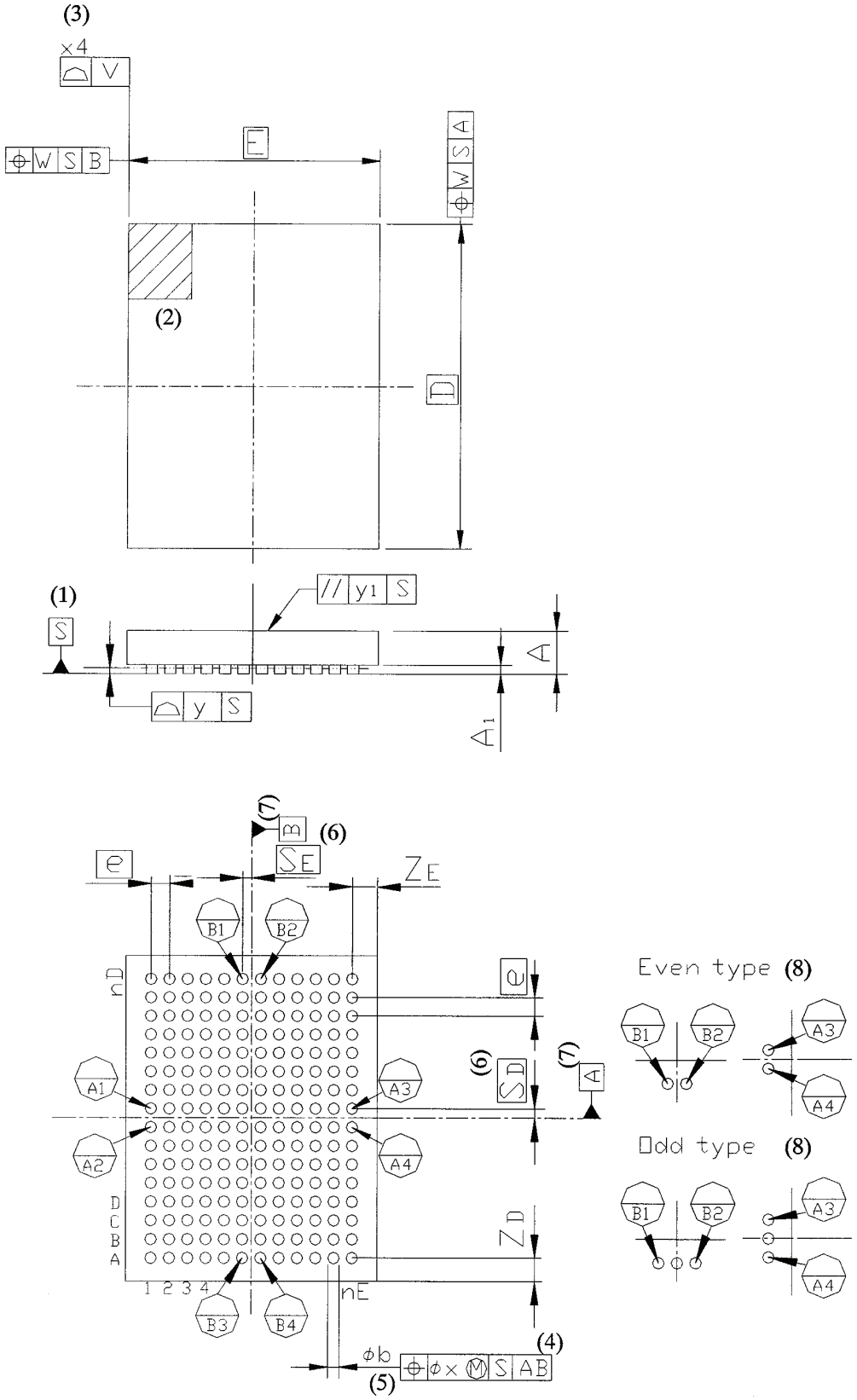


Figure 2

Notes ([1]): Datum $\boxed{S}$ is defined as the seating plane on which a package is placed.

([2]): The hatched zone indicates the index-marking area. The terminal A1 corner must be identified on the top surface of the package by using a distinguishing feature. The index-marking area is basically 1/16 of the package body area in compliance with **IEC** rule. Even a small package, of which 1/16 body area is not sufficient to contain whole identification mark, will have the mark within a quarter of the top surface.

([3]): Ranges of package length D and package width E are specified as $\boxed{D}$ +/-v and $\boxed{E}$ +/-v, respectively.

([4]): True position tolerance of terminal “x” is applied to all terminals.

([5]): The terminal diameter “b” is the maximum diameter of individual ball as measured in a plane parallel to the seating plane.

([6]): $\boxed{S_D}$ and $\boxed{S_E}$ are the dimensions which define the positions of balls next to the datum $\boxed{A}$ and datum $\boxed{B}$.

([7]): Definitions of datum $\boxed{A}$ and datum $\boxed{B}$ are described in the section of **Explanation**.

([8]): Datum $\boxed{A}$ is defined by the positions of terminals A1, A2, A3 and A4, while datum $\boxed{B}$ is defined by the positions of terminals, B1, B2, B3 and B4.

Remarks: An array of possible terminal zones including true position tolerances is shown in **Figure 3**.

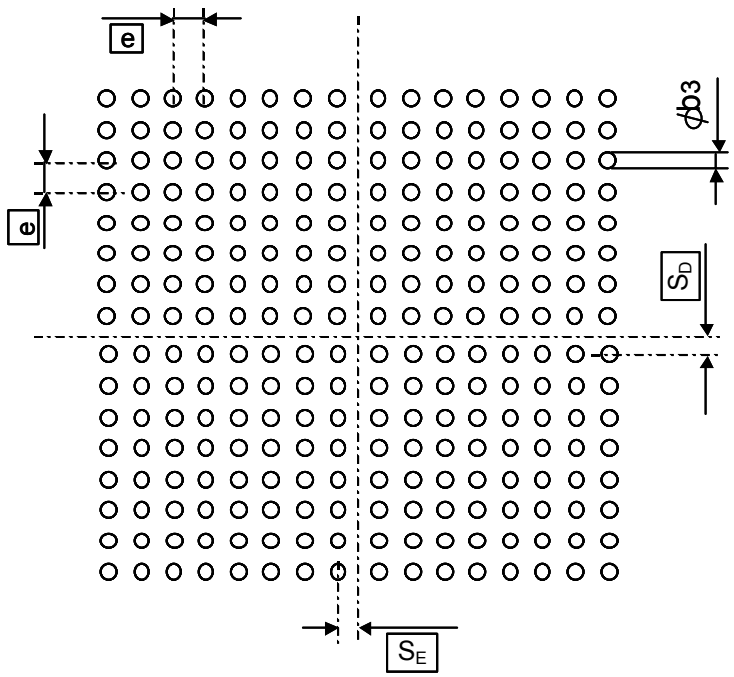


Figure 3

10. Dimensions

10.1 Group 1

Table 1

Unit: mm

Term	Symbol	Specification	Recommended value	Notes
Code of package nominal dimension	E × D	**(1) Flanged type** Code of package nominal dimension for Flanged-type package is defined as “the package length (D) × width (E)”, which is expressed in the tenths place in millimeter. **(2) Real chip-size type** Code of package nominal dimension for Real chip-size package is defined as “the package length (D) × width (E)”, which is expressed in the hundredths place in millimeter.	-	-
Package length	D	**(1) Flanged type** Package length, D_{nom}, ranges from 1.5 to 21.0 mm in increments of 0.5 mm for rectangular packages. While, the length of square package ranges from 1.5 to 14.5 mm in increments of 0.5 mm, and from 15.0 to 21.0 mm in increments of 1.0 mm. **(2) Real chip-size type** Package length, D_{nom}, is expressed in the hundreds place in millimeter. Minimum package length: 0.50 mm Maximum package length: 21.00 mm	-	-
Package width	E	**(1) Flanged type** Package width, E_{nom}, ranges from 1.5 to 21.0 mm in increments of 0.5 mm for rectangular packages. While, the width of square packages ranges from 1.5 to 14.5 mm in increments of 0.5 mm, and from 15.0 to 21.0 mm in increments of 1.0 mm. **(2) Real chip-size type** Package width, E_{nom}, is expressed in the hundreds place in millimeter. Minimum package width: 0.50 mm Maximum package width: 21.00 mm	-	-

Table 1 (Continued)

Unit: mm

<table>
<tr><th>Term</th><th>Symbol</th><th>Specification</th><th>Recommended value</th><th>Notes</th></tr>
<tr><td>Profile tolerance of package body</td><td>v</td><td>(1) v = 0.15 mm for Flanged type.
<table>
<tr><th></th><th>Package size</th><th>v</th></tr>
<tr><td>Level 1</td><td>1.5 – 21.0</td><td>0.15</td></tr>
<tr><td rowspan="2">Level 2</td><td>1.5 – 12.0</td><td>0.08</td></tr>
<tr><td>12.5 – 21.0</td><td>0.1</td></tr>
</table>
(2) v = 0.05 mm for Real chip-size packages including WLCSP.</td><td>-</td><td>Tolerance includes body-edge burr.</td></tr>
<tr><td>Off-center tolerance</td><td>w</td><td>(1) For Flanged type FBGA and FLGA
For Level 1:
<table>
<tr><th>e</th><th>w</th></tr>
<tr><td>0.80</td><td>0.20</td></tr>
<tr><td>0.65</td><td>0.20</td></tr>
<tr><td>0.50</td><td>0.20</td></tr>
<tr><td>0.40</td><td>0.15</td></tr>
<tr><td>0.30</td><td>0.15</td></tr>
</table>
For Level 2:
w = 0.15 mm regardless of the ball pitch.
(2) For Real chip-size type (including WLCSP):
w = 0.05</td><td>-</td><td>-</td></tr>
<tr><td>Profile height</td><td>A</td><td>Level 1
<table>
<tr><th>Amax</th></tr>
<tr><td>0.30</td></tr>
<tr><td>0.40</td></tr>
<tr><td>0.50</td></tr>
<tr><td>0.65</td></tr>
<tr><td>0.80</td></tr>
<tr><td>1.00</td></tr>
<tr><td>1.27</td></tr>
<tr><td>1.70</td></tr>
<tr><td>2.00</td></tr>
</table>
Level 2
<table>
<tr><th>Amax</th><th>Bilateral tolerance</th></tr>
<tr><td>0.30</td><td>0.07</td></tr>
<tr><td>0.40</td><td>0.07</td></tr>
<tr><td>0.50</td><td>0.07</td></tr>
<tr><td>0.65</td><td>0.10</td></tr>
<tr><td>0.80</td><td>0.10</td></tr>
<tr><td>1.00</td><td>0.10</td></tr>
<tr><td>1.27</td><td>0.10</td></tr>
<tr><td>1.70</td><td>0.10</td></tr>
<tr><td>2.00</td><td>0.10</td></tr>
</table>
* A_{nom} is at supplier's discretion.</td><td>-</td><td>"A" includes
(1) the heat slug, and
(2) the package warpage and tilt errors.</td></tr>
<tr><td>Stand-off height</td><td>A_1</td><td>(1) For FBGA
<table>
<tr><th>e</th><th>b_{nom}</th><th>A_{1min}</th><th>A_{1nom}</th><th>A_{1max}</th></tr>
<tr><td>0.80</td><td>0.50</td><td>0.35</td><td>0.40</td><td>0.45</td></tr>
<tr><td>0.80</td><td>0.45</td><td>0.30</td><td>0.35</td><td>0.40</td></tr>
<tr><td>0.65</td><td>0.40</td><td>0.28</td><td>0.33</td><td>0.38</td></tr>
<tr><td>0.50</td><td>0.30</td><td>0.20</td><td>0.25</td><td>0.30</td></tr>
<tr><td>0.40</td><td>0.25</td><td>0.15</td><td>0.20</td><td>0.25</td></tr>
<tr><td>0.30</td><td>0.20</td><td>0.10</td><td>0.15</td><td>0.20</td></tr>
</table>
(2) For FLGA
A_{1max} = 0.10</td><td>-
-</td><td>-
-</td></tr>
</table>

Table 1 (Continued)

Unit: mm

<table>
<tr><th>Term</th><th>Symbol</th><th>Specification</th><th>Recommended value</th><th>Notes</th></tr>
<tr><td>Terminal pitch</td><td>e</td><td>e = 0.80
0.65
0.50
0.40
0.30
0.25</td><td>-</td><td>-</td></tr>
<tr><td>Terminal diameter</td><td>b</td><td>
(1) For FBGA
<table>
<tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr>
<tr><td>0.80</td><td>0.45</td><td>0.50</td><td>0.55</td></tr>
<tr><td>0.80</td><td>0.40</td><td>0.45</td><td>0.50</td></tr>
<tr><td>0.65</td><td>0.35</td><td>0.40</td><td>0.45</td></tr>
<tr><td>0.50</td><td>0.25</td><td>0.30</td><td>0.35</td></tr>
<tr><td>0.40</td><td>0.20</td><td>0.25</td><td>0.30</td></tr>
<tr><td>0.30</td><td>0.17</td><td>0.20</td><td>0.23</td></tr>
</table>
(2) For C-FLGA
<table>
<tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr>
<tr><td>0.80</td><td>0.45</td><td>0.50</td><td>0.55</td></tr>
<tr><td>0.65</td><td>0.35</td><td>0.40</td><td>0.45</td></tr>
<tr><td>0.50</td><td>0.25</td><td>0.30</td><td>0.35</td></tr>
<tr><td>0.40</td><td>0.20</td><td>0.25</td><td>0.30</td></tr>
</table>
(3) For P-FLGA
<table>
<tr><th>e</th><th>min.</th><th>nom.</th><th>max.</th></tr>
<tr><td>0.80</td><td>0.35</td><td>0.40</td><td>0.45</td></tr>
<tr><td>0.65</td><td>0.28</td><td>0.33</td><td>0.38</td></tr>
<tr><td>0.50</td><td>0.20</td><td>0.25</td><td>0.30</td></tr>
<tr><td>0.40</td><td>0.15</td><td>0.20</td><td>0.25</td></tr>
<tr><td>0.30</td><td>0.12</td><td>0.15</td><td>0.18</td></tr>
<tr><td>0.25</td><td>0.10</td><td>0.13</td><td>0.16</td></tr>
</table>
</td><td>
<table>
<tr><th>e</th><th>b_{nom}</th></tr>
<tr><td>0.80</td><td>0.50</td></tr>
<tr><td>0.65</td><td>0.40</td></tr>
<tr><td>0.50</td><td>0.30</td></tr>
<tr><td>0.40</td><td>0.25</td></tr>
<tr><td>0.30</td><td>0.20</td></tr>
</table>
-
-
-</td><td>-
-
-</td></tr>
</table>

Table 1 (Continued)

Unit: mm

<table>
<tr><th>Term</th><th>Symbol</th><th>Specification</th><th>Recommended value</th><th>Notes</th></tr>
<tr><td>True position tolerance of terminals</td><td>x</td><td><table><tr><th>e</th><th>x</th></tr><tr><td>0.80</td><td>0.08</td></tr><tr><td>0.65</td><td>0.08</td></tr><tr><td>0.50</td><td>0.05</td></tr><tr><td>0.40</td><td>0.05</td></tr><tr><td>0.30</td><td>0.03</td></tr><tr><td>0.25</td><td>0.03</td></tr></table></td><td>-</td><td>-</td></tr>
<tr><td>Coplanarity</td><td>y</td><td><table><tr><th>e</th><th>y</th></tr><tr><td>0.80</td><td>0.10</td></tr><tr><td>0.65</td><td>0.10</td></tr><tr><td>0.50</td><td>0.08</td></tr><tr><td>0.40</td><td>0.08</td></tr><tr><td>0.30</td><td>0.05</td></tr><tr><td>0.25</td><td>0.05</td></tr></table></td><td>-</td><td>-</td></tr>
<tr><td>Parallelism of the top surface</td><td>y_1</td><td>y_1 = 0.20</td><td>-</td><td>-</td></tr>
<tr><td>Center terminal(s) position in length</td><td>S_D</td><td>When M_D is an odd number, S_D = 0
When M_D is an even number, S_D = e /2</td><td>-</td><td>-</td></tr>
<tr><td>Center terminal(s) position in width</td><td>S_E</td><td>When M_E is an odd number, S_E = 0
When M_E is an even number, S_E = e /2</td><td>-</td><td>-</td></tr>
</table>

Table 1 (Continued)

Unit: mm

Term	Symbol	Specification	Recommended value	Notes
Terminal matrix		Terminal position is determined by terminal pitch $\boxed{e}$, matrix size, M_D, M_E, $\boxed{S_D}$, and $\boxed{S_E}$.	-	-
Number of terminals	n	**(1)** For FBGA and FLGA: n_{max} = M_E max × M_D max (M_E max-1) × M_D max M_E max × (M_D max-1) (M_E max-1) × (M_D max-1) Maximum matrix sizes for the above combinations are listed in **Table 3**. **(2)** For FLGA, in addition to the above algorithm, the following combinations are allowed: n_{max} = (M_E max+1) × M_D max M_E max × (M_D max+1) (M_E max+1) × (M_D max+1) Maximum matrix sizes for the above combinations are listed in **Table 3**. M_D max ≦ ($\boxed{D}$ -bmax-v-w-x-2 (E.C.)) / $\boxed{e}$ +1 M_E max ≦ ($\boxed{E}$ -bmax-v-w-x-2 (E.C.)) / $\boxed{e}$ +1 E.C.: Edge clearance (=0.11 mm)	-	This table indicates the possible matrix size in each side, and the number of terminals as M_D × M_E.
Maximum matrix size in length	M_D			
Maximum matrix size in width	M_E			

10.2 Group 2

Table 2

Unit: mm

Term	Symbol	Specification	Recommended value	Notes
Overhang dimension in length	Z_D	$Z_D = \{D_{nom} - (M_D - 1) \times \boxed{e}\} / 2$	-	-
Overhang dimension in width	Z_E	$Z_E = \{E_{nom} - (M_E - 1) \times \boxed{e}\} / 2$	-	-
Terminal diameter of possible terminal zones	b_3	b_3 = bmax + x	-	-

Table 3 Combination of D/E and M_D/M_E

Table 3-1 [e] = 0.80 mm pitch FBGA/FLGA

[D] or [E]		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (Only for FLGA)
Flanged type	Real chip-size type			
1.5	0.95-1.74	-	-	2
2.0	1.75-2.54	2	-	3
2.5				
3.0	2.55-3.34	3	2	4
3.5				
4.0	3.35-4.14	4	3	5
4.5	4.15-4.94	5	4	6
5.0				
5.5	4.95-5.74	6	5	7
6.0	5.75-6.54	7	6	8
6.5				
7.0	6.55-7.34	8	12	14
7.5			13	15
8.0	7.35-8.14	9	8	10
8.5	8.15-8.94	10	9	11
9.0				
9.5	8.95-9.74	11	10	12
10.0	9.75-10.54	12	11	13
10.5				
11.0	10.55-11.34	13	12	14
11.5				
12.0	11.35-12.14	14	13	15
12.5	12.15-12.94	15	14	16
13.0				
13.5	12.95-13.74	16	15	17
14.0	13.75-14.54	17	16	18
14.5				
15.0	14.55-15.34	18	17	19
15.5				
16.0	15.35-16.14	19	18	20
16.5	16.15-16.94	20	19	21
17.0				
17.5	16.95-17.74	21	20	22
	17.96-18.45	35	34	36
18.0	17.75-18.54	22	21	23
18.5				
19.0	18.55-19.34	23	22	24
19.5				
20.0	19.35-20.14	24	23	25
20.5	20.15-20.94	25	24	26
21.0				
	20.95-21.0	26	25	27

Table 3 Combination of D/E and M_D/M_E

Table 3-2 [e] = 0.65 mm pitch FBGA/FLGA

[D] or [E]		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (Only for FLGA)
Flanged type	Real chip-size type			
1.5	0.85-1.49	-	-	2
2.0	1.50-2.14	2	-	3
2.5	2.15-2.79	3	2	4
3.0				
3.5	2.80-3.44	4	3	5
4.0	3.45-4.09	5	4	6
4.5	4.10-4.74	6	5	7
5.0	4.75-5.39	7	6	8
5.5				
6.0	5.40-6.04	8	7	9
6.5	6.05-6.69	9	8	10
7.0	6.70-7.34	10	9	11
7.5				
8.0	7.35-7.99	11	10	12
8.5	8.00-8.64	12	11	13
9.0	8.65-9.29	13	12	14
9.5				
10.0	9.30-9.94	14	13	15
10.5	9.95-10.59	15	14	16
11.0	10.60-11.24	16	15	17
11.5	11.25-11.89	17	16	18
12.0				
12.5	11.90-12.54	18	17	19
13.0	12.55-13.19	19	18	20
13.5	13.20-13.84	20	19	21
14.0				
14.5	13.85-14.49	21	20	22
15.0	14.50-15.14	22	21	23
15.5	15.15-15.79	23	22	24
16.0				
16.5	15.80-16.44	24	23	25
17.0	16.45-17.09	25	24	26
17.5	17.10-17.74	26	25	27
18.0	17.75-18.39	27	26	28
18.5				
19.0	18.40-19.04	28	27	29
19.5	19.05-19.69	29	28	30
20.0	19.70-20.34	30	29	31
20.5				
21.0	20.35-20.99	31	30	32
	21.00	32	31	33

Table 3 Combination of D/E and M_D/M_E

Table 3-3 [e] = 0.50 mm pitch FBGA/FLGA

[D] or [E]		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (Only for FLGA)
Flanged type	Real chip-size type			
1.0	0.72-1.95	-	-	2
1.5	1.22	2	-	3
2.0	1.72-2.21	3	2	4
2.5	2.22-2.71	4	3	5
3.0	2.72-3.21	5	4	6
3.5	3.22-3.71	6	5	7
4.0	3.72-4.21	7	6	8
4.5	4.22-4.71	8	7	9
5.0	4.72-5.21	9	8	10
5.5	5.22-5.71	10	9	11
6.0	5.72-6.21	11	10	12
6.5	6.22-6.71	12	11	13
7.0	6.72-7.21	13	12	14
7.5	7.22-7.71	14	13	15
8.0	7.72-8.21	15	14	16
8.5	8.22-8.71	16	15	17
9.0	8.72-9.21	17	16	18
9.5	9.22-9.71	18	17	19
10.0	9.72-10.21	19	18	20
10.5	10.22-10.71	20	19	21
11.0	10.72-11.21	21	20	22
11.5	11.22-11.71	22	21	23
12.0	11.72-12.21	23	22	24
12.5	12.22-12.71	24	23	25
13.0	12.72-13.21	25	24	26
13.5	13.22-13.71	26	25	27
14.0	13.72-14.21	27	26	28
14.5	14.22-14.71	28	27	29
15.0	14.72-15.21	29	28	30
15.5	15.22-15.71	30	29	31
16.0	15.72-16.21	31	30	32
16.5	16.22-16.71	32	31	33
17.0	16.72-17.21	33	32	34
17.5	17.22-17.71	34	33	35
18.0	17.72-18.21	35	34	36
18.5	18.22-18.71	36	35	37
19.0	18.72-19.21	37	36	38
19.5	19.22-19.71	38	37	39
20.0	19.72-20.21	39	38	40
20.5	20.22-20.71	40	39	41
21.0	20.72-21.00	41	40	42

Table 3 Combination of D/E and M_D/M_E

Table 3-4 [e] = 0.40 mm pitch FBGA/FLGA

[D] or [E]		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (Only for FLGA)
Flanged type	Real chip-size type			
1.0	1.50-1.95	-	-	2
1.5		2	-	3
2.0	1.96-2.45	3	2	4
2.5	2.46-2.95	5	4	6
3.0	2.96-3.45	6	5	7
3.5	3.46-3.95	7	6	8
4.0	3.96-4.45	8	7	9
4.5	4.46-4.95	10	9	11
5.0	4.96-5.45	11	10	12
5.5	5.46-5.95	12	11	13
6.0	5.96-6.45	13	12	14
6.5	6.46-6.95	15	14	16
7.0	6.96-7.45	16	15	17
7.5	7.46-7.95	17	16	18
8.0	7.96-8.45	18	17	19
8.5	8.46-8.95	20	19	21
9.0	8.96-9.45	21	20	22
9.5	9.46-9.95	22	21	23
10.0	9.96-10.45	23	22	24
10.5	10.46-10.95	25	24	26
11.0	10.96-11.45	26	25	27
11.5	11.46-11.95	27	26	28
12.0	11.96-12.45	28	27	29
12.5	12.46-12.95	30	29	31
13.0	12.96-13.45	31	30	32
13.5	13.46-13.95	32	31	33
14.0	13.96-14.45	33	32	34
14.5	14.46-14.95	35	34	36
15.0	14.96-15.45	36	35	37
15.5	15.46-15.95	37	36	38
16.0	15.96-16.45	38	37	39
16.5	16.46-16.95	40	39	41
17.0	16.96-17.45	41	40	42
17.5	17.46-17.95	42	41	43
18.0	17.96-18.45	43	42	44
18.5	18.46-18.95	45	44	46
19.0	18.96-19.45	46	45	47
19.5	19.46-19.95	47	46	48
20.0	19.96-20.45	48	47	49
20.5	20.46-20.95	50	49	51
21.0	20.96-21.00	51	50	52

Table 3 Combination of D/E and M_D/M_E

Table 3-5 [e] = 0.30 mm pitch FBGA/FLGA

[D] or [E]		M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (Only for FLGA)
Flanged type	Real chip-size type			
1.0	0.58-1.17	-	-	2
1.5	1.18-1.77	3	2	4
2.0	1.78-2.07	5	4	6
2.5	2.08-2.67	6	5	7
3.0	2.68-3.27	8	7	9
3.5	3.28-3.57	10	9	11
4.0	3.58-4.17	11	10	12
4.5	4.18-4.77	13	12	14
5.0	4.78-5.07	15	14	16
5.5	5.08-5.67	16	15	17
6.0	5.68-6.27	18	17	19
6.5	6.28-6.57	20	19	21
7.0	6.58-7.17	21	20	22
7.5	7.18-7.77	23	22	24
8.0	7.78-8.07	25	24	26
8.5	8.08-8.67	26	25	27
9.0	8.68-9.27	28	27	29
9.5	9.28-9.57	30	29	31
10.0	9.58-10.17	31	30	32
10.5	10.18-10.77	33	32	34
11.0	10.78-11.07	35	34	36
11.5	11.08-11.67	36	35	37
12.0	11.68-12.27	38	37	39
12.5	12.28-12.57	40	39	41
13.0	12.58-13.17	41	40	42
13.5	13.18-13.77	43	42	44
14.0	13.78-14.07	45	44	46
14.5	14.08-14.67	46	45	47
15.0	14.68-15.27	48	47	49
15.5	15.28-15.57	50	49	51
16.0	15.58-16.17	51	50	52
16.5	16.18-16.77	53	52	54
17.0	16.78-17.07	55	54	56
17.5	17.08-17.67	56	55	57
18.0	17.68-18.27	58	57	59
18.5	18.28-18.57	60	59	61
19.0	18.58-19.17	61	60	62
19.5	19.18-19.77	63	62	64
20.0	19.78-20.07	65	64	66
20.5	20.08-20.67	66	65	67
21.0	20.68-21.00	68	67	69

Table 3 Combination of D/E and M_D/M_E

Table 3-6 [e] = 0.25 mm pitch FLGA

[D] or [E] Real chip-size type	M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (Only for FLGA)
0.51-0.75	-	-	2
0.76-1.00	2	-	3
1.01-1.25	3	2	4
1.26-1.50	4	3	5
1.51-1.75	5	4	6
1.76-2.00	6	5	7
2.01-2.25	7	6	8
2.26-2.50	8	7	9
2.51-2.75	9	8	10
2.76-3.00	10	9	11
3.01-3.25	11	10	12
3.26-3.50	12	11	13
3.51-3.75	13	12	14
3.76-4.00	14	13	15
4.01-4.25	15	14	16
4.26-4.50	16	15	17
4.51-4.75	17	16	18
4.76-5.00	18	17	19
5.01-5.25	19	18	20
5.26-5.50	20	19	21
5.51-5.75	21	20	22
5.76-6.00	22	21	23
6.01-6.25	23	22	24
6.26-6.50	24	23	25
6.51-6.75	25	24	26
6.76-7.00	26	25	27
7.01-7.25	27	26	28
7.26-7.50	28	27	29
7.51-7.75	29	28	30
7.76-8.00	30	29	31
8.01-8.25	31	30	32
8.26-8.50	32	31	33
8.51-8.75	33	32	34
8.76-9.00	34	33	35
9.01-9.25	35	34	36
9.26-9.50	36	35	37
9.51-9.75	37	36	38
9.76-10.00	38	37	39
10.01-10.25	39	38	40
10.26-10.50	40	39	41
10.51-10.75	41	40	42

Table 3 Combination of D/E and M_D/M_E

Table 3-6 [e] = 0.25 mm pitch FLGA (continued)

[D] or [E] Real chip-size type	M_D max or M_E max	M_D max-1 or M_E max-1	M_D max+1 or M_E max+1 (Only for FLGA)
10.76-11.00	41	40	42
11.01-11.26	42	41	43
11.26-11.50	43	42	44
11.51-11.75	44	43	45
11.76-12.00	45	44	46
12.01-12.25	46	45	47
12.26-12.50	47	46	48
12.51-12.75	48	47	49
12.76-13.00	49	48	50
13.01-13.25	50	49	51
13.26-13.50	51	50	52
13.51-13.75	52	51	53
13.76-14.00	53	52	54
14.01-14.25	54	53	55
14.26-14.50	55	54	56
14.51-14.75	56	55	57
14.76-15.00	57	56	58
15.01-15.25	58	57	59
15.26-15.50	59	58	60
15.51-15.75	60	59	61
15.76-16.00	61	60	62
16.01-16.25	62	61	63
16.26-16.50	63	62	64
16.51-16.75	64	63	65
16.76-17.00	65	64	66
17.01-17.25	66	65	67
17.26-17.50	67	66	68
17.51-17.75	68	67	69
17.76-18.00	69	68	70
18.01-18.25	70	69	71
18.26-18.50	71	70	72
18.51-18.75	72	71	73
18.76-19.00	73	72	74
19.01-19.25	74	73	75
19.26-19.50	75	74	76
19.51-19.75	76	75	77
19.76-20.00	77	76	78
20.01-20.25	78	77	79
20.26-20.50	79	78	80
20.51-20.75	80	79	81
20.76-21.00	81	80	82

11. Registration procedure of standard outline drawings

The committee member who wishes to propose a new outline standard will fill in the Appendix Form 5 in the "Administrative Rules of the TSC on Semiconductor Device Packages", and proceed to the registration procedure of the standard, following the "Manual for the standard of integrated circuit packages".

Symbol "*" in **Table 4** indicates the cells which will be filled with dimensions or descriptions.

Table 4

Reference Number				
Package codes		#-#FBGA###-##.## x ##.##-##.## #-#FLGA###-##.## x ##.##-##.##		
Symbols		MIN	NOM	MAX
Group 1	D		*	
	E		*	
	V			*
	W			*
	A			*
	A_1	*	*	*
	e		*	
	b	*	*	*
	x			*
	y			*
	y_1			*
	n		*	
	M_D		*	
	M_E		*	
	Terminal depopulation	* (**Note**)		
Group 2	S_D		*	
	S_E		*	
	Z_D		*	
	Z_E		*	
	b_3			*

Note: Please fill in either "Full matrix", "Staggered matrix" or "Perimeter matrix with X rows" here, where "X" is natural number. Any other unique patterns would be defined or illustrated in each standard of individual package outline.

EXPLANATION

1. Purpose of this design guide

The purpose of this design guide is to standardize the package outlines of Fine-Pitch Ball Grid Array (FBGA) packages and Fine-Pitch Land Grid Array (FLGA) packages in the industry, and to establish the design requirements that shall be followed for designing future package standard outlines or related parts.

2. History of deliberations

CSP Workshop, which is the predecessor of the "Future Generation Packaging Workshop", was formed as a subordinate of the Electronics Device Integration Technologies Committee in early 1995 for the purpose of investigating CSP and discussing the possibility of outline standardization. After many months of discussion, CSP Workshop transferred standardization activity to the Technical Standardization Committee on Semiconductor Device Packages. The Area Array Subcommittee, the subordinate organization of the committee, started the deliberation in details on Oct. 1995.

A recent surge in market demand for FBGA and FLGA induced the standardization activity of square body FBGA and FLGA based on the "Design guideline of integrated circuits for Ball Grid Array" (referred to as "BGA Design Guide" hereinafter), **JEITA EDR-7315**, in order to avoid the confusion that might have caused by the absence of outline standard in industry. The subcommittee completed the deliberation on Apr. 1998, and released the publication **JEITA EDR-7316** (referred to as "FBGA/FLGA design guide" hereinafter).

In late 1990, rising market demand for memory devices packaged in FBGA and FLGA drove the committee to prepare the design guide for the packages with rectangular outlines, and the deliberation started on Nov. 1998. The previous FBGA/FLGA design guide, **JEITA EDR-7316**, was reviewed for inclusion of rectangular outlines, and the draft was produced by amending and adding some descriptions to the document. The subcommittee completed the deliberations and preparations of draft on May 1999. The committee approved the design guide as the provisional standard, **JEITA EDX-7316**, which had been effective until Mar. 2001. The subcommittee resumed discussion to unify **JEITA EDR-7316** and **JEITA EDX-7316**, and then completed the draft on Mar. 2001. It was published as FBGA/FLGA design guide, **JEITA EDR-7316A**, for both square and rectangular bodies.

Since then, trends toward downsizing and multifunction feature of portable electronics devices drove the LSI packages to smaller and higher-density outlines. Packages with finer terminal pitches and the ultimate chip-size outlines have appeared in the market. "Ultra Fine Pitch Package Task Force" was formed on Dec. 2003, and started the deliberation in order to standardize the packages with the terminal pitch of 0.3 mm or lower and "Wafer Level Chip Size Package". The outcome was published as **JEITA EDR-7316B** as an amendment of **JEITA EDR-7316A** on May 2006. Then the dicing type package task force was formed to review the package tolerances to meet the tighter-tolerance requirements from the higher-density board assembly, and finally published **JEITA EDR-7316C** on Jan. 2007.

3. Main dimensions reviewed

(1) Datum

The committee chose the ball-based datum, emphasizing the importance of the ball position accuracy for fine pitch packages. In order to harmonize with **JEDEC** standard, the datum definition was revised so that two nearest balls to the midpoint of each side determines the datum. Datum definition is described in section **4.** in detail.

(2) Code of package nominal dimension

Code of package nominal dimension is composed of the package width and length which are expressed in the tenths place in millimeter for Flanged type FBGA and in the hundredths place in millimeter for Real chip-size package (Drop the number at the thousandths place). Code of package nominal dimensions, expressed in the tenth place or hundredth place, symbolize the concept of CSP which pursues the minimal package size.

Also, the code of package nominal dimension, which used to be expressed by E × D, was redefined to be D × E in order to harmonize the **JEDEC** standard.

(3) Background of the event when the definitions of the package length "D" and width "E" were exchanged

BGA Design Guide, **JEITA EDR-7315**, used to define that the body size in the vertical direction was package width "E" and one in the horizontal direction was package length "D", when a package was viewed from the terminal side with the index corner in the bottom left corner position. Two conflicting issues were brought up against this definition.

(a) Commercially available rectangular BGA appeared to have larger package width than package length according to this definition, and it conflicted with the common sense that package length is larger than package width.

(b) The package width in **JEDEC** standard refers to the package length in **JEITA** standard, and vice versa. The Committee interchanged the terms so that the body side in the vertical direction is package length "D" and the one in the horizontal direction is package width "E", when a package is viewed from the terminal side with the index corner in the bottom left corner position, to avoid the unnecessary confusion in the industry.

Also, the committee agreed to disregard the relative size of length and width in the definition.

It is because some of memory packages have larger width than length due to the industry standard footprints, or memory die with larger width than length.

(4) Package length (D) and width (E)

The subcommittee determined that the maximum package length and width of FBGA and FLGA are 21.00 mm, because the maximum die size available is around 20.00 mm sq., and the body size which could contain it was 21.00 mm sq. from the list in the BGA design guide. Minimum permissible body size is lowered to 1.50 mm based on the expectation of the market trend toward the further miniaturization. While, the Wafer Level CSP extends to the minimum body size of 0.5 mm sq. because the package with four terminals at 0.25 mm pitch can exist.

(5) Package height (A)

Maximum FBGA package height was specified to be 2.00 mm based on the survey and discussions in the Area Array Subcommittee. This design guide, following the amendment of **JEITA EDR-7303B**, included the additional categories of maximum package height, 1.00, 0.80, 0.65, and 0.50 mm which were coded as V, W, U, and X, respectively. Then, additional two categories, 0.4 mm and 0.3 mm, were included as an amendment to this design guide based on the survey results conducted among the **JEITA** member companies.

(6) Stand off height (A_1)

(a) FBGA

The simulation results and actual measurements of the FBGA, of which ball diameter was 60% of the terminal pitch, indicated that the stand off height was equal to 50% of the terminal pitch. It turns into the current practice that the nominal dimension of stand off height is defined as 50% of the terminal pitch. There were some discussions whether a stand off height "A_1" should be defined by the minimum value only or by all minimum, nominal and maximum values. Subcommittee concluded that all minimum, nominal, and maximum specifications were necessary for pick-and-place machines to mount the devices on board and to test devices in sockets. In addition to the variation of 0.5 mm ball diameter, optional variation of 0.45 mm ball diameter was included in this guide. Nominal stand off height for 0.45 mm ball diameter was calculated by subtracting the differential of ball diameters of original 0.5 mm and optional 0.45 mm from the original stand off height of 0.4 mm, and came to 0.35 mm.

(b) FLGA

Although there are two terminal types in FLGA, flat land type and bump type, FLGA is defined as the package of which stand off height is 0.10 mm or lower without regard to type of terminals.

(7) Terminal pitch (e)

Variations of terminal pitches were derived by 20% reduction rule from the reference pitch of 1.00 mm, and were determined to be 0.80, 0.65, 0.50, 0.40, 0.30, and 0.25 mm. The packages with 0.25 mm pitch were categorized as FLGA only because of its low stand off height. While, the package with 1.0 mm terminal pitch was categorized as BGA and follows BGA Design Guide.

(8) Terminal diameter (b)

(a) FBGA

Solder ball diameter is basically given by 60% of ball pitch. FBGA with solder balls of 0.5 mm diameter at 0.8 mm pitch saw some difficulties during manufacturing process, even though the ball diameter follows 60% of ball pitch. It raised a question what would be the proper ball diameter for 0.80 mm pitch FBGA, and options of 0.45 mm or 0.40 mm in diameter were proposed. Subcommittee reached an agreement on adopting 0.45 mm in diameter as an option for 0.8 mm pitch FBGA, because it allows the same designs for test socket and PWB. While, the ball diameter of 0.40 mm requires a separate design so that it was rejected as an option to 0.8 mm pitch FBGA.

(b) FLGA

The design guide defined that the land diameter is 60% of terminal pitch for Ceramic FLGA, and 50% for Plastic FLGA. Given that ball diameter is 60% of the ball pitch for FBGA, ball-land diameter will be 50% of the pitch and is the same as the one of Plastic FLGA. It allows suppliers to utilize the same package substrate for both FBGA and FLGA, and secure more space between lands for routing traces. A coefficient of thermal expansion of Ceramic FLGA is so different from the one of PWB that Ceramic FLGA needs larger diameter of lands to assure the solder joint reliability.

Wafer Level CSP has the tighter terminal-position tolerance of +/-0.03 mm over all terminals because of the high-precision proceeding technology.

(9) Parallelism of top surface (y1)

Parallelism tolerance of top surface was determined by the consideration of the pick-up mechanism of the machine. Under the miniaturization and low-profile trend, a question was raised if the parallelism tolerance of top surface should be determined by the package thickness, width and length. The subcommittee concluded not to change the parallelism tolerance of top surface, y1, because the coplanarity, y, is tight enough to control the parallelism error as well.

(10) Coplanarity (y)

The coplanarity criteria of FBGA were quoted from the specifications of QFPs, which are often mounted with FBGA on the same PWB. For the packages with 0.3 mm pitch or lower, the coplanarity criteria are determined by the expected thickness of the solder paste on the PWB.

(11) True position tolerance of terminals (x)

The true position tolerance of terminals is basically 10% of the terminal pitch.

Comparing the packages of 0.25 and 0.3 mm ball pitch with that of 0.4 mm ball pitch in terms of the space between each possible existing zone of terminals (defined by **JEITA ED-7304**), it becomes approximately 0.05 mm which is considered to be enough to mount on PWB, and then x is obtained. Wafer Level CSP was given 0.03 mm regardless of ball pitch because of higher process capability.

(12) Profile tolerance of package body and off-center tolerance (v, w)

The profile tolerance of package body “v” and off-center tolerance “w” were determined based on the survey results carried out in the committee. Wafer Level CSP was given 0.05 mm for both profile and off-center tolerances over all terminals because of higher process capability.

(13) Maximum matrix size (M_D, M_E)

M_D max and M_E max denote the maximum matrix sizes in length and width, respectively, or “Mmax” denote the maximum matrix size of a square-body package. The maximum matrix size is calculated by the following algorithms and truncated into integer.

$$M_D \max \leqq (\boxed{D} - bmax - v - w - x - 2\,(E.C.)) / \boxed{e} + 1$$

$$M_E \max \leqq (\boxed{E} - bmax - v - w - x - 2\,(E.C.)) / \boxed{e} + 1$$

$\boxed{D}$, $\boxed{E}$: Package length and width

bmax : Maximum ball diameter (b_{nom} + tolerance of ball diameter)

v : Body-edge tolerance

w : Off-center tolerance

x : Terminal true position tolerance

E.C. : Edge clearance (0.11 mm)

$\boxed{e}$: Terminal pitch

"M_D max-1" and "M_E max-1" arrays, which are the matrix sizes reduced by one row and one column from the standard "M_D max" and "M_E max", are also included in the design guide. The committee discussed further possibility of inclusion of "M_D max+1" and "M_E max+1" arrays, and concluded that design guide allows this variation only for FLGA as far as (E.C.) remains positive.

(14) Background of defining maximum matrix size

(a) Maximum matrix size (Mmax)

Maximum terminal matrix size "Mmax" was determined as the geometrically possible numbers to hold terminals on the underside of packages. **JEITA** Semiconductor Packing Subcommittee and **JEDEC JC-11** claimed that customer preferred the solder balls were immune from touching the tray. Also, manufacturers and customers demanded some clearance between the outermost rows or columns of balls and body edge to prevent the ball deformation or ball missing during their handling. Subcommittee discussed the introduction of additional edge clearance and reached the agreement to set additional space.

The body-edge tolerance, v, was determined based on the requirements of the body-based alignment mechanism of pick-and-place machine, and the off-center tolerance, w, was determined based on the positioning accuracy.

(b) Maximum terminal matrix size reduced by one row and one column (Mmax-1)

$M_D$max-1 and $M_E$max-1 arrays, which are the matrix sizes reduced by one row and one column from the standard $M_D$max and $M_E$max, are also standard variation in the design guide. Allowing both Mmax and Mmax-1 as standard terminal matrix sizes, the design guide provides both odd and even numbers of variations for the listed body sizes. FLGA, having none of the balls, is allowed to have additional variation of Mmax+1, depending on the combination of body size and land pitch allows.

(15) Identification of the terminal A1 corner

The subcommittee discussed the unique ball layout that indicates the terminal A1 corner for the convenience of the recognition system of pick-and-place machine. Proposals of the layout include the addition of a ball at the most inner corner of the peripheral ball layout and the depopulation of A1 ball from the array. The subcommittee, however, did not achieve an agreement to standardize the ball layout. Market has already seen many packages whose balls at all corners were depopulated, or the packages whose center space was surrounded by peripheral balls was not sufficient for additional ball, and so on. In addition to the geometrical constraint of the package layout, the requirements of board assemblers have not been consistent enough to proceed to standardize the specific ball layout as the terminal A1 corner index.

Identification of terminal A1 corner by additional or depopulated ball, however, may gradually penetrate into the industry.

(16) Package overhang (Z_D, Z_E)

First issue of **JEITA EDR-7316** expressed the package overhang, as basic dimensions of $\boxed{Z_D}$ and $\boxed{Z_E}$. The committee corrected the expression to "Z_D" and "Z_E", following the claim that these values were not basic dimensions from Netherlands National Committee at the IEC meeting.

(17) Others

(a) During the discussion of the draft **JEITA EDR-7316B**, there was an opinion that the nominal dimensions of stand-off height "A_1" and terminal diameter "b" were allowed to be any figures in the range of 30 to 70% of a certain value with tighter tolerance. The reasons of this proposal were:

(1) Some ball-formation methods on package do not satisfy the current nominal value.

(2) "A_1" and "b" dimensions are dependent on the size of the raw solder balls and the land size of substrate.

(3) A substrate is often used for both BGA and LGA. "A_1" and "b" sometimes do not meet the nominal dimensions in such cases.

The task force, however, concluded that the nominal dimension shall be the single specific value for the purpose of the standardization of packages and test sockets.

(b) The package tolerances are classified into two levels to establish the criteria for the dicing type package in addition to the conventional criteria. Semiconductor suppliers can choose the levels according to their process capability.

4. Definition of the datum

Previous method to establish the datum $\boxed{A}$ and $\boxed{B}$ was first determining the center lines which were calculated from all terminal centers by using the least mean square method, and then, adjusting these two lines crossing perpendicularly. The procedure to establish the datums was then revised to harmonize with the **JEDEC** standard, and was summarized in "Measuring method for package dimensions of Ball Grid Array", **JEITA ED-7304**, which still took the ball-based datum but the similar process to establish the datum as **JEDEC** method specifies.

(a) Determine two solder balls which locate closest to the midpoint on each outermost row or column of the package, excluding the midpoint ball itself.

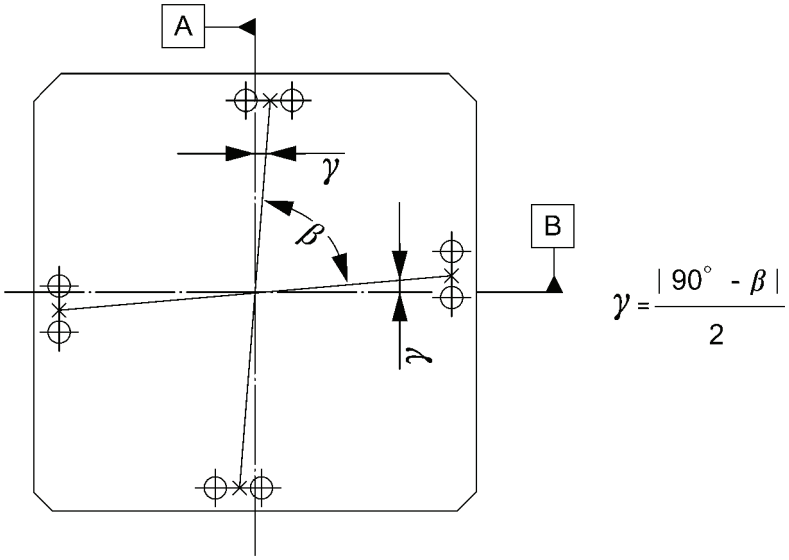
(b) Obtain the midpoint of these two balls on each side.

(c) Draw the line between the midpoints on one side and the counter side.

(d) Measure the angle β between the centerlines crossing together.

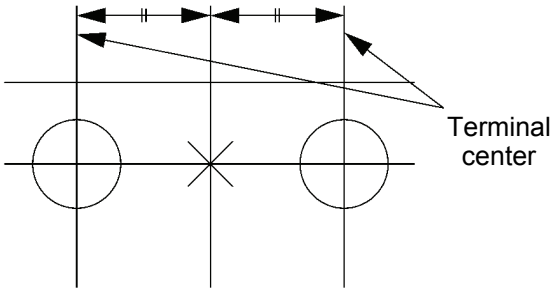
(e) Adjust both centerlines to cross perpendicularly by rotating the half angles of the differential between 90 degrees and β.

(f) These lines will hereafter be referred to as datum $\boxed{A}$ and $\boxed{B}$.



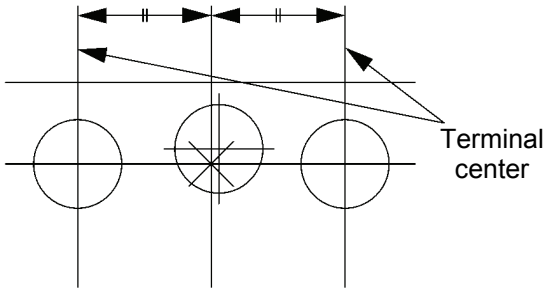
Appendix figure 1

Definition of the midpoints of each side



Midpoint of two terminal center

Appendix figure 2 When M_E is an even number



Midpoint of two terminal center

Appendix figure 3 When M_E is an odd number

5. Members of deliberative bodies

This design guide was deliberated in the Subcommittee on Integrated Circuit Packages, which is the subordinate organization of TSC on Semiconductor Device Packages.

Details of technical issues were discussed in the task force, which had been formed by experts from the member companies of the Subcommittee on Integrated Circuit Packages specifically for this task.

Participated members are:

<Technical Standardization Committee on Semiconductor Device Packages>

TSC Chair	Toshiba Corp.	Chiaki Takubo

<Subcommittee on Integrated Circuit Packages>

Subcommittee chair	Sony Corp.	Hiroyuki Shigeta
Assistant chair	NEC Electronics Corp.	Hirofumi Nakajima
	Fujitsu Ltd.	Kazunari Kosakai
Members	Amkor Technology Japan	Jun Taniguchi
	Elpida Memory, Inc.	Fumitake Okutsu
	Enplas Corp.	Takayuki Yamada
	Oki Electric Industry Co., Ltd.	Akio Nakamura
	Kyocera Corp.	Akihiko Funahashi
	Sanyo Electric Co., Ltd.	Kiyoshi Mita
	Sumitomo 3M Ltd.	Kouji Kukimoto
	Seiko Epson Corp.	Yoshiaki Emoto
	Dai Nippon Printing Co., Ltd.	Yoshiyuki Saitou
	Toshiba Corp.	Yasuhiro Koshio
	Texas Instruments Japan Ltd.	Takayuki Ohuchida
	Hitachi Cable Ltd.	Tsuyoshi Ishihara
	Fuji Electric Co Ltd.	Osamu Hirohashi
	Matsushita Electric Industrial Co., Ltd.	Toshiyuki Fukuda
	Yamaichi Electric Co., Ltd.	Hideo Watanabe
	Unitechno Inc.	Hitoshi Matsunaga
	Renesas Technology Corp.	Takanori Hashizume
	Rohm Co., Ltd.	Youichi Kimura
Special members	Shin-Etsu Polymer Co., Ltd.	Ken Tamura
	Toyojushi Co., Ltd.	Hitoshi Kazama