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Design guideline of integrated circuits for Surface Vertical Package (SVP)

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Design guideline of integrated circuits for Surface Vertical Package (SVP)

1. SCOPE OF APPLICATION

This standard regulated outline drawings and dimensions of surface vertical package (SVP), especially plastic packages, classified as form 1 under the EIAJ ED-7300 (standard for preparing standard outline drawings (integrated circuits) of semiconductor devices).

NOTE This technical report is revised edition of EIAJ ED-7424.

2. TERMS

The definition of the terms used in this technical report complies with the EIAJ ED-7300. New terms will defined in the description of this technical report.

3. BACKGROUND

The shrink zigzag inline package (SZIP) is a new development of the zigzag inline package (ZIP) to respond to the ongoing miniaturization of electronic devices. The SVP was the result of applying surface mounting technology to this series of vertical packages to facilitate PCB design and allow further miniaturization. In order to include memory devices and to ensure compatibility between different products, the outer dimensions suggested by JEDEC were considered in the standardization of the package. Standard design values, i.e. design center concepts have been used as guidelines in the standardization effort in determining each dimensional value.

4. DEFINITION OF SVP

The SVP is defined as a package with leads projecting from one side of the package and whose external leads (the part of the leads that are connected to a PCB) have an L-shape configuration to allow surface mounting. It is a package with an L-shape metal stand - which is used to determine the position of the package relative to a PCB and to keep the package vertical - that is placed on the same side as the terminals.

5. NUMBER OF TERMINALS

Numbering of terminal complies with the EIAJ ED-7300.

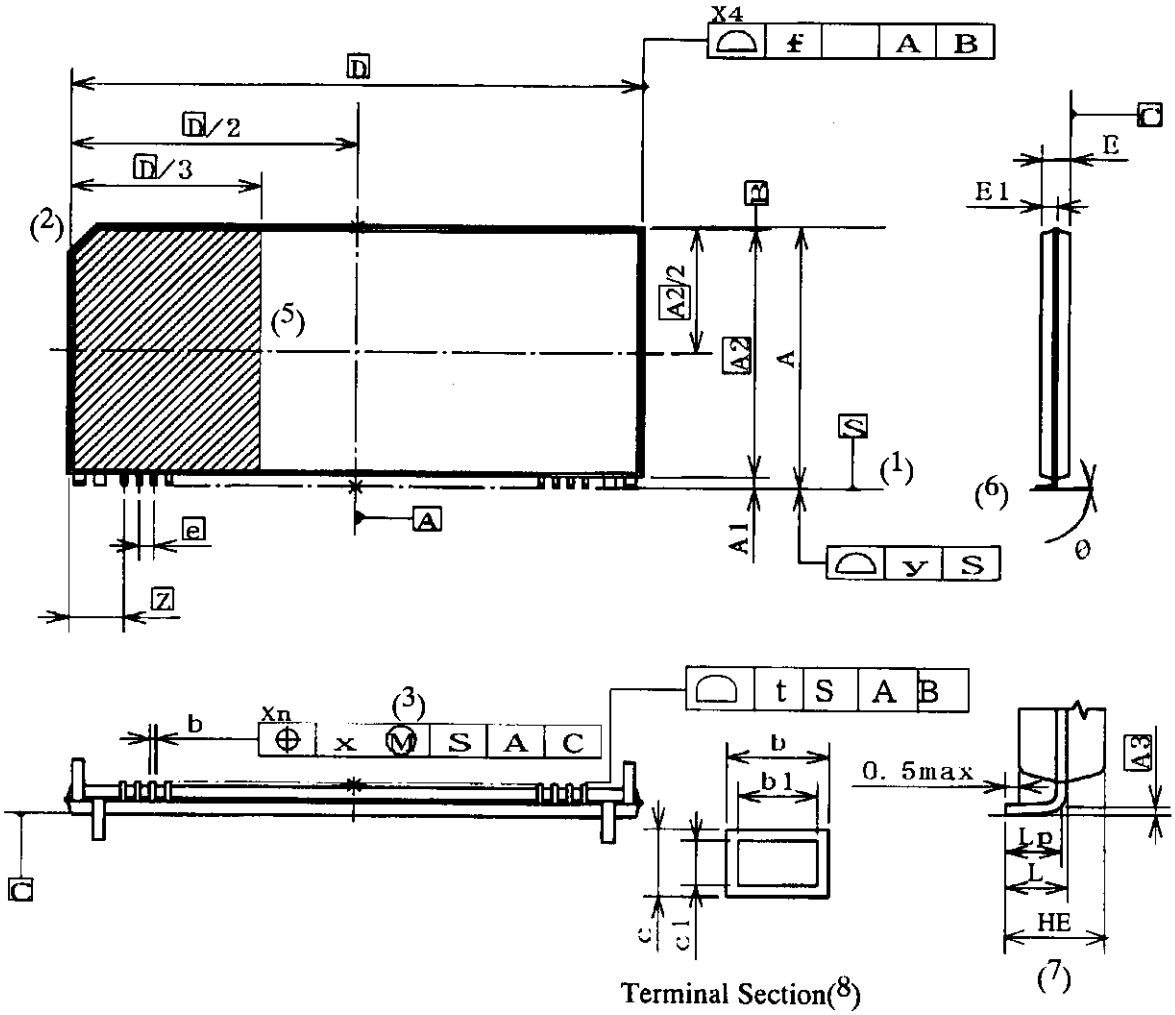
6. NOMINAL DIMENSIONS

The dimensions of package body (Symbol:$A_2 \times D$) is applied to nominal dimensions.

7. REFERENCE CHARACTERS AND DRAWINGS

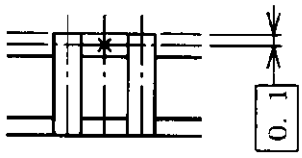
7.1 Outline Drawings

Figure 1



Terminal Section(8)

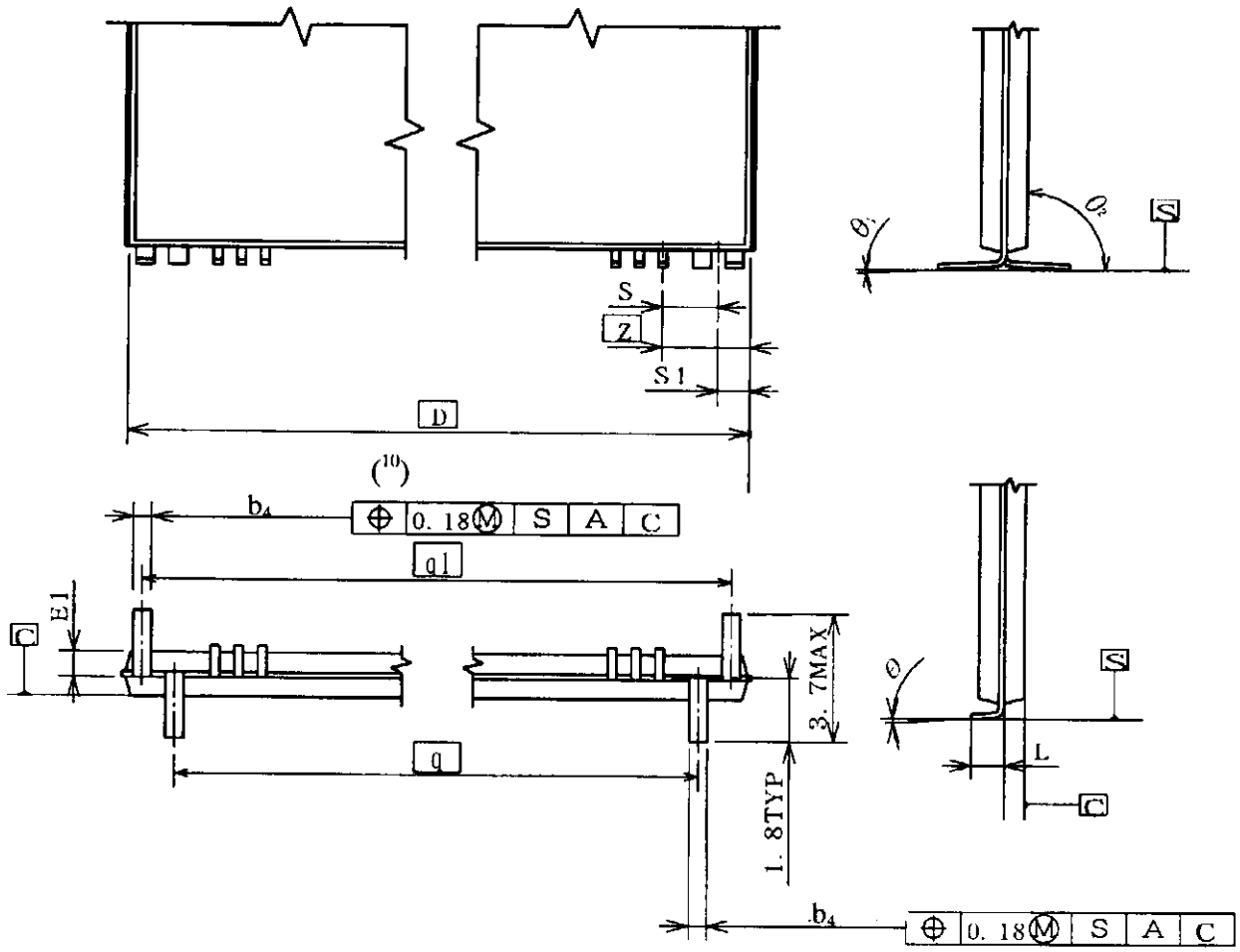
Detail area of datum A



The center of facing side of adjacent leads
at position 0.1mm inside top of the leads.

7.2 Detail of Stand Lead

Figure 2



Note (1) The mounting surface, with which a package is in contact.

(2) Visual and mechanical index like the chamfer such as the one shown in the drawing above is not required but recommended.

(3) The maximum mounting conditions apply to the positional tolerance of the terminals. (For the maximum body conditions, refer to ISO 2692/JIS B 0023.)

(4) Specifies the true geometric position.

(5) Shows the allowable position of the index mark. More than half area of the index mark must be included in the shaded area.

(6) Terminals must be bent in L-shape to top side of a package.

(7) The dimension doesn't include Stand terminals.

(8) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

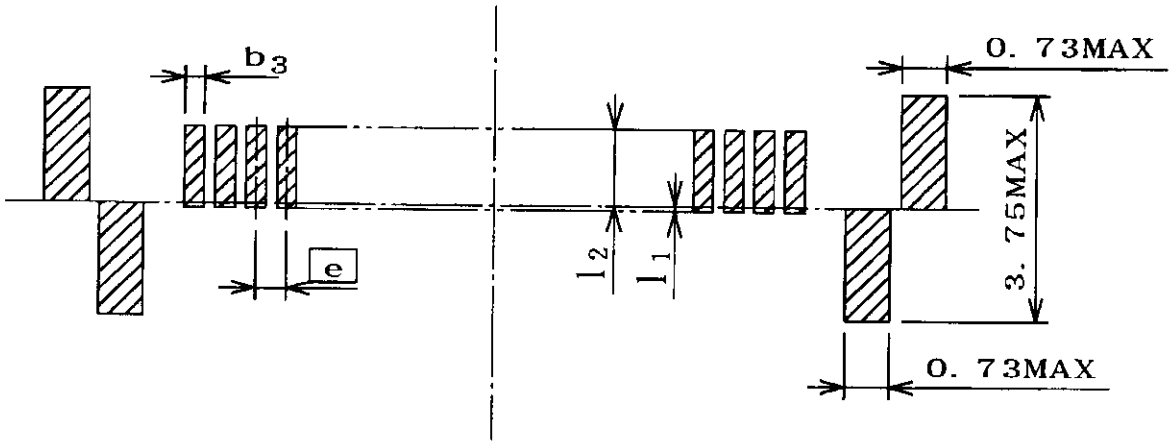
(9) Resin burrs and gate remains of the package sides with no terminals are 0.15mm MAX per side.

(10) Stand terminal width denotes the raw material width.

REMARKS 1 ALLOWABLE RANGE OF SOLDERING PART OF TERMINALS

The range where the terminals to be soldered can exist is shown in Figure 3 as reference for the foot print design.

Figure 3



$l_{1\,max} = t/2$

$l_{2\,max} = L_{P\,max} + t/2$

$b_{3\,max} = b_{max} + x$

8. DIMENSIONAL STIPULATIONS, RECOMMENDED VALUES, SUPPLEMENTARY MATTERS, ETC

8.1 Group 1

Table 1

Unit : mm

Name	Reference symbol	Stipulations	Recommended value	Supplementary matters, etc
Nominal size	$A_2 \times D$	1. Nominal size combines Package height A_2 with Package length D. 2. Nominal size is shown the followings. 5×16,18,20,22,25,28,32,36 6×16,18,20,22,25,28,32,36 7×16,18,20,22,25,28,32,36 9×16,18,20,22,25,28,32,36 11×16,18,20,22,25,28,32,36 13×16,18,20,22,25,28,32,36		Package height is less than 7mm, A_2 is determined as 1mm along. Package height is more than 7mm, A_2 is determined as 2mm along.
Package length	D	Package length D is shown the followings. D=16.00, 18.00, 20.00, 22.00, 25.00 28.00, 32.00, 36.00		Mismatch of the upper and lower dies and resin burrs are not included.
Package width	A_2	Package width A_2 is determined as follows. A_2=5.00,6.00,7.00,9.00,11.00,13.00		It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
Seated height	A	The maximum values of the seated height A are determined as follows. A_2 / A_{max} 5.00 / 5.80 6.00 / 6.80 7.00 / 7.80 9.00 / 9.80 11.00 / 11.80 13.00 / 13.80		A includes the resin burrs and residual gate.
Stand-off height	A_1	min / max 0.40 / 0.60	A = 0.50	
Standard height of soldered points	A_3	A_3 = 0.25		
Terminal pitch	e	e = 0.50 e = 0.65 e = 0.80		Determines the true geometrical position.

Table 1 (Continued)

Unit : mm

Name	Reference symbol	Stipulations	Recommended value	Supplementary Matters, etc
Length of soldered part	L_P	min 0.60 / max 1.20		
Terminal width	b	e: 0.50 / min 0.17 / max 0.27 e: 0.65 / min 0.17 / max 0.32 e: 0.80 / min 0.24 / max 0.40	1. Pb/Sn solder plating e: 0.50 / nom 0.22 e: 0.65 / nom 0.24 e: 0.80 / nom 0.32 2. Pd plating e: 0.50 / nom 0.20 e: 0.65 / nom 0.22 e: 0.80 / nom 0.30	1. b, c includes surface treatments. b_1, c_1 denotes the raw material dimensions. 2. b, b_1, c and c_1 apply to the ranges of 0.1 and 0.25 from the end of a terminal. 3. Values b, c apply to Pb/Sn solder plated terminal. The standard thickness of the solder layer shall be 0.010+0.010/-0.005. As Pd plating, it is very thin so terminal width is $b_{nom}=b_{1nom}$ $c_{nom}=c_{1nom}$
	b_1	e: 0.50 / min 0.17 / nom 0.20 / max 0.23 e: 0.65 / min 0.17 / nom 0.22 / max 0.27 e: 0.80 / min 0.24 / nom 0.30 / max 0.36		
Terminal thickness	c	min 0.09 / max 0.20	1.Solder plated c_{nom}= 0.17 2.Pd plated c_{nom}= 0.15	
	c_1	min 0.09 / nom 0.15 / max 0.16		
Package thickness	E	min 1.20 / max 1.40	E_{nom} = 1.25	The warp of package is included.
Package thickness of terminal bending side	E_1	min 0.37 / max 1.03		

Table 1 (Continued)

Unit : mm

Name	Reference symbol	Stipulations	Recommended value	Supplementary Matters, etc
Overall width	H_E	H_{Emax} = 1.90		
Stand lead pitch	q	q = D −2.70		
	q_1	q_1 = q +1.80		
Terminal angle	θ	$\theta = 0^\circ \sim 8^\circ$	3°	
	θ_1	$\theta_1 = 0^\circ \sim 5^\circ$		
Tolerance of terminal center position	x	e: 0.50 → x: 0.08 e: 0.65 → x: 0.13 e: 0.80 → x: 0.16		The concept of the terminal center shall be specified in the outline drawings.
Coplanarity	y	e: 0.50 → y: 0.08 e: 0.65 → y: 0.10 e: 0.80 → y: 0.10		Coplanarity is included stand leads.
Tolerance of package edge position	f	f_{max} = 0.2		
Positional tolerance of terminal tips	t	t_{max} = 0.2		
Number of terminals	n	Number of terminals are determined as follows. (1) Number of terminals n is a maximum number that is decided by each terminal pitch and package length D except for overhang Z is more than 2.25mm. But number of terminals must be an even number only. (2) Number of existing terminals may be less than a maximum number. But the 1st terminal and nth terminal must be existence. And non-existing terminals must be continuously even number of central terminals.		

8.2 Group 2

Table 2

Unit : mm

Name	Reference symbol	Stipulations	Recommended value	Supplementary Matters, etc
Terminal length	L	min 0.65 / max 1.20		
Center position of stand lead	S_1	$S_{1nom}= \{D-(q+q_1)/2\}/2$	$S_{1nom} = 0.90$	The resin burrs and residual gate are not included.
	S	$S_{nom}= \{(q+q_1)/2-e\times(n-1)\}/2$		
Package angle	θ_2	$\theta_2=85^\circ \sim 95^\circ$	90°	
Package overhang	Z	$Z = \{D-e\times(n-1)\}/2$		The resin fins and residual gate are not included.
Stand terminal width	b_4	min 0.45 / max 0.55		

Table 3 Number of terminals

Unit : mm

D	e = 0.50		e = 0.65		e = 0.80	
	n	Z	n	Z	n	Z
16.00	24	2.250	18	2.475	14	2.800
18.00	28	2.250	20	2.825	16	3.000
20.00	32	2.250	24	2.525	20	2.400
22.00	36	2.250	26	2.875	22	2.600
25.00	42	2.250	32	2.425	26	2.500
28.00	48	2.250	36	2.625	30	2.400
32.00	56	2.250	42	2.675	34	2.800
36.00	64	2.250	48	2.725	40	2.400

9. STANDARD REGISTRATION

When you need to register a new outline specification on the standard, complete the appendix format 3 in Technical Standardization Committee on Semiconductor Device Package steering rule, in compliance with the Standardization Rule.

In order to make a package dimension table, which comes under Item 2, Appendix format 3, fill the dimensions marked with (√) in the following table 4.

Table 4

Serial Number				
External Type		SVP○○○−P−○○○○−○.○○		
Reference Symbol		min	nom	max
Group 1	D		√	
	A_2		√	
	A			√
	A_1	√	√	√
	A_3		√	
	b	√		√
	b_1	√	√	√
	c	√		√
	c_1	√	√	√
	θ	√	√	√
	θ_1	√		√
	E	√	√	√
	E_1	√		√
	H_E			√
	e		√	
	f			√
	t			√
	Lp	√		√
	q		√	
	q_1		√	
	x			√
	y			√
	n		√	
Group 2	S		√	
	S_1		√	
	θ_2		√	
	Z		√	
	L		√	
	b_4	√		√

EXPLANATION

1. OBJECT OF ESTABLISHMENT

This technical report is intended to provide the industrial standards for surface vertical packages (to be referred to as SVPs hereinafter) and the design guidelines in producing the SVPs and developing the automatic mounting machines and related parts.

2. PROGRESS OF DELIBERATION

After JEDEC proposed the establishment of SVP, the Plastic Package Committee, recognizing the need for a new standard, started work on SVP packages. At the 4th meeting of the Plastic Package Committee in April 1991, the standardization of SVP was recognized and the formulation of general rules for the preparation of outline drawings of such packages was discussed in the Plastic Package Subcommittee. Two of the proposed package holders, PSSVP and LSSVP, were retained while the dimensions were unified and the number of terminals was determined to maintain footprint compatibility. The dimension is determined that the metric dimensions which was the international trend. It was decided that the nominal size of the new package should be package height (A_2)× package length (D).

After going through the deliberations described above, the Plastic Package Committee ended formal deliberations and established and issued the new standard in the 20th meeting of the Special Technical Committee on Semiconductor Device Package in fiscal 1993.

Upon revision of the standard, two package holders are unified LSSVP, and the review were made by the Plastic Package Subcommittee. Thereafter, the final draft of the standard was approved by Semiconductor Package Standardization Committee during the review made in April 1998, which was established and issued as a new design guideline.

3. BACKGROUND FOR DIMENSIONAL PROVISIONS

(1) Terminal width (b) (b_1), terminal thickness (c), (c_1)

With regard to the surface treatment of the pin, the palladium plating (hereinafter referred to as the Pd plating) was added to the conventional solder plating which was believed to increase in the fortune. The "b_{nom}" "c_{nom}" specification after the surface treatment was set to the target value of 0.01mm for the solder plating, and the same nominal width as that of the leadframe material was adopted since the plating thickness of the Pd was as small as a few micron meters.

(2) Package thickness of terminal bending side (E_1)

As the package holder is standardized in LSSVP, the dimensions of PSSVP are deleted.

(3) Tolerance of terminal center position

As the package holder is standardized in LSSVP, the dimensions of PSSVP are deleted.

(4) Terminal angle (θ), (θ_1)

As the terminal length is different stand terminals and electrode terminals, the terminal angles are instituted by the terminal length of a stand or an electrode. The terminal angle of an electrode terminal is determined to a range of 0 degree to 8 degree, and that of a stand terminal is determined to a range of 0 degree to 5 degree.

(5) Package (θ_2)

As this package is a vertical surface package, the package angle is instituted as a new dimension because of assembled packages perpendicular to the board.

4. INDUSTRIAL COPYRIGHT

Fujitsu Ltd. owns the patent (Patent No. 2,116,007). "SVP" is a registered trademark of Sony Corporation.

COMMITTEE MEMBERS

This design guide was mainly deliberated by the Plastic Package Subcommittee of the Technical Standardization Committee on Semiconductor Device Packages. The following lists their members.

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