EIAJ EDR-7318A

JEITA

Technical Report of Japan Electronics and Information Technology Industries Association

EIAJ EDR-7318A

Design guideline of integrated circuits for Plastic Small Outline Non-leaded package (P-SON)

Established in November, 1998
Revised in April, 2002

Prepared by
Technical Standardization Committee on Semiconductor Device Package

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EIAJ EDR-7318A

Technical Report of Japan Electronics and Information Technology Industries Association

Design guideline of integrated circuits for Plastic Small Outline Non-leaded package (P-SON)

1. Scope of Application

As providing the basics of standard outline drawing for semiconductor package. This technical report defines the forms and dimensions of plastic non lead package (hereinafter called P-VSON) which is classified into N-terminals of second category having the package form of B. This technical report is a revision version of **EIAJ ED-7318**.

Note: This technical report is corresponds **EIAJ ED-7311-13A** (Standard of integrated circuits package P-SON). The other relation standards are shown below.

EIAJ EDR-7324A (Design guideline of integrated circuits for Plastic Quad Flat Non Leaded Package (herein after referred to as P-QFN)), established in May 1999, revised in April 2002.

EIAJ ED-7311-22 (Standard of integrated circuits package (P-QFN)), established in April 2002.

2. Definition of the Technical Terms

The definition of the technical terms used in this Design guideline is in conformity with **EIAJ ED-7300**, As for the new term, it is due to the definition in this technical report.

3. History

Recently, as electronic devices become smaller, conventional leaded type packages such as SOP and QFP become unsuitable, and demand for non-leaded type packages makes suppliers develop and commercialize such type of packages. This technical report is in intended to standardize the outer dimensions or “terminal-N” packages and ensure compatibility between products.

For the integration of definitions about dimensions of packages which have leads on both sides or around 4 sides, the packages were overviewed when the design guide was made.

EIAJ EDR-7318 (Design guideline of integrated circuits for P-VSON and **EIAJ EDR-7324** (Design guideline of integrated circuits for P-VQFN) are considered a comment in every country in case of IEC standardization with a standard revision needed in spreading a variation rapidly by the development trend of each company, And added Seated height newly. Also, it considered an outline drawing by the saw cut which are a consistence with JEDEC standard and a technology development trend in recent years, too, and it was created in the addition. As for both standards, it begins a deliberation from September 2001, **EIAJ EDR-7318A** and **EIAJ EDR-7324A** are established in April 2002.

This technical report shows the standard design values on the concept of the design centers as far as possible for standardization.

4. Definition of the P-SON

It is classified into N terminals of second category having the form of A. It's leads are flat and positioned at the bottom in two arrays along the both sides of the package to make it possible to mount on the printed circuit board. This Design guideline defines the plastic package whose mounting height is no higher than 1.20mm. (Metal exposing area is not defined in this report)

5. Numbering of Pins.

In conformity with the definition of **EIAJ ED-7300**.

6. Nominal Dimensions

The package body size (package length: D, package width: E) is regarded as Nominal dimensions.

7. Reference Characters and Drawing

Figure 1 (L_1=0.10)

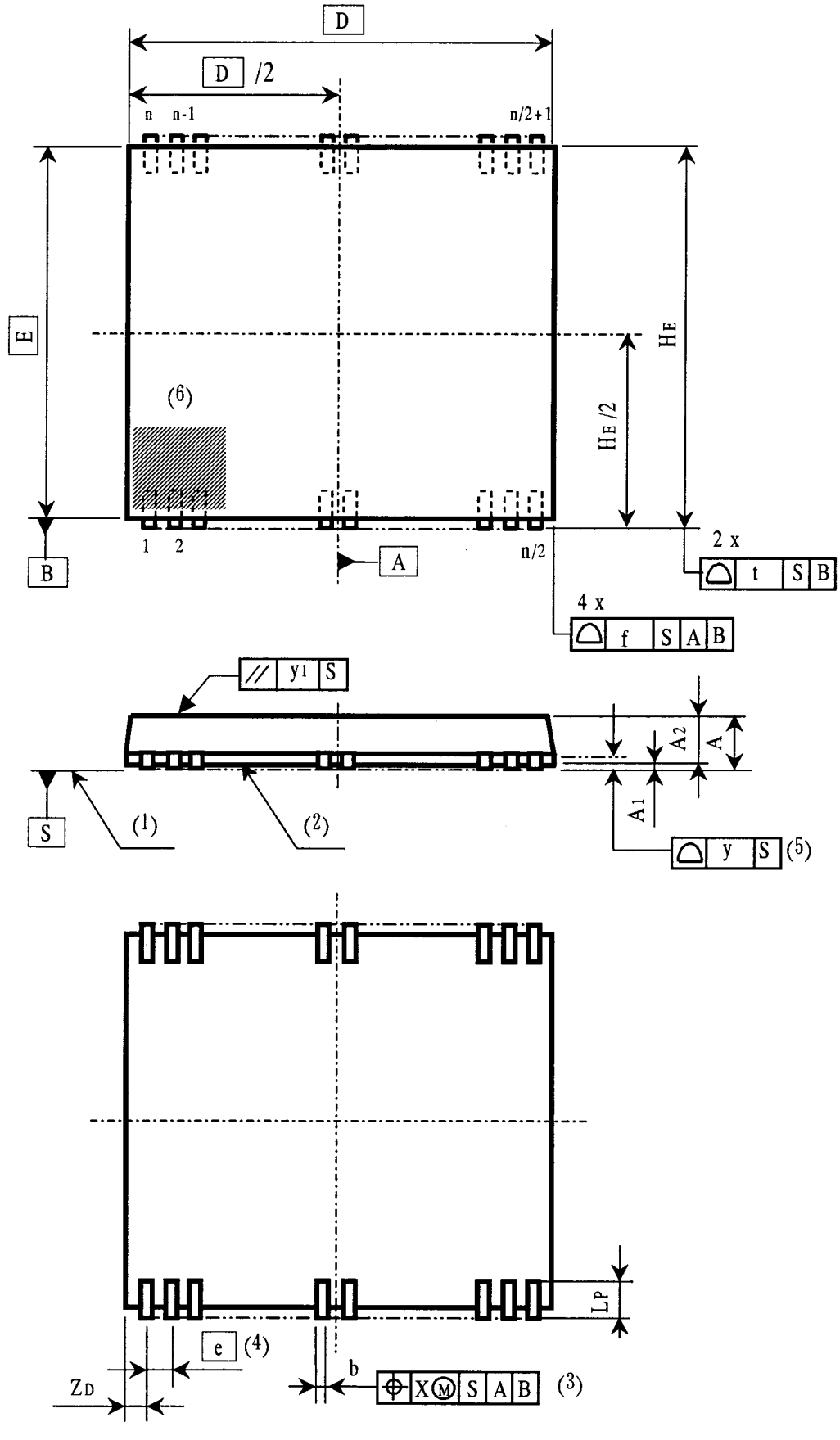
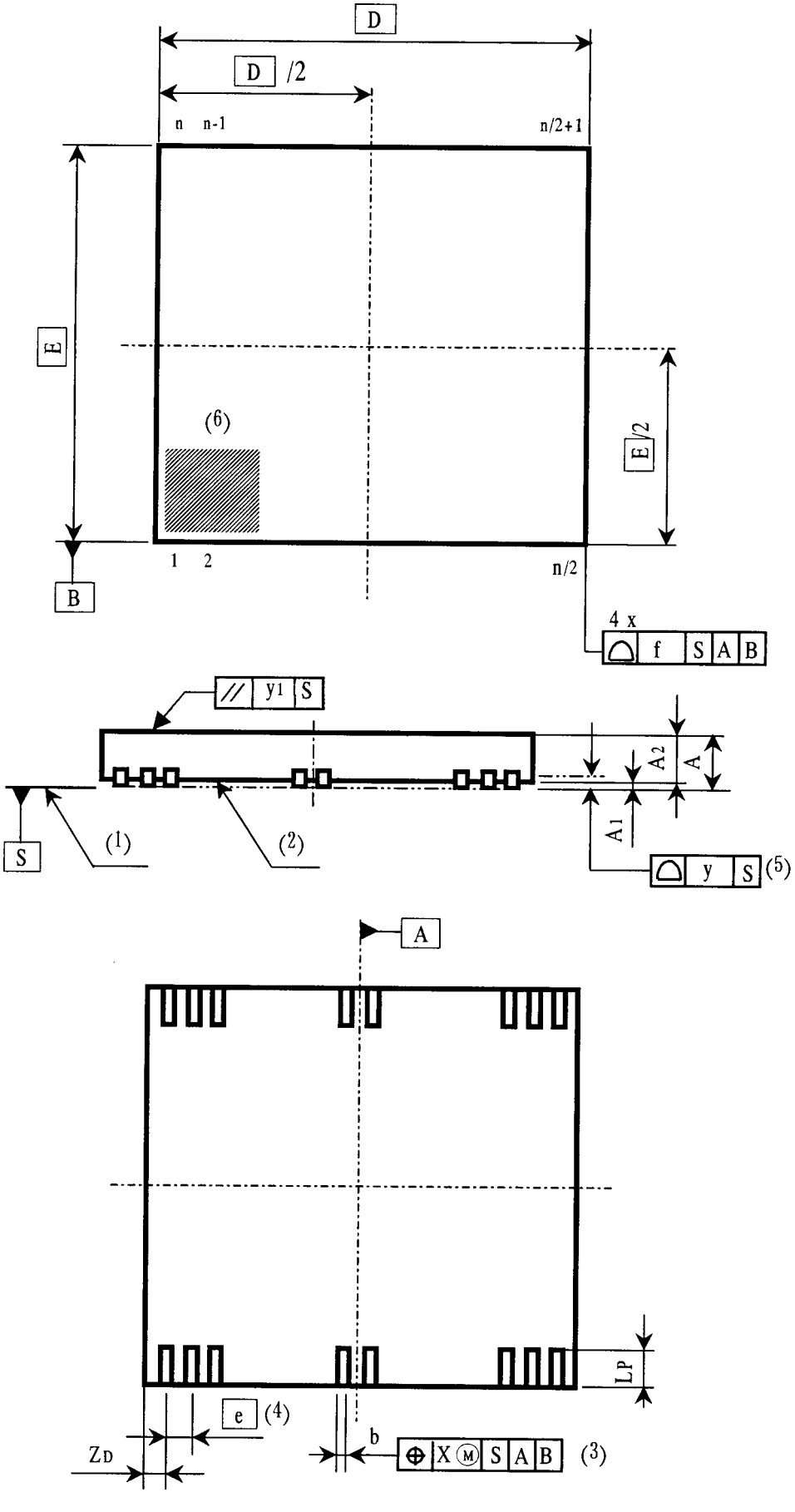
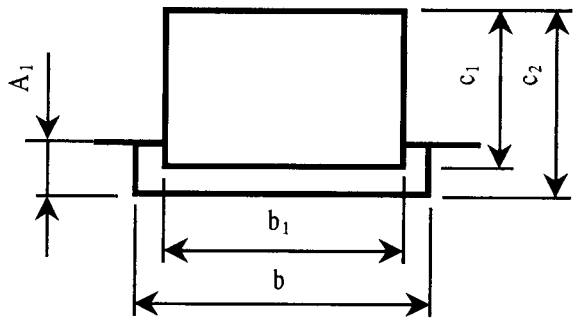


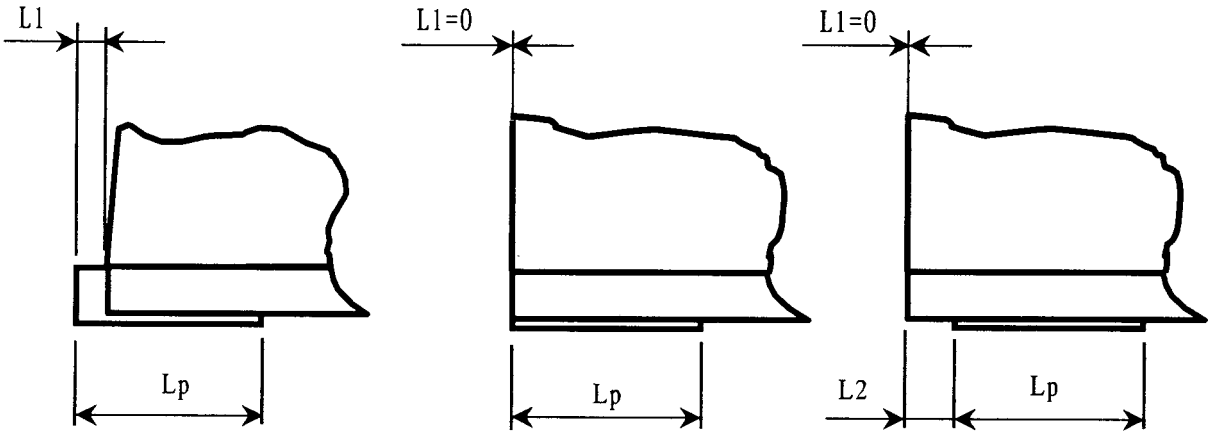
Figure 2 (L_1=0)


D
D /2
n n-1
n/2+1
E
E/2
(6)
1 2
n/2
B
4 x
f S A B
// y1 S
A2
A
A1
S
(1)
(2)
y S
(5)
A
LP
e
(4)
ZD
b
X M S A B
(3)

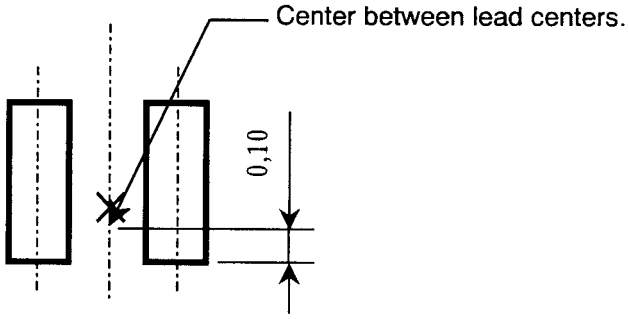
Figire 3



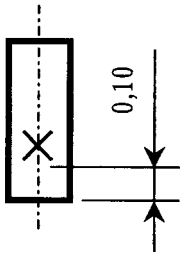
Terminal cross section ([7])



Terminal to be soldered



(a)For even number of leads on a package side.



(b)For odd number of leads on a package side.

The detailed figure (datum target)

Notes

(1) The mounting surface, with which a package is in contact.

(2) The base surface, which is in parallel with the mounting surface and links the lowest points, except the stand-off.

(3) The maximum material requirements apply to the positional tolerance of the terminals.
(For the maximum material requirements, refer to **ISO 2692**/**JIS B 0023**.)

(4) Specifies the true geometric position of the terminal axis.

(5) Specifies the vertical shift of the flat part of each terminal form the mounting surface.

(6) Shows the allowable position of the Index mark area, which is based on the IEC standard and basically 1/16 with package body size, however in case of small package size, it is less than 1/4 with package body size, it must be included in the shaded area entirely.

(7) The dimensions of the terminal section apply to the terminal region ranges of 0.10mm and 0.25mm from the end of a terminal.

8. OUTLINE DIMENSION

Stipulated dimensions of each part are shown below in the **table 1** and **2**.

8.1 Group 1

Table 1

unit: mm

Description	Reference Symbol	Standards	Recomm -ended	Remarks
Nominal dimensions	E×D	※Written below		
Package width	E	Each dimension is identical with the nominal dimensions. E = 2.00, 2.50, 3.00 --- 9.50, 10.00, 11.00, 12.00, 13.00	—	(1) Exclude resin burr. (2) Maximum 0.20 of resin burr or gate burr.
Package length	D	D = 2.00, 2.50, 3.00 --- 9.50, 10.00, 11.00---- 26.00 $D = \{(n/2-1) \times e\} + 2Z_{Dnom}$		Line-up is made every 0.50mm step for 2.00 - 10.00mm, and 1.00mm step for 10.00 - 13.00, 26.00mm
Tolerance of package lateral profile	f	(1) Tolerance of package lateral profile shall be specified in the outline drawing. ⌓ | f | S | A | B (2) Reference symbol "f" shall be replaced as below. f = 0.20	—	
Seated height	A	A: T >1.00 ≦1.20; V >0.80 ≦1.00; W >0.65 ≦0.80; U >0.50 ≦0.65; X ≦0.50	—	Include package warp-age.
Stand-off height	A_1	min 0.00 / nom 0.02 / max 0.05	—	
Package body height	A_2	$A_2 = A - A_1$	—	

Table 1 (continued)

unit: mm

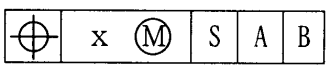
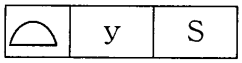
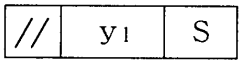
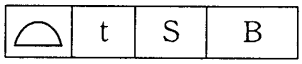
<table>
<tr><th>Description</th><th>Reference Symbol</th><th>Standards</th><th>Recommended</th><th>Remarks</th></tr>
<tr><td rowspan="2">Terminal width</td><td>b</td><td>(1) b shows the terminal width with plating.
<table><tr><th>e</th><th>min</th><th>nom</th><th>max</th></tr><tr><td>1.00</td><td>0.57</td><td>-</td><td>0.67</td></tr><tr><td>0.80</td><td>0.37</td><td>-</td><td>0.47</td></tr><tr><td>0.65</td><td>0.32</td><td>-</td><td>0.42</td></tr><tr><td>0.50</td><td>0.27</td><td>-</td><td>0.37</td></tr><tr><td>0.40</td><td>0.17</td><td>-</td><td>0.27</td></tr></table></td><td>(1) Palladium plating
<table><tr><th>e</th><th>bnom</th></tr><tr><td>1.00</td><td>0.60</td></tr><tr><td>0.80</td><td>0.40</td></tr><tr><td>0.65</td><td>0.35</td></tr><tr><td>0.50</td><td>0.30</td></tr><tr><td>0.40</td><td>0.20</td></tr></table>(2)Solder plating
<table><tr><th>e</th><th>bnom</th></tr><tr><td>1.00</td><td>0.62</td></tr><tr><td>0.80</td><td>0.42</td></tr><tr><td>0.65</td><td>0.37</td></tr><tr><td>0.50</td><td>0.32</td></tr><tr><td>0.40</td><td>0.22</td></tr></table></td><td rowspan="2">(1) b_1 indicates the width of bare lead frame.
(2) b indicates the width of plated lead frame.
(3) Terminal width was made wider than SOP or QFP according to the mounting reliability evaluation result.
(4) b and b_1 are within 0.10～0.25mm range from the end of terminal.
(5) Solder plaing, the standard thickness of solder layer shall be [0.010+0.010/-0.05]. Palladium plating, it is very thin, so terminal width and thickness is bnom=$b_1$nom.</td></tr>
<tr><td>b_1</td><td><table><tr><th>e</th><th>min</th><th>nom</th><th>max</th></tr><tr><td>1.00</td><td>0.57</td><td>0.60</td><td>0.63</td></tr><tr><td>0.80</td><td>0.37</td><td>0.40</td><td>0.43</td></tr><tr><td>0.65</td><td>0.32</td><td>0.35</td><td>0.38</td></tr><tr><td>0.50</td><td>0.27</td><td>0.30</td><td>0.33</td></tr><tr><td>0.40</td><td>0.17</td><td>0.20</td><td>0.23</td></tr></table></td><td>—</td></tr>
<tr><td>Terminal pitch</td><td>e</td><td>e = 0.40, 0.50, 0.65, 0.80, 0.10</td><td>—</td><td></td></tr>
<tr><td>Length of soldered part</td><td>Lp</td><td><table><tr><th>e</th><th>min</th><th>nom</th><th>max</th></tr><tr><td>1.00</td><td>0.7</td><td>1.00</td><td>1.20</td></tr><tr><td>0.80</td><td>0.50</td><td>0.75</td><td>0.90</td></tr><tr><td>0.65</td><td>0.40</td><td>0.65</td><td>0.80</td></tr><tr><td>0.50</td><td>0.35</td><td>0.50</td><td>0.75</td></tr><tr><td>0.40</td><td>0.35</td><td>0.50</td><td>0.75</td></tr></table></td><td>—</td><td>(1) Length of the soldered part Lp was determined by taking the mounting reliability into consideration.</td></tr>
<tr><td>Tolerance of terminal center position</td><td>x</td><td>(1)Tolerance of terminal center position shall be specified in the outline drawing.
 
(2) Reference symbol “x” shall be replace as below.
x = 0.05</td><td>—</td><td>(1) The concept of the maximum material requirements shall be applied.</td></tr>
</table>

Table 1 (continued)

Unit: mm

Description	Reference Symbol	Standards	Re commended	Remarks
Co planarity	y	(1) Co planarity shall be specified in the outline drawing.  (2) Reference symbol "y" shall be replaced as below. y = 0.05	—	
Parallelism of Package top surface	y_1	(1) Parallelism of Package top surface shall be specified in the outline drawing.  (2) Reference symbol "y_1" shall be replaced as below y_1 = 0.20	—	The valve is derived from the manufacturing ability of the suppliers
Positional tolerance of terminal tips	t	(1) Positional tolerance of terminal tips shall be specified in the outline drawing.  (2) Reference symbol "t" shall be replaced as below t = 0.20	—	(1) Include package warp- age.
Number of terminal position	n	※Refer to the **table 4**.	—	(1) Maximum number of terminal when $Z_D \geqq b_1$nom ×1.5 (2) Depopulation is optional.

8.2 Group 2

Table 2

Unit: mm

<table>
<tr><th>Description</th><th>Reference Symbol</th><th>Standards</th><th>Recommended</th><th>Remarks</th></tr>
<tr><td>Package over hang</td><td>Z_D</td><td>∗Refer to the table 4.</td><td>-</td><td>(1) Exclude resin burr or gate burr.
(2) $Z_D \geq b_1$nom x 1.5</td></tr>
<tr><td rowspan="2">Terminal thickness</td><td>c_1</td><td rowspan="2"><table><tr><th></th><th>min</th><th>nom</th><th>max</th></tr><tr><td>c_1</td><td>0.09</td><td>-</td><td>0.21</td></tr><tr><td>c_2</td><td>0.09</td><td>-</td><td>0.25</td></tr></table></td><td rowspan="2">-</td><td rowspan="2">(1) c_1 indicates the thickness of bare laedframe.
(2) c_2 indicates the thickness of plated terminal.
(3) c_1, c_2 are within 0.10 ~0.25 range from the edge of terminal.
(4) Solder plating, the standard thickness of solder layer shall be c_1+0.04/-0.00 . Palladium plating, it is very thin, so terminal width and thickness $c_1$nom=$c_2$nom .</td></tr>
<tr><td>c_2</td></tr>
<tr><td>Overall width</td><td>H_E</td><td>$H_E = \boxed{E} + 2L_1$nom</td><td>-</td><td></td></tr>
<tr><td>Terminal salient length</td><td>L_1</td><td><table><tr><th></th><th>min</th><th>nom</th><th>max</th></tr><tr><td>L_1</td><td>0.00</td><td>0.10</td><td>-</td></tr></table></td><td>L_1max=0.20</td><td>(1) L_1 valve is derived from the manufacturing ability of the suppliers.</td></tr>
<tr><td>To the terminal from-the edge oft he package</td><td>L_2</td><td><table><tr><th></th><th>min</th><th>nom</th><th>max</th></tr><tr><td>L_2</td><td>0.00</td><td>-</td><td>0.15</td></tr></table></td><td>-</td><td>(1) L_2 valve is derived from the manufacturing ability of the suppliers.</td></tr>
</table>

9. Individual standard registration:

To propose new outline for individual standard, necessary information in Form 5 of Technical Standardization committee on Semiconductor Device package administrative provisions is made an entry and proceeded by standard preparation procedure. In which time, package dimension table in the clause 2, Form 5 follows the table below. Dimension is marked where (v) is shown. Also, Outline type should be marked in accordance with **EIAJ ED-7303B**[Name and Code for Integrated Circuits Package].

Table 3

Serial Number				
External Type		P－○SON○○○－○○○○－○. ○○		
Reference Symbol		min	nom	max
Group 1	D		v	
	E		v	
	F			v
	A			v
	A_1	v	v	v
	A_2	v	v	v
	b	v	v	v
	b_1	v	v	v
	e		v(*)	
	Lp	v	v	v
	x			v
	y			v
	y_1			v
	t			v
	n		v	
Group 2	Z_D		v	
	c_1	v		v
	c_2	v		v
	H_E		v	
	L_1		v	
	L_2		v	

(*)Means true geometrical position

Table 4 Package length vs Pin count

unit: mm

D	0.40 Pitch		0.50 Pitch		0.65 Pitch		0.80 Pitch		1.00 Pitch	
	n	Z_D	n	Z_D	n	Z_D	n	Z_D	n	Z_D
2.00	8	0.40	6	0.50	-	-	-	-	-	-
2.50	10	0.45	8	0.50	6	0.600	-	-	-	-
3.00	14	0.30	10	0.50	8	0.525	6	0.70	-	-
3.50	16	0.35	12	0.50	10	0.775	6	0.95	-	-
4.00	18	0.40	14	0.50	10	0.700	8	0.80	6	1.00
4.50	20	0.45	16	0.50	12	0.625	8	1.05	6	1.25
5.00	24	0.30	18	0.50	14	0.55	10	0.90	8	1.00
5.50	26	0.35	20	0.50	14	0.800	12	0.75	8	1.25
6.00	28	0.40	22	0.50	18	0.725	14	0.60	10	1.00
6.50	30	0.45	24	0.50	18	0.650	14	0.85	10	1.25
7.00	32	0.30	26	0.50	20	0.575	16	0.70	12	1.00
7.50	36	0.35	28	0.50	20	0.825	16	0.95	12	1.25
8.00	38	0.40	30	0.50	22	0.75	18	0.80	14	1.00
8.50	40	0.45	32	0.50	24	0.675	20	0.65	14	1.25
9.00	44	0.30	34	0.50	26	0.60	20	0.90	16	1.00
9.50	46	0.35	36	0.50	28	0.525	22	0.75	16	1.25
10.00	48	0.40	38	0.50	28	0.775	24	0.60	18	1.00
11.00	54	0.30	42	0.50	32	0.625	26	0.70	20	1.00
12.00	58	0.40	46	0.50	34	0.80	28	0.80	22	1.00
13.00	64	0.30	50	0.50	38	0.65	30	0.90	24	1.00
14.00	68	0.40	54	0.50	40	0.825	34	0.60	26	1.00
15.00	74	0.30	58	0.50	44	0.675	36	0.70	28	1.00
16.00	78	0.40	62	0.50	48	0.525	38	0.80	30	1.00
17.00	84	0.30	66	0.50	50	0.70	40	0.90	32	1.00
18.00	88	0.40	70	0.50	54	0.55	44	0.60	34	1.00
19.00	94	0.30	74	0.50	56	0.725	46	0.70	36	1.00

Table 4 (continued)

unit: mm

D	0.40 Pitch		0.50 Pitch		0.65 Pitch		0.80 Pitch		1.00 Pitch	
	n	Z_D	n	Z_D	n	Z_D	n	Z_D	n	Z_D
20.00	98	0.40	78	0.50	60	0.575	48	0.80	38	1.00
21.00	104	0.30	82	0.50	62	0.75	50	0.90	40	1.00
22.00	108	0.40	86	0.50	66	0.60	54	0.60	42	1.00
23.00	114	0.30	90	0.50	68	0.775	56	0.70	44	1.00
24.00	118	0.40	94	0.50	72	0.625	58	0.80	46	1.00
25.00	124	0.30	98	0.50	74	0.80	60	0.90	48	1.00
26.00	128	0.40	102	0.50	78	0.65	64	0.60	50	1.00

EIAJ EDR-7318A

Explanation

1. Objective of establishment

This technical report accounts for the industrial standard of Plastic non leaded package(hereinafter called P-SON).

It was established to provide the design guideline of P-SON when it is made into product or when automatic mounting machinery and associated parts are developed.

2. Background

As systems get smaller, many companies started to develop non leaded package that does not have protruding leads as SOP and QFP have by arranging leads at the bottom of the package. Non leaded package needed to have an industrial standard as SOP or QFP. So, Technical Standardization Committee on Semiconductor Device Package organized a project of standardization of non lead package in November 1997 and standardization of P-VSON AND P-VQFN went on till June 1998.

Referring to the existing design guide of SOP and QFP for basic parts, standardization went on to make tolerance or dimensions of P-VSON and P-VQFN are identical as possible even for the unique part of non lead package.

EIAJ EDR-7318 and **EIAJ EDR-7324** are considered a comment in every county in case of IEC standardization with standard revision needed in spreading a variation rapidly by the development trend of each company,and added Seated height newly.Also,it consider an outline drawing by the saw cut which is a consistence with JEDEC standard, **MO-229**(Thermal Heat-sink V/WDFPN), **MO-220**(Thermal Heat-sink V/WQFN) and technology development trend in recent years,too, And it was created in the addition. As for both standards, it begins a deliberation from September 2001, **EIAJ EDR-7318A** and **EIAJ EDR-7324A** are established in April 2002

Datum set up method, definition of tolerance of dimension, etc. are in conformity with **EIAJ ED-7300**.

3. Key points.

(1) Nominal dimension(E X D): The old standard was E = 5.00mm minimum, and D = 7.00mm minimum.

This technical report is changed nominal dimension is E, D = 2.00mm minimum.

The reason to change these is that the development of small size packages is advanced.

(2) Package height(A): Old **EIAJ EDR-7318** taking advantage of the characteristic of Non-leaded packages, it is defined to have 1.0mm maximum.This technical report is added T, V, W, U, X with considered of IEC standard and accordance with **EIAJ ED-7303B** [Name and Code for Integrated Circuits Package].

(3) Stand-off(A_1): To indicate that the leads are not buried in the package, it is defined 0.0 minimum. To indicate that more than half of the sides of the lead is protected by resin, it is defined to have 0.05mm maximum.

(4) Terminal width(b, b_1): Taking the mounting reliability into consideration, These are defined to have wider width than those of SOP and QFP.

(5) Thickness of terminal(c_1, c_2): The part of a lead that is to be mounted is buried under resin, terminal thickness is defined as c_2 equals to thickness of bare leadframe(c_1) + bottom plating.

It is difficult to measure by non-destructive method so that dimensions of material is shown in Group 2.

(6) Terminal pitch(e): It is defined to have five kinds of practical dimension: 1.00/0.80/0.65/0.50/0.40.

(7) Positional tolerance of terminal center (X): Owing to the fact that it is non-leaded package, it is defined to have integrated tolerance value regardless of pitch.

(8) Terminal co planarity (y): Owing to the fact that it is non-leaded package, it is defined to have integrated co planarity value regardless of pitch.

(9) Number of terminal (n): Defined as maximum number of terminal acquired when Overhang(Z_D) terminal width(b_1) X 1.5. Depopulation of leads in both ends of arrays is optional with no depopulation in-between because of the risk that it would affect the mounting reliability.

(10) Length of the soldered part (Lp): Taking the mounting reliability into consideration, it is defined with repect to individual pitch.

(11) Length of protrusion of terminal (L_1): Defines the protruding length from the package.

L_1min=0.00mm in addition to L_1nom=1.00mm .

(12) To the terminal from the edge of the package (L_2): In case of the saw cut method, the terminal drags from the end of the package and sometimes designs, too. L_2 is defined to be length to the terminal which was dragged from the end of the package and L_2 min = 0.00mm, L_2max = 0.15mm which adjustment with the JEDEC standard were considered.

(13) Overall with (H_E): Overall width indicate means true geometrical position (H_E) in old **EIAJ EDR-7318**. **EIAJ EDR-7318A** not indicate means true geometrical position (H_E).It added H_E = E + L_1 ,and it moved in Group 2.

(14) Pattern of terminal areas : At old **EIAJ EDR-7318**, pattern of terminal areas can exist was shown Figure as reference for the foot print design. However , this technical report is delated because becomes complex of length of protrusion of terminal (L_1) and to the terminal edge of the package (L_2) which provides newly.

4. With regard to Industry proprietorship

This general principle includes the patent pending by Fujitsu(published number 6-132453) and by LG semicon (application number 9-254578).

5. Review committee members

This technical report has been reviewed mainly by IC Package Sub-Committee and Project Group of Semiconductor Package Standardization Committee.

A detailed discussion of the standard started PJ, and executed a special committee in addition.

The members are as shown below.

<Technical Standardization Committee on Semiconductor Device Packages>

Chairman	SONY CORP.	Kazuo Nishiyama

<IC Package Sub-committee>

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Co- Chief	HITACHI LTD.	Yoshinori Miyaki
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