

Technical Report of Electronic Industries Association of Japan

EIAJ EDR-7320

Design guideline of integrated circuits for Small Outline Packages (SOP)

Established in December, 1998

Prepared by

Technical Standardization Committee on Semiconductor Device Package

Published by
Electronic Industries Association of Japan

5-13, Nishi-shinbashi 1-chome, Minato-ku, Tokyo 105-0003, Japan Printed in Japan Standard of Electronic Industries Association of Japan

Design guideline of integrated circuit for Small Outline Package (SOP)

1. Scope of application

This standard regulated outline drawings and dimensions of small outline package (hereinafter referred to as SOP), especially plastic package, classified as form 1 under the EIAJ ED-7300 (standard for preparing standard outline drawings (integrated circuit) of semiconductor devices).

Note This technical report is revised edition of EIAJ ED-7402.

2. Terminology

The definition of the terms used in this technical report complies with the EIAJ ED-7300. New terms will defined in the description of this technical report.

3. History

Recently, electric appliances become smaller and thinner, the demand for surface mount devices are increasing rapidly. This design guideline is intended to standardize the outer dimensions of SOPs and ensure compatibility between products. It shows the standard design values on the concept of the design centers as far as possible for standardization.

4. Definition of SOP

SOP is classified as form B with L terminal in the item 6, "Outline classification of the semiconductor packages" of the EIAJ ED-7401A, and defined a package with formed terminals led out of the longer sides of itself of in two directions, whose terminal pitch is over 1.0mm, are flat toward the outside of the package body for mounting on PCB surface.

5. Designation of the pin number

Numbering of terminal complies with the EIAJ ED-7300.

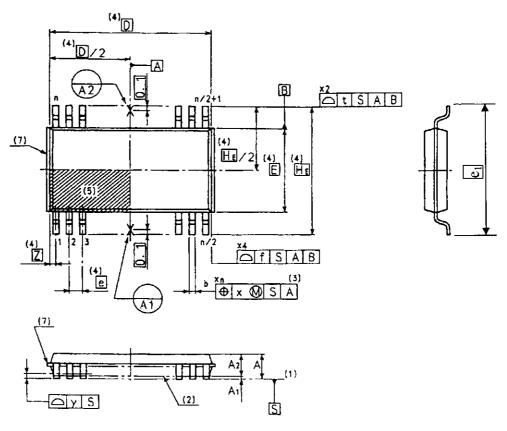
6. Nominal dimensions

The dimension of package width (Symbol : e_1) is applied to nominal dimension.

7. REFERENCE CHARACTERS AND DRAWINGS

7.1 Outline Drawings

Figure 1



Detail area of datum A

For even number of terminals on a package side

For odd number of terminals on a package side

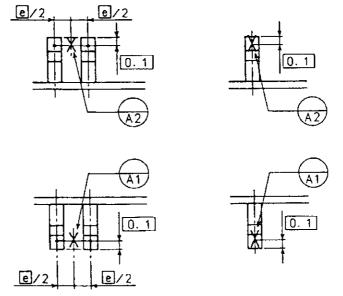
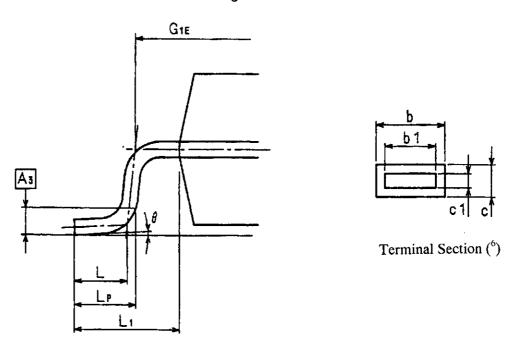


Figure 2



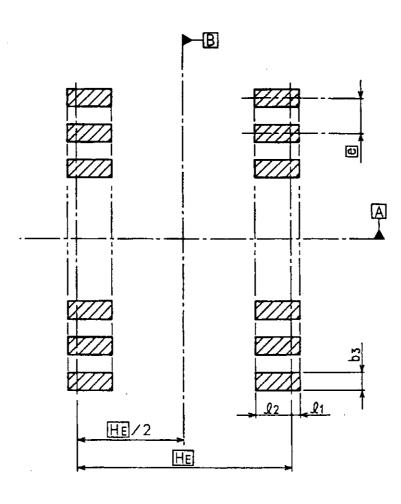
Note (1) The mounting surface, with a package is in contact.

- (2) The base surface, which is in parallel with the mounting surface and links the lowest points of package, expect the stand-off.
- (3) The maximum mounting conditions apply to the positional tolerance of the terminals. (For the maximum body conditions, refer to ISO 2692/JIS B 0023)
- (4) Specifies the true geometric position.
- (5) Shows the allowable position on the index mark. More than half area of the index mark must be included in the shade area.
- (b) The dimensions of the terminal section apply to the range of 0.1mm and 0.25mm from the end of a terminal.
- (7) Resin burrs and gate remains of thee package sides with no terminals are 0.15mm MAX per side.
- (8) Resin burrs of the terminal sides are 0.25mm MAX per side.

7.2 ALLOWABLE RANGE OF SOLDERING PART OF TERMINALS

The range where the terminals to be soldered can exist is shown in Figure 3 as reference for the foot print design.

Figure 3



$$\ell_{2max} = L_{Pmax} + t/2$$

$$b_{*m*x} = b_{m*x} + x$$

8.1 OUTER DIMENSION

Table 1

GROUP 1			1	Unit mm
Description	Symbol	Standards	Recommended Values	Remarks
Nominal dimensions	၉၂	225mil:(5.72) 300mil:(7.62) 375mil:(9.53) 450mil:(11.43) 525mil:(13.34) 600mil:(15.24)		
Package width	E	e1 min max 225mil 3.92 4.72 300mil 5.02 6.22 375mil 6.33 8.13 450mil 8.23 10.03 525mil 10.14 11.94 600mil 12.04 13.84	e ₁ nom	 Mismatch of the upper and lower dies and resin burrs aren't included. It is recommended that upper and lower cavities be equal. If they are different,
Package length	D	$\begin{array}{c cccc} n & D_{max} \\ \hline 6/8 & 6.05 \\ \hline 10/12 & 8.59 \\ \hline 14/16 & 11.13 \\ \hline 18/20 & 13.67 \\ \hline 22/24 & 16.21 \\ \hline 28 & 18.75 \\ \hline 30/32 & 21.29 \\ \hline 36 & 23.83 \\ \hline 40/42 & 27.64 \\ \hline 44 & 28.91 \\ \hline \end{array}$	$\begin{array}{c cccc} n & D_{nom} \\ \hline 6/8 & 5.08 \\ \hline 10/12 & 7.62 \\ \hline 14/16 & 10.16 \\ \hline 18/20 & 12.70 \\ \hline 22/24 & 15.24 \\ \hline 28 & 17.78 \\ \hline 30/32 & 20.32 \\ \hline 36 & 22.86 \\ \hline 40/42 & 26.67 \\ \hline 44 & 27.94 \\ \hline \end{array}$	the larger dimension shall be regarded.
Overall width	H _E	e1 min max 225mil 5.72 6.99 300mil 7.62 8.89 375mil 9.53 10.8 450mil 11.43 12.7 525mil 13.34 14.61 600mil 15.24 16.51	e ₁ nom 225mil 6.22 300mil 8.42 375mil 10.33 450mil 12.23 525mil 14.14 600mil 16.04	
Stand-off height	A_1	$A_{1min} = 0$	min nom max 0.05 0.15 0.25	:
Package height	A_2	$A_2 = 1.01 \sim 4.00$	$A_{2\text{nom}} = 1.2$ 1.4 1.7 2.7	
Tolerance of package edge	f	$f_{max} = 0.20$		

Table 1 (Continued)

\sim $^{\circ}$	\sim	TT	- 1
1 TK		1 1	- 1

Unit mm

OKOUI I				Unit mm
Description	Symbol	Standards	Recommended Values	Remarks
Standard height of soldered points	A ₃	$\underline{\mathbf{A}_3} = 0.25$		
Terminal pitch	е	e = 1.27		Determines the true geometric position.
Length of soldered part	Lp	$ \begin{array}{c cccc} L_1 & min & max \\ \hline 1.0 & 0.45 & 0.75 \\ \hline 1.6 & 0.73 & 1.03 \\ \end{array} $	$ \begin{array}{c cc} L_1 & nom \\ \hline 1.0 & 0.6 \\ \hline 1.6 & 0.88 \\ \end{array} $	
Terminal	b	min max 0.35 0.51	1. Pb / Sn Plating b _{nom} = 0.42 2. Pd Plating b _{nom} = ().4()	1. b,c includes surface treatments. b1,c1 denotes the raw material dimensions. 2. b,b ₁ ,c and c ₁ apply to
width	b ₁	min max 0.35 0.47	$b_{1nom} = 0.40$	the ranges of 0.1 and 0.25 from the end of a terminal. 3. Values b,c apply to Pb/Sn solder plated
Terminal	c	min max 0.10 0.35	1. Pb / Sn Plating c _{nom} = 0.17 2. Pd Plating c _{nom} = 0.15	terminal. The standard thickness of the solder layer shall be 0.010+0.010/-0.005. As Pd plating, it is
thickness	c ₁	min max 0.10 0.31	$c_{1nom} = 0.15$	very thin so terminal width is $b_{\text{nom}} = b_{\text{1nom}}$ $c_{\text{nom}} = c_{\text{1nom}}$
Terminal angle	0	$\begin{array}{c cc} min & nom & max \\ \hline 0^{\circ} & & 15^{\circ} \end{array}$	min nom max 0° 3° 8°	
Tolerance of terminal center position	х	$\mathbf{x}_{\text{max}} = 0.13$	$\mathbf{x}_{\text{max}} = 0.12$	
Coplanerity	y	$y_{\text{max}} = 0.15$	$y_{\text{max}} = 0.1$	
Positional tolerance of terminal tips	t	$t_{max} = 0.20$		

8.2

Table 1

GROUP 2	

Unit	mr

GROUP Z		T-1		Unit mm
Description	Symbol	Standards	Recommended Values	Remarks
Package overhang	Z		$Z_{\text{nom}} = 0.635 \text{ or } 1.27$	Resin burrs or residual gates are not Included.
Length of flat part of terminal	L	$L_{\min} = 0.25$	L ₁ nom 1.0 0.5 1.6 0.8	
Terminal length	L_1	$L_{1min} = 0.76$	e1 nom 225mil 1.0 others 1.6	
Width between first bent part of terminal	G_{1E}	$\begin{array}{c cccc} & & & & & & \\ L_1 & & & & & \\ \hline 1.0 & & E + 0.8 & \\ \hline 1.6 & & E + 1.4 & \\ \hline \end{array}$		Used for designing a test socket, tray, etc.

9. Individual standard

When you need to register a new outline specification on the standard, complete the appendix format 5 in Technical Standardization Committee on Semiconductor Device Package steering rule, in compliance with the Standardization Rule.

In order to make a package dimension table, which comes under Item 2, Appendix format 5, fill the dimensions marked with (\checkmark) in the following table 2.

table 2

Serial I	Number			
Extern	al Type		000×000 0.0 - 0000 -	
Syn	nbol	min	nom	max
	D		✓	
	E		1	
	A ₂	1	√	1
	A_1	✓	✓	1
	A			1
	A ₃		✓	
	b	1		1
	b ₁	✓	1	1
	С			1
Group 1	c_1	1	✓	1
	0	1	✓	1
	H _E		1	
	Lp	1		1
	e		1	
	t			1
	f			1
	Х			1
	. <u>y</u>			1
	n		1	
	Z		1	
Group 2	I.		1	
2.04p 2	L ₁		.	
	G_{1E}		1	

Explanatory notes

1. Purpose of establishment

This technical report is establish to provide the industrial standards for small outline packages (to be referred to as SOPs hereinafter) and design guidelines in producing the SOPs and developing the automatic mounting machines and related parts.

2. Progress of deliberation

EIAJ ED-7402-1 which is the general rule for SOP outlines which is the forerunner of this technical report is established and issued in February 1989. EIAJ ED-7402-1 will be abolished by the lapse of ten years in 1999, this technical report was reconsidered by the design guideline in Plastic Package Subcommittee. The recommended values, which were based on EIAJ ED-7402-1, of this design guide was shown as impossible as in this revision.

3. Basic idea

(1) Datum

The datum and geometrical tolerance were adopted from this technical report. In adopting the datum, we referred to the JEDEC standards for various packages, and registered packages. For the datum in package length, a point 0.1mm inside the terminal nose at the package center was set as datum target, sharing a tolerance for the terminal center position.

4. Background for the dimensional specifications

(1) Package width (E)

The lead length is 1.0mm in case of nominal dimension 225mil, lead length is 1.6mm in other case., the recommended value of package width, what is based on that lead length, is newly set, because the old standard was set wide range and an old recommended value was nothing.

(2) Package length (D)

As only maximum value of package length was shown, the nominal value which becomes a design guide was shown newly. And the number of the maximum terminals increases from 42 to 44, a new package length is added. Since the resin burr and the gate remainder at the end face directly affect an outer dimension, they must be 0.15 at maximum on single side (the same specification as the JEDEC).

(3) Package height (A₂)

The range of standard dimension of design guideline is from 1.01 to 4.00 same as of ED-7402-1, the nominal dimensions of package height are decided 1.2,1.4,1.7 and 2.7.

(4) Terminal width, Terminal thickness (b, b₁, c, c₁)

Terminal width before treatment is newly shown, because terminal width after treatment was shown and to deal with extremely thin plating other than solder plating, for which a demand is expected to increase in the future. The nominal dimension of terminal width after treatment is shown nominal dimension of Pb/Sn and Pd plating.

(5) Length of flat part of terminal, Terminal length, Length of soldered part (L, L₁, L_P) The recommended values of length of flat part of terminal (L), terminal length (L₁) and length of soldered part (L_P) are prescribed (L, L₁, L_P)= (0.5, 1.0, 0.6) at nominal dimension 225mil, (L, L₁, L_P) = (0.8, 1.6, 0.88) at other nominal dimensions, because of making design guide clear. The length of soldered part (L_P) is added in standard.

5. Committee Member

This technical report has been discussed by the Plastic Subcommittee of Technical Standardization Committee on Semiconductor Device Package. The member are as shown below.

<Technical Standardization Committee on Semiconductor Device Package>

Chairman Shouzou Minamide SHARP CORPORATION

<Plastic Package Subcommittee>

Chairman Kaoru Sonobe NEC Corp.
Co-chairman Takashi Okada Toshiba Corp.

Takahiro Imura Texas Instruments Japan Ltd.

Members Young Jun Roh LG Electronics Japan Inc.

Hideo Shimada Enplas Corp.

Kazuhiko Sera Oki Electronic Industry Co., Ltd.

Hideyuki Iwamura Sanyo Electronic Co., Ltd.

Takayuki Nagumo Sumitomo 3M, Ltd. Akitoshi Hara Seiko Epson Corp.

Toshihiko Nojiri Sony Corp. ihiko Murayama Sony Corp.

Kenji Kanesaka Nippon Steel Semiconductor Corp.

Tsuneo Kobayashi IBM Japan, Ltd. Tsukasa Ito AMP Japan, Ltd.

Hiroaki Hirao Samsung Electronics Japan Co., Ltd.

Kenichi Kurihara NEC Corp.

Nobuo Sato Motorola Japan Ltd.

Nobuya Kanemitsu Hitachi Ltd. Masanori Yoshimoto Fujitsu Ltd.

Osamu Hirohashi Fuji Electric Co., Ltd.

Shigeki Sakaguchi Matsushita Electronics Corp.
Kou Shimomura Mitsubishi Electronic Corp.
Nanahiro Hayakawa Yamaichi Electronics Co., Ltd.

Hitoshi Matsunaga Unitechno Inc. Kazumi Morimoto Rohm Co., Ltd.