EIAJ EDR-7323A

JEITA

Technical Report of Japan Electronics and Information Technology Industries Association

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Design guideline of integrated circuits for Pin Grid Array (PGA)

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Design guideline of integrated circuits for Pin Grid Array (PGA)

1. Scope of Application

This technical report regulated which among the packages classified as form D in the **EIAJ ED-7300** [Recommended practice on Standard for the preparation of outline drawings of semiconductor packages]. Pin Grid Array (hereinafter referred to as PGA) which is applied terminal pitch e = 2.54mm and Shrink pitch Pin Grid Array (hereinafter referred to as SPGA) which is applied 1.27mm, and the ceramic and plastic are main constituent in the package body material which excludes a terminal part. This technical report provides about those outline drawings and dimensions.

Note: This technical report is the revision version to have integrated the following two standards into. Also, correspond to this technical report, **EIAJ ED-7311-23** (Standard of integrated circuits package (PGA)) was established in June 2002, newly.

EIAJ ED-7408A (General rules for the preparation of outline drawings of integrated circuits, Pin Grid Array Packages) established in April 1998 and revised in February 1994.

EIAJ EDR-7323 (Design guideline of integrated circuits for Shrink pitch Pin Grid Array) established in May 1999.

2. Definition of the Technical Terms

The definition of the technical terms used in this technical report is in conformity with **EIAJ ED-7300**, and the definition of technical terms appearing a new are given within the text of this standard.

3. BACKGROUND

In recent years, it corresponds to the multifunction of the electronic equipment; the demand to the numerous pin package is increasing rapidly. It answers the demand, at first, PGA appeared that of terminal pitch e = 2.54mm (100mil), and which the pin insertion type to into the printed circuit board through hall. And it is possible to make more numerous pins, SPGA appeared that of terminal pitch e = 1.27mm(50mil), and which the surface mount type of the printed circuit board in the same way Quad Flat I – lead package (QFI). This standard intended to standardize the outer dimensions of PGA and ensure compatibility between products as far as possible for standardization.

4. Definition of PGA, SPGA

It calls with "PGA" in case of terminal pitch e = 2.54mm (100mil), and "SPGA" in case of terminal pitch e = 1.27mm(50mil). Form D with pin terminal in the item 7, “Outline classification of shapes of semiconductor package “ at the **EIAJ ED-7300**. The package pin terminal which was arranged in pin grid array format, and it heads for the seating plane from the base plane of the package body, it be possible to mount to the printed circuit board.

C- (S)PGA The main constituent of the package body material which excludes a terminal part is a ceramic.

P- (S)PGA The main constituent of the package body material which excludes a terminal part is plastic.

IPGA Interstitial PGA, terminal arranges zigzag.

5. Numbering of Terminals

According to **EIAJ ED-7300** rules, Index is positioned at the lower left corner of the package body when it is viewed from the seating plane. A row that is the closest to the index corner is named, A, and as the row moves further away from the index the rows are named, B, C, ... AA, AB, ... Also, a column that is the closest to the index corner is numbered 1, and as the column moves further away to the right, they are numbered 2, 3,.....The numbering of terminals are named by these combinations A1, B1,..... In naming the rows, the letters I, O, Q, S, X, and Z should not be used.

6. Nominal Dimensions

The number of the matrix (Symbol : M) is applied to Nominal Dimensions. "M_E " is the number of the matrix which the direction of the package width (E) , "M_D " is the number of the matrix which the direction of the package length (D).

7. REFERENCE CHARACTERS AND DRAWING

7.1 Outline Drawing

Figure 1 (PGA, Cavity up)

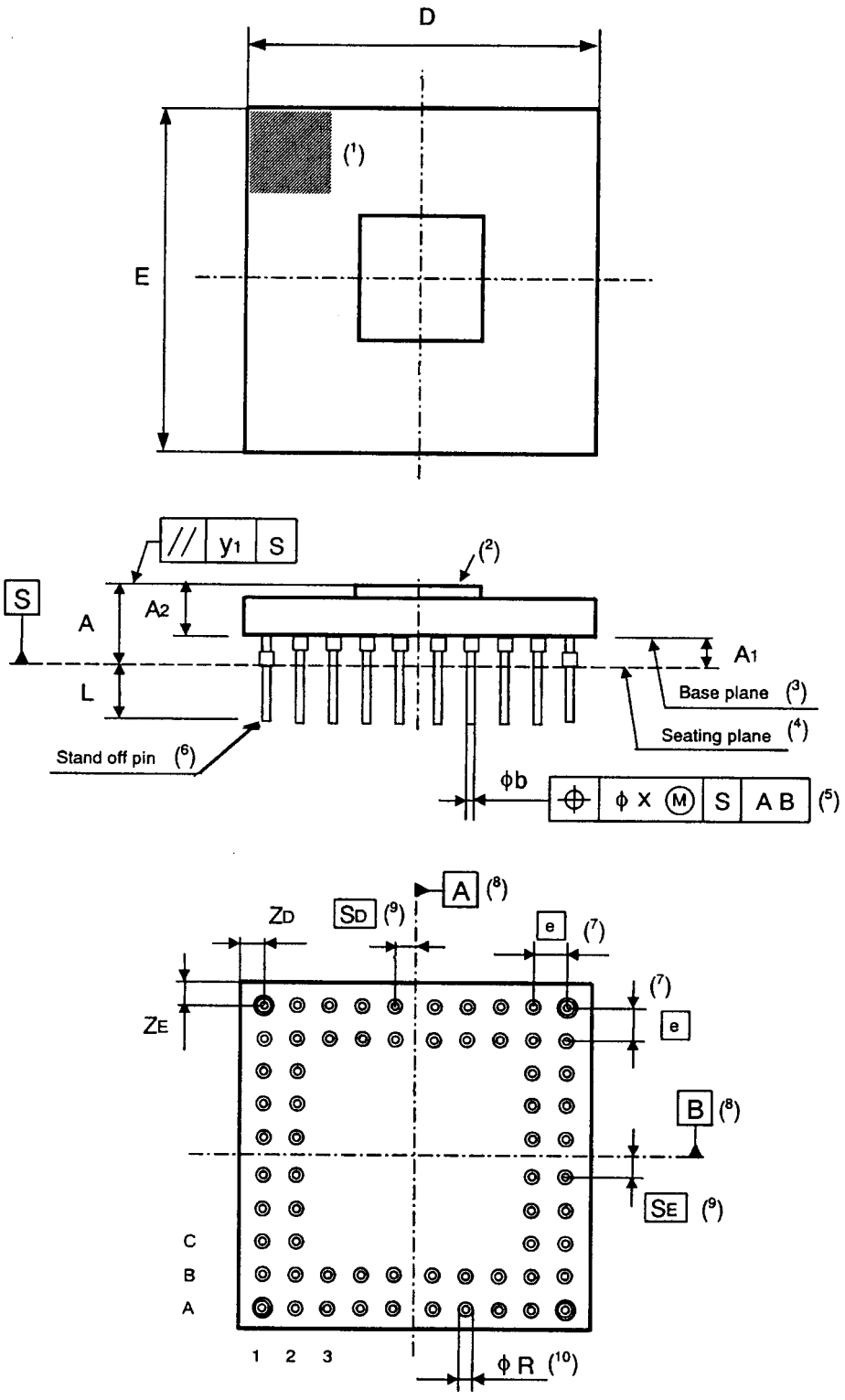


Figure 2 (PGA, Cavity down)

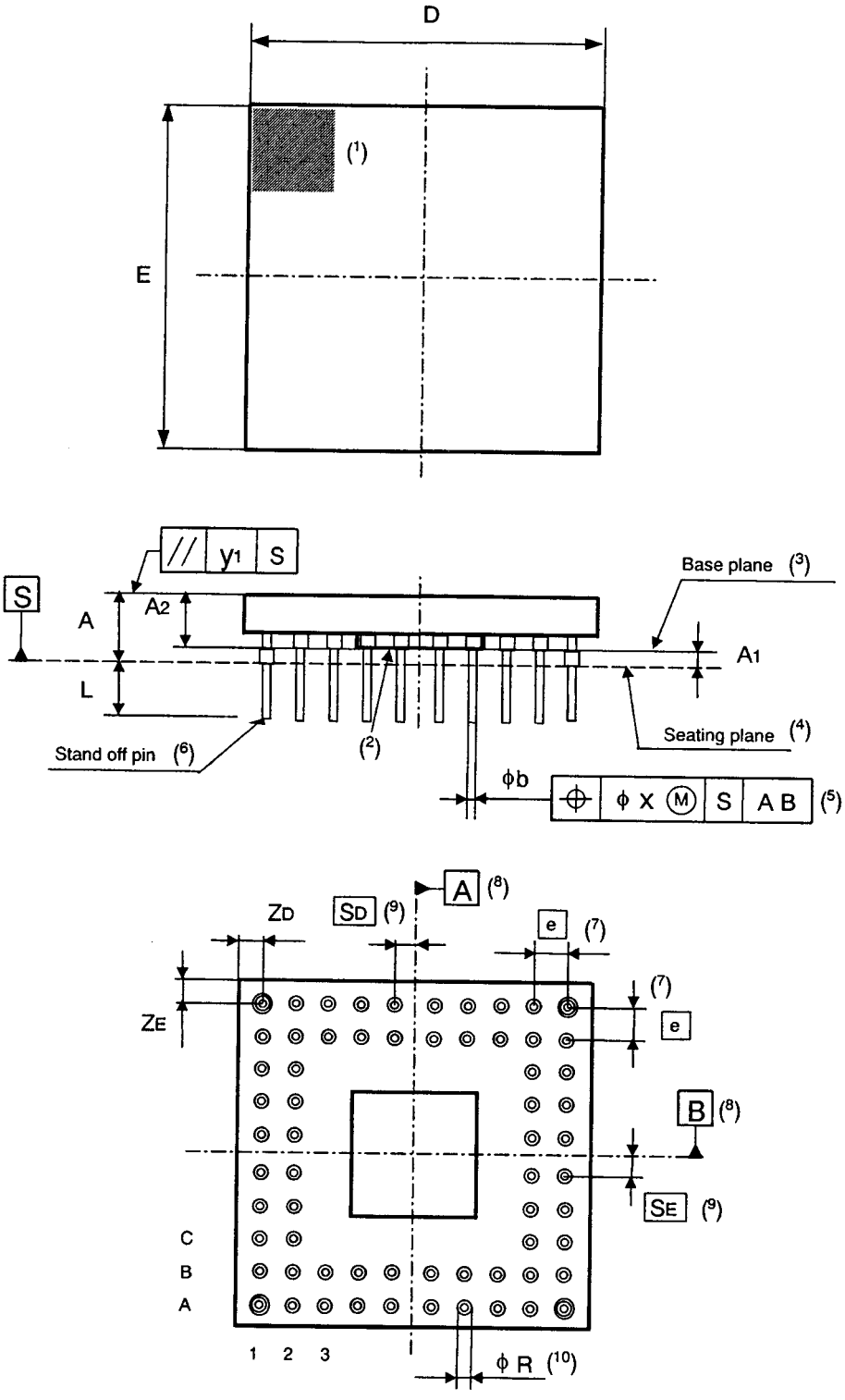


Figure 3 (SPGA, Cavity up)

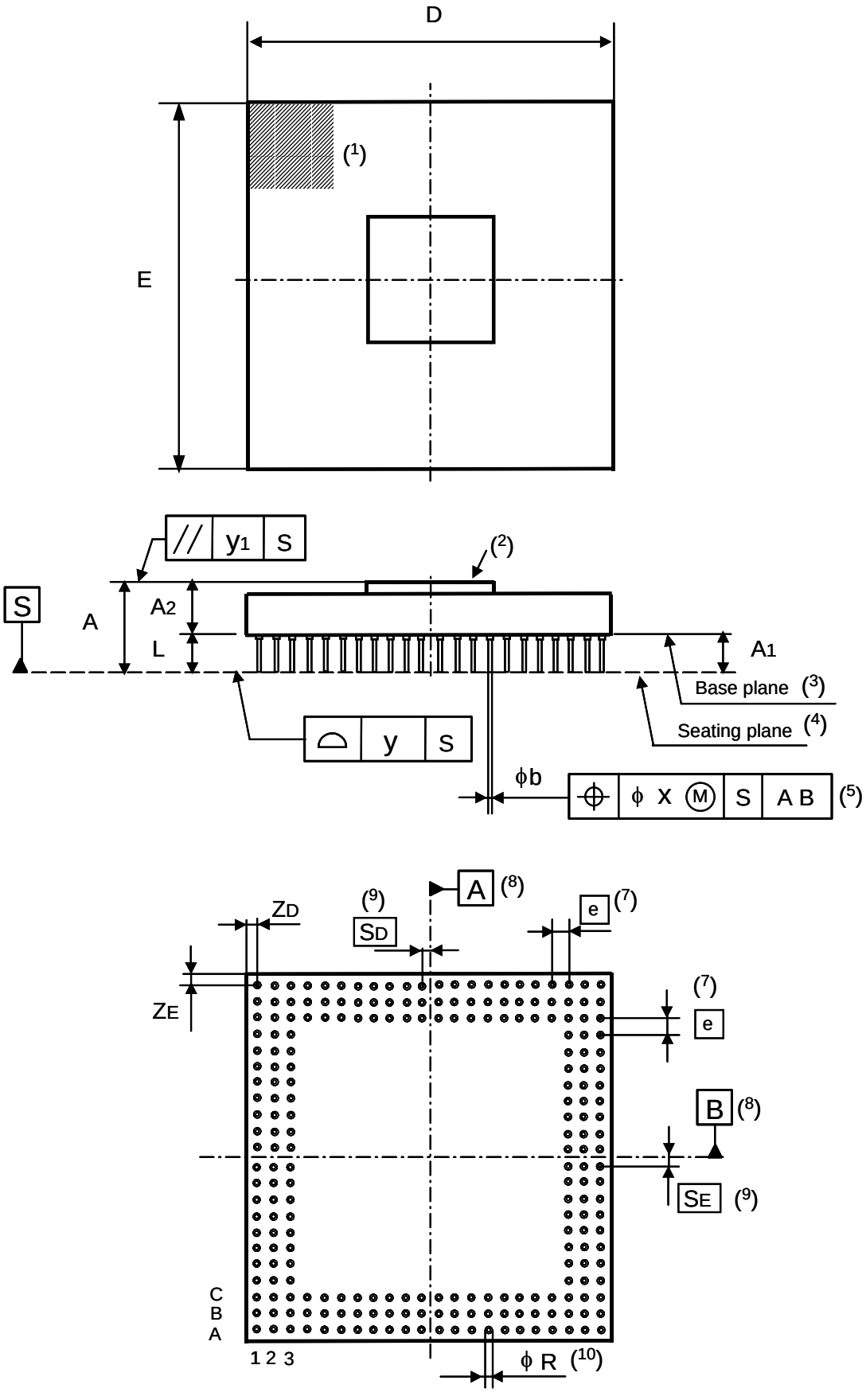


Figure 4 (SPGA, Cavity down)

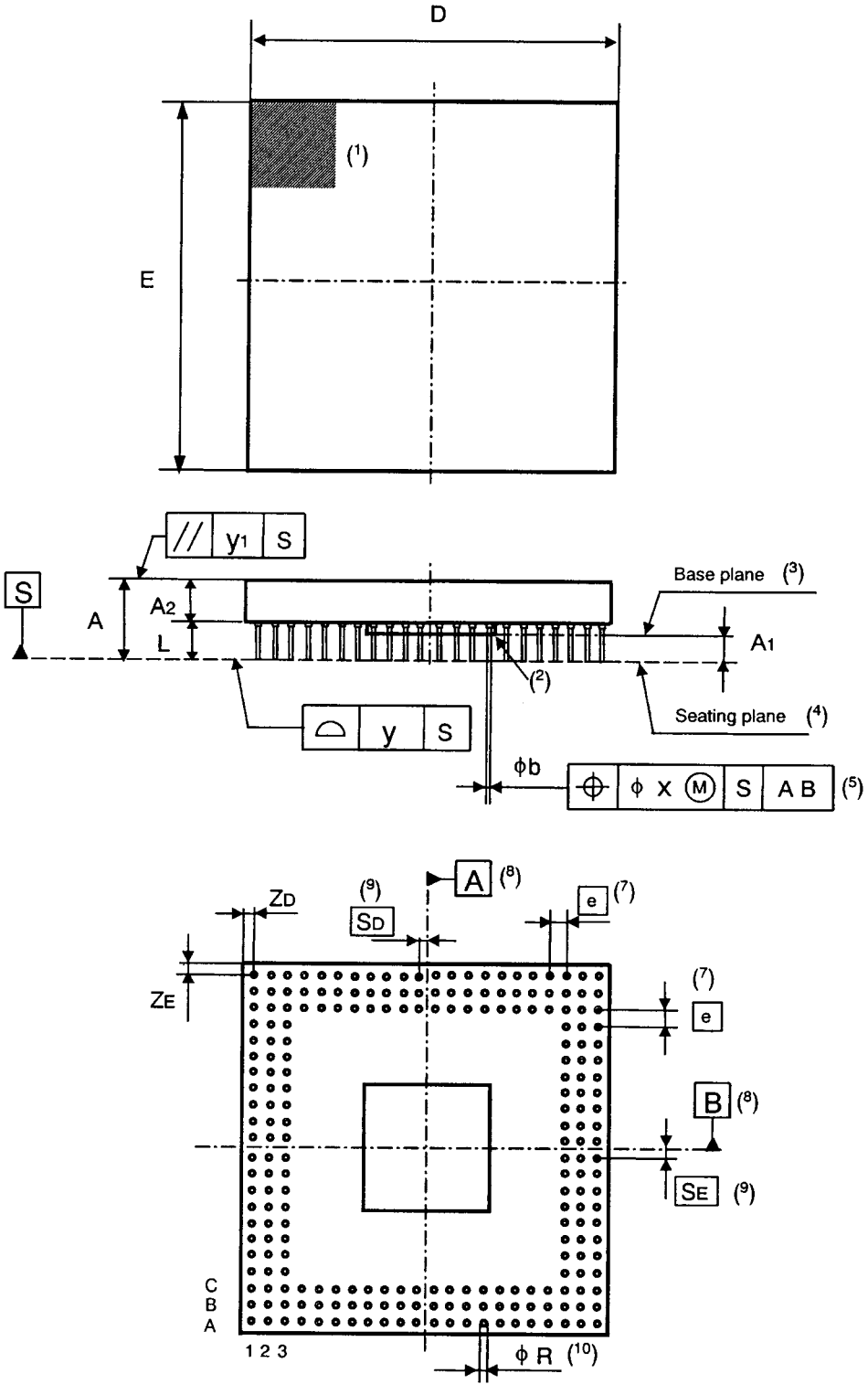


Figure 5 Terminal cross section

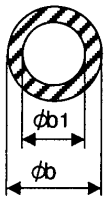
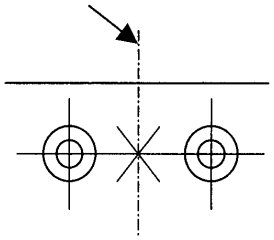


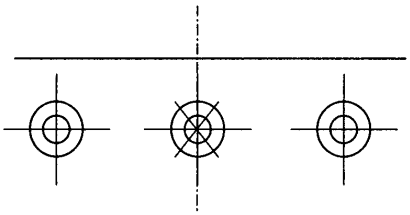
Figure 6 The detailed figure (target of datum A, B)

For even number of terminals on a package side

Center between lead centers



For odd number of terminals on a package side



Note:

([1]) Shows the allowable position of the Index mark area, which is basically 1/16 with package body size, however in case of small package body size, it is less than 1/4 with package body size, It must be included in the shaded area entirely.

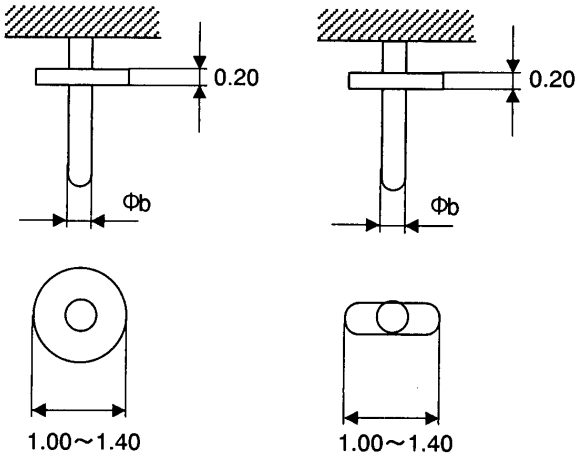
([2]) Indicates Lid (cap). Lid (cap) may consist material of metal, epoxy resin, ceramic. It is called "Lid" which flat to the package surface. And it is called "Cap" which 凸 shape or 凹 shape to the package surface.

([3]) The base plane, which is in parallel with the seating plane and links the lowest point, except the stand off.

([4]) The seating plane, with which a package is in contact.

([5]) The maximum material requirements apply to the positional tolerance of the terminals.
(Refer to **ISO 2692/JIS B 0023**.)

([6]) The recommendation shape and the recommendation size of the standoff pin are shown. It applies a standoff pin to PGA (e =2.54mm) as the option. (It doesn't apply to SPGA(e =1.27mm)). The standoff pin must exist in the position of the object in the diagonal line of the terminal grid arrangement.



([7]) Terminal pitch (e) specifies the true geometric position of the terminal axis.

([8]) It connects respectively the terminal of center which is opposite to each side of package, it finds the angle β to accomplish, mixing. It looks for as it divides $|90^\circ - \beta|$ which deference between the β and 90° , to each side equally a orthogonal axis. It defined datum lines A , B of package. (See, Explanatory notes **3. Basic idea**)

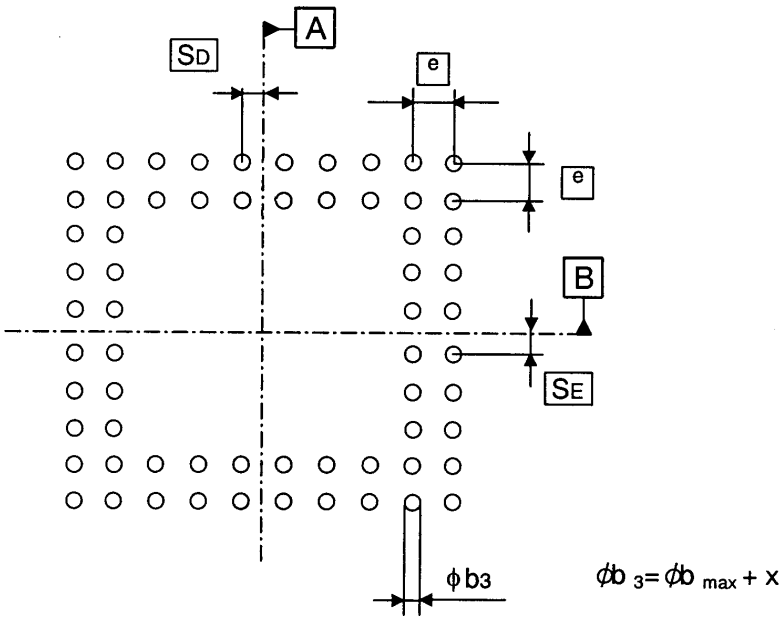
([9]) The center terminal position to the direction of the package width, length(S_E , S_D) are stipulated the position of the closest terminal with respect to the package center which the datum line A , B.

([10]) Indicates the diameter of the metal zed pad(ϕ R).

REMARKS: Range where pattern of terminal position areas exist

Range where pattern of terminal position areas exist is shown in **Figure 7** as reference for foot pattern design.

Figure 7



8. OUTER DIMENSION

Table 1 below shows the standard dimensions. Combinations of the standard dimensions shown below allow a number of package variations. If a package is newly designed, their dimensions shall be selected in the **9. Standard package List**.

8.1 GROUP 1

Table 1

Unit: mm

<table>
<tr><th>Description</th><th>Reference symbol</th><th>Standards</th><th>Recommended</th><th>Remarks</th></tr>
<tr><td>Nominal dimension</td><td>M</td><td>(1) It prescribes the number of the matrix (M) with nominal dimension.
(2) It makes the number of the matrix (M) equal to or more than 2 integers.
(3) Nominal dimension (M) is shown below.
<table>
<tr><th>e</th><th colspan="6">M</th></tr>
<tr><td rowspan="7">2.54</td><td>8</td><td>15</td><td>22</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>9</td><td>16</td><td>23</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>10</td><td>17</td><td>24</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>11</td><td>18</td><td>25</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>12</td><td>19</td><td>26</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>13</td><td>20</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>14</td><td>21</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><th>e</th><th colspan="6">M</th></tr>
<tr><td rowspan="8">1.27</td><td>-</td><td>15</td><td>22</td><td>29</td><td>36</td><td>43</td></tr>
<tr><td>-</td><td>16</td><td>23</td><td>30</td><td>37</td><td>44</td></tr>
<tr><td>-</td><td>17</td><td>24</td><td>31</td><td>38</td><td>45</td></tr>
<tr><td>-</td><td>18</td><td>25</td><td>32</td><td>39</td><td>46</td></tr>
<tr><td>-</td><td>19</td><td>26</td><td>33</td><td>40</td><td>-</td></tr>
<tr><td>-</td><td>20</td><td>27</td><td>34</td><td>41</td><td>-</td></tr>
<tr><td>-</td><td>21</td><td>28</td><td>35</td><td>42</td><td>-</td></tr>
</table>
</td><td>“M_E“ in number of matrix to direction of package width (E). “M_D“ in number of matrix to direction of package length (D). And it makes them same number ($M_E = M_D$).</td><td>(1) The number of the matrix (M) shows the number of the terminal lines, which lurks in one line.
(2) “M_E“ in number of matrix to direction of package width (E). “M_D“ in number of matrix to direction of package length (D).
(3) The number of matrix is calculated by the following formula.
$M_E = E / e + 1$
$M_D = D / e + 1$</td></tr>
<tr><td>Package width</td><td>E</td><td rowspan="2">(1) Refer to Table 2 Standard package List.
(2) It prescribes package width (E) and package length (D) by the following formula.
$E = e \times (M_E - 1) + 2Z_E$
$D = e \times (M_D - 1) + 2Z_D$</td><td rowspan="2">Tolerance is
Plastic PGA
It makes equal to or less than $\pm$0.25.

Ceramic PGA
It makes equal to or less than $\pm$0.50.</td><td rowspan="2"></td></tr>
<tr><td>Package length</td><td>D</td></tr>
</table>

Table1 (continued)

Unit: mm

<table>
<tr><th>Description</th><th>Reference symbol</th><th>Standards</th><th>Recommended</th><th>Remarks</th></tr>
<tr><td>Package Seated height</td><td>A</td><td>
<table>
<tr><th>A_{min}</th><th>A_{max}</th></tr>
<tr><td>2.45</td><td>6.10</td></tr>
</table>
(1) It contains the warp and the inclination of the package.
(2) It doesn't contain heat sink height, a chip condenser.
(3) It contains a lid (cap).
</td><td>
<table>
<tr><th>A_{nom}</th></tr>
<tr><td>4.25</td></tr>
</table>
</td><td>(1) Refer to IEC60191-2/A2.</td></tr>
<tr><td>Standoff height</td><td>A_1</td><td>
<table>
<tr><th>e</th><th>A_{1min}</th><th>A_{1nom}</th><th>A_{1max}</th><th></th></tr>
<tr><td rowspan="2">2.54</td><td>1.00</td><td>1.27</td><td>1.52</td><td>Cavity up</td></tr>
<tr><td>0.65</td><td>1.27</td><td>1.52</td><td>Cavity down</td></tr>
<tr><td>1.27</td><td>0.25</td><td>-</td><td>-</td><td></td></tr>
</table>
(1) Height to lid (cap) which is the nearest seated plane, it makes the standoff height of cavity down type.
</td><td>-</td><td>(1) The shape of standoff pin which is used in PGA (e=2.54) is a note ([6]) of 7. Reference characters and drawing.
(2) It makes A_{1min} of SPGA(e =1.27) the same rule with BGA.</td></tr>
<tr><td>Package height</td><td>A_2</td><td>
<table>
<tr><th>A_{2min}</th><th>A_{2nom}</th><th>A_{2max}</th></tr>
<tr><td>1.78</td><td>-</td><td>4.55</td></tr>
</table>
(1) It contains the warp and the inclination of the package.
(2) It doesn't contain heat sink height, a chip condenser.
(3) It contains a lid (cap).
</td><td>-</td><td>(1) According to IEC 60191-2/A2.</td></tr>
<tr><td rowspan="2">Terminal diameter</td><td>ϕb</td><td>(1) ϕb shows terminal diameter which contains solder dip, Au plating size of the terminal pin.
<table>
<tr><th>e</th><th>ϕb_{min}</th><th>ϕb_{nom}</th><th>ϕb_{max}</th><th></th></tr>
<tr><td rowspan="2">2.54</td><td>0.40</td><td>(0.46)</td><td>0.64</td><td>Solder dip</td></tr>
<tr><td>0.40</td><td>(0.46)</td><td>0.51</td><td>Au plating</td></tr>
<tr><td>1.27</td><td>0.15</td><td>(0.20)</td><td>0.25</td><td></td></tr>
</table>
</td><td>-</td><td rowspan="2">(1) In case of solder pip, The thickness standardizes at [ϕb_1 +0.18/-0.05].
(2) In case of Au plating, It makes $\phi b_{nom}=\phi b_{1nom}$ because the thickness is about several μm.
(3) In case of solder plating,
The thickness standardizes at [ϕb_1 +0.010/-0.005].</td></tr>
<tr><td>ϕb_1</td><td>(1) ϕb_1 shows the material diameter of the terminal pin.
<table>
<tr><th>e</th><th>ϕb_{1min}</th><th>ϕb_{1nom}</th><th>ϕb_{1max}</th></tr>
<tr><td>2.54</td><td>0.40</td><td>0.46</td><td>0.51</td></tr>
<tr><td>1.27</td><td>0.15</td><td>0.20</td><td>0.25</td></tr>
</table>
</td><td>-</td></tr>
</table>

Table1 (continued)

Unit: mm

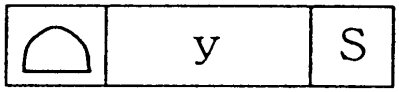
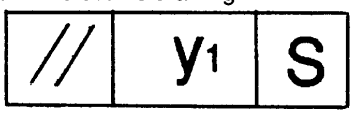
Description	Reference symbol	Standards	Recommended	Remarks
Terminal pitch	e	naming: PGA 2.54; SPGA 1.27	–	Means true geometrical position.
Terminal length	L	e: 2.54 — L min 2.54, L nom 3.30, L max 5.08; e: 1.27 — L min 1.20, L nom 2.00, L max 2.30	In case of e =2.54, it makes L_{max} following as same as SIP, ZIP, DIP. e: 2.54 — L max 3.90	Terminal length (L) is full length (height) from the seating plane.
Positional tolerance of terminal center	x	(1) Positional tolerance of terminal center shall be specified in the outline drawing.  (2) Reference symbol "x" shall be replaced as below. e: 2.54 — x 0.25; e: 1.27 — x 0.19	–	(1) M means the concept of the maximum material requirements and it shall be applied.
Terminal co planarity	y	(1) The co planarity shall be specified in the outline drawing.  (2) Reference symbol "y" shall be replaced as below. But, e= 2.54(PGA) is unnecessary to the rule. e: 2.54 — y -; e: 1.27 — y 0.10	–	(1) In case of PGA (e= 2.54), it is not in the rule, because pin insertion type. (1) In case of SPGA(e=1.27), It provides for surface mount type.
Parallelism of package top surface	y_1	(1) Parallelism of package top surface shall be specified in the outline drawing.  (2) Reference symbol "y_1" shall be replaced as below. y_1 =0.35		It makes the same rule with BGA(**EIAJ EDR-7315A**).

Table1 (continued)

Unit: mm

<table>
<tr><th>Description</th><th>Reference symbol</th><th>Standards</th><th>Recommended</th><th>Remarks</th></tr>
<tr><td>Center terminal position in package width direction</td><td>S_E</td><td>(1) M_E is an odd number, S_E = 0
(2) M_E is an even number, S_E = e /2
<table><tr><th></th><th>e</th><th>S_E</th></tr><tr><td>PGA</td><td>2.54</td><td>1.27</td></tr><tr><td>SPGA</td><td>1.27</td><td>0.635</td></tr></table></td><td>-</td><td>-</td></tr>
<tr><td>Center terminal position in package length direction</td><td>S_D</td><td>(1) M_D is an odd number, S_D = 0
(2) M_D is an even number, S_D = e /2
<table><tr><th></th><th>e</th><th>S_D</th></tr><tr><td>PGA</td><td>2.54</td><td>1.27</td></tr><tr><td>SPGA</td><td>1.27</td><td>0.635</td></tr></table></td><td>-</td><td>-</td></tr>
<tr><td>Terminal layout</td><td></td><td>(1) Terminal layout is fixed in the following condition.
“e” terminal pitch.
“M_E” number of matrix to direction of package width (E).
“M_D” number of matrix to direction of package length (D).
“S_E” center terminal position in package width direction.
“S_D” center terminal position in package length direction.
(2) It may delete a terminal optionally. But, it makes inside of allowable number of missing terminals (n_1).</td><td>-</td><td>Refer to 11.The reference of terminal layout figure. (IEC 60191-2/A2)</td></tr>
<tr><td>Number of existing maximum terminals</td><td>n_{max}</td><td>Number of existing maximum terminals is calculated by the following formula.
$n_{max} = M_E \times M_D$</td><td>-</td><td rowspan="3">(1) Refer to Table 2 Standard package List about number of maximum terminals about each number of matrix.
(2) The existing number of minimum terminals is calculated by the following formula.
$n_{min} = n_{max} - n_1$</td></tr>
<tr><td>Allowable number of missing terminals</td><td>n_1</td><td>Allowable number of missing terminals is calculated by the following formula.
$n_1 = (M_E - 2) \times (M_D - 2)$</td><td>-</td></tr>
<tr><td>Number of existing terminals</td><td>n</td><td>(1) All existing numbers of the terminals.
(2) It doesn't have the electric connection and insertion prevention pin and so on, too, is contained.</td><td>-</td></tr>
</table>

8.2 Group 2

Table1 (continued)

Unit: mm

<table>
<tr><th>Description</th><th>Reference symbol</th><th>Standards</th><th>Recommended</th><th>Remarks</th></tr>
<tr><td>Package overhang</td><td>Z_E
Z_D</td><td>(1) Package overhang is calculated by the following formula.
$Z_E = (E - (M_E - 1) \times e)/2$
$Z_D = (D - (M_D - 1) \times e)/2$
(2) Package overhang standards value.
<table>
<tr><th>e</th><th colspan="3">Z_E , Z_D</th></tr>
<tr><td>2.54</td><td>2.032</td><td>1.27</td><td>-</td></tr>
<tr><td>1.27</td><td>-</td><td>1.27</td><td>0.635</td></tr>
</table></td><td></td><td>(1) Refer to Table 2 Standard package List about package width and length, which is calculated by each overhang hang.
(2) Refer to Explanatory notes.</td></tr>
<tr><td>Metal zed pad diameter</td><td>ϕR</td><td>(1) It prescribes metal zed pad diameter as follows.
<table>
<tr><th>e</th><th>ϕR_{min}</th><th>ϕR_{nom}</th><th>ϕR_{max}</th><th></th></tr>
<tr><td>2.54</td><td>-</td><td>1.78</td><td>2.03</td><td>ceramic</td></tr>
<tr><td></td><td>-</td><td>1.78</td><td>2.03</td><td>plastic</td></tr>
<tr><td>1.27</td><td>-</td><td>-</td><td>1.05</td><td></td></tr>
</table>
(2) It prescribes a minimum distance among neighbor metal zed pad diameter as follows.
<table>
<tr><th>e</th><th></th></tr>
<tr><td>2.54</td><td>0.51</td></tr>
<tr><td>1.27</td><td>0.22</td></tr>
</table>
It calculates a minimum distance among neighbor metal zed pad diameter shown in the following.
$e - \phi R_{max}$</td><td>–</td><td>(1) There is not a minimum metal zed pad diameter (ϕR_{min}) in the rule.
(2) In case of e=1.27, Only maximum metal zed pad diameter (ϕR_{max}) is a rule.</td></tr>
<tr><td>Range where pattern of terminal diameter position areas exist</td><td>ϕb_3</td><td>(1) Range where pattern of terminal diameter position areas exist is calculated by the following formula.
$\phi b_3 = \phi b_{max} + x$</td><td>–</td><td></td></tr>
</table>

9. Standard package List

To further clarifies the combinations of part dimensions, the combinations of recommended package classifications shall be indicated as shown below as assistance in the design and development of new package in the future.

Table 2 Standard package List

PGA, e=2.54				E, D	
M	n_{max}	n_{min}	n_1	Z_E, Z_D	
				2.03	1.27
8	64	28	36	21.84	20.32
9	81	32	49	24.38	22.86
10	100	36	64	26.92	25.40
11	121	40	81	29.46	27.94
12	144	44	100	32.00	30.48
13	169	48	121	34.54	33.02
14	196	52	144	37.08	35.56
15	225	56	169	39.62	38.10
16	256	60	196	42.16	40.64
17	289	64	225	44.70	43.18
18	324	68	256	47.24	45.72
19	361	72	289	49.78	48.26
20	400	76	324	52.32	50.80
21	441	80	361	54.86	53.34
22	484	84	400	57.40	55.88
23	529	88	441	59.94	58.42
24	576	92	484	62.48	60.96
25	625	96	529	65.02	63.50
26	676	100	576	67.56	66.04

M: Number of the matrix
n_{max} : Number of existing maximum terminals
n_{min} : Number of existing minimum terminals
n_1 : Allowable number of missing terminals
E, D: Package width, length (mm)
Z_E, Z_D: Package overhang (mm)

SPGA, e=1.27				E, D	
M	n_{max}	n_{min}	n_1	Z_E, Z_D	
				1.27	0.635
15	225	56	169	20.32	19.05
16	256	60	196	21.59	20.32
17	289	64	225	22.86	21.59
18	324	68	256	24.13	22.86
19	361	72	289	25.40	24.13
20	400	76	324	26.67	25.40
21	441	80	361	27.94	26.67
22	484	84	400	29.21	27.94
23	529	88	441	30.48	29.21
24	576	92	484	31.75	30.48
25	625	96	529	33.02	31.75
26	676	100	576	34.29	33.02
27	729	104	625	35.56	34.29
28	784	108	676	36.83	35.56
29	841	112	729	38.10	36.83
30	900	116	784	39.37	38.10
31	961	120	841	40.64	39.37
32	1024	124	900	41.91	40.64
33	1089	128	961	43.18	41.91
34	1156	132	1024	44.45	43.18
35	1225	136	1089	45.72	44.45
36	1296	140	1156	46.99	45.72
37	1369	144	1225	48.26	46.99
38	1444	148	1296	49.53	48.26
39	1521	152	1369	50.80	49.53
40	1600	156	1444	52.07	50.80
41	1681	160	1521	53.34	52.07
42	1764	164	1600	54.61	53.34
43	1849	168	1681	55.88	54.61
44	1936	172	1764	57.15	55.88
45	2025	176	1849	58.42	57.15
46	2116	180	1936	59.69	58.42

10. Standard Registration

When you need to register a new outline specification on the standard, complete the appendix format 5 in Technical Standardization Committee on Semiconductor Device Package steering rule, in compliance with the Standardization Rule. In order to make a package dimension table, which come sunder Item 2, Appendix format 5, fill the dimensions marked with (レ) in the following Table.

Incidentally, it supposes that it enters package code form type according to **EIAJ ED-7303B** [Name and Code for Integrated Circuits Package].

Table 3

Serial Number				
External Type		C(P)-PGAOOO- SOOU(D)-2.54 C(P)-SPGAOOO- SOOU(D)-1.27		
Reference Symbol		min	nom	max
Group1	M		レ	
	E		レ	
	D		レ	
	A			レ
	A_1	レ	レ	レ
	A_2	レ	レ	レ
	ϕb	レ		レ
	ϕb_1	レ	レ	レ
	e		レ(*1)	
	L	レ	レ	レ
	x			レ
	y			レ(*2)
	y_1			レ
	n		レ	
Group2	Z_E		レ	
	Z_D		レ	
	ϕR			レ

(*1)Means true geometrical position, (*2) PGA (e=2.54) is not in the rule.

10.1 External Type

External type entering point

C: Ceramic
P: Plastic

S : Square→see note.
OO : Matrix→see note.

C(P)- (S)PGAOOO - SOO U(D) -2.54 ←Pitch

n : number of terminal

U : Cavity Up →see note.
D : Cavity Down →see note.

note. It may write at way package width (E) x package length (D).

11. The reference of terminal layout figure

As assistance in the design and development of new package in the future. The reference of terminal layout figure shown below.

The reference of terminal layout figure (1/3)

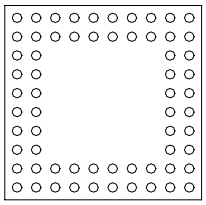


Fig.1

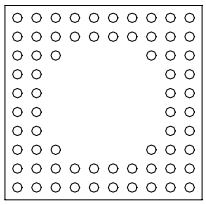


Fig.2

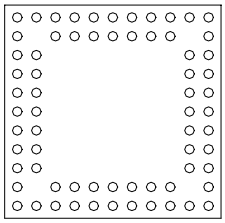


Fig.3

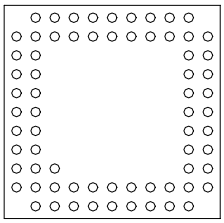


Fig.4

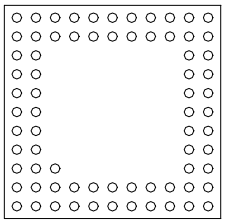


Fig.5

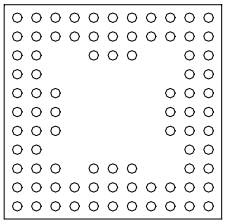


Fig.6

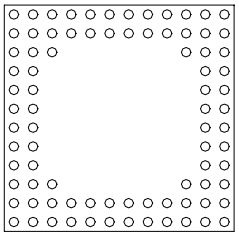


Fig.7

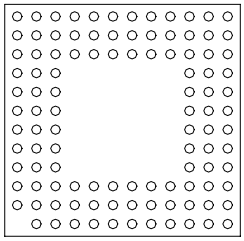


Fig.8

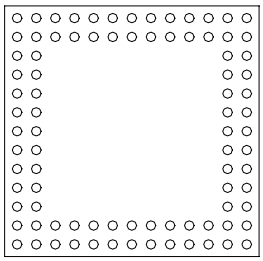


Fig.9

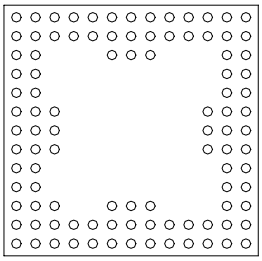


Fig.10

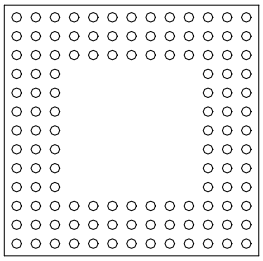


Fig.11

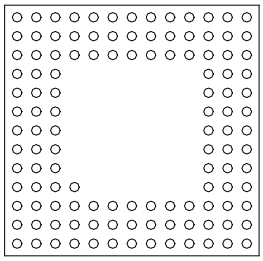


Fig.12

The reference of terminal layout figure (2/3)

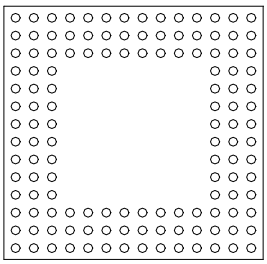


Fig.13

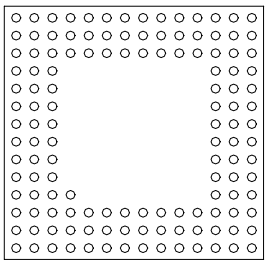


Fig.14

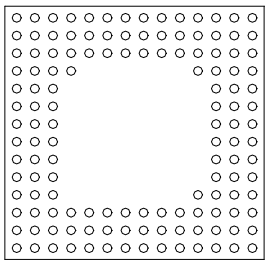


Fig.15

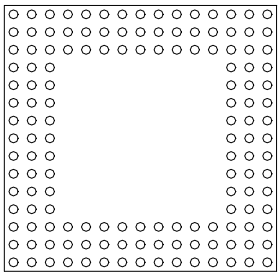


Fig.16

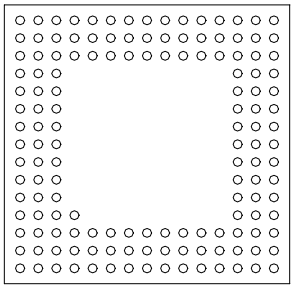


Fig.17

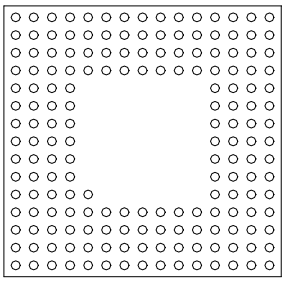


Fig.18

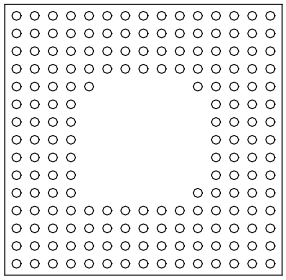


Fig.19

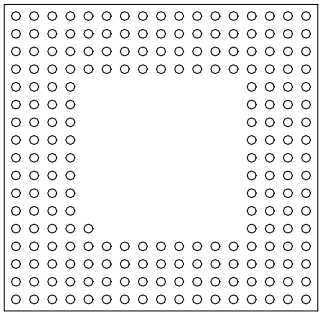


Fig.20

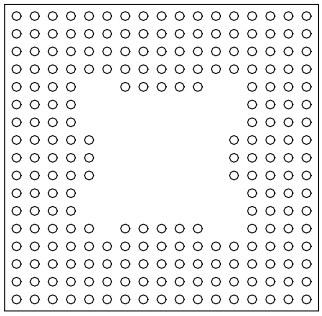


Fig.21

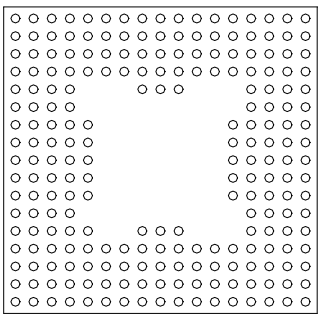


Fig.22

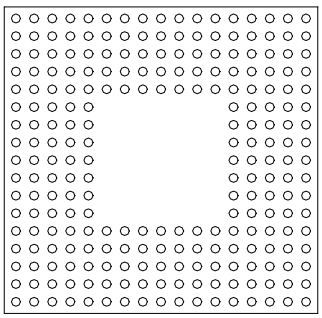


Fig.23

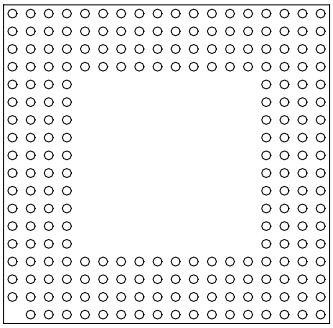


Fig.24

The reference of terminal layout figure (3/3)

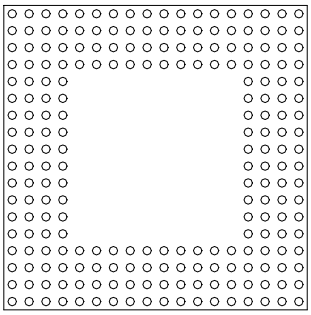


Fig.25

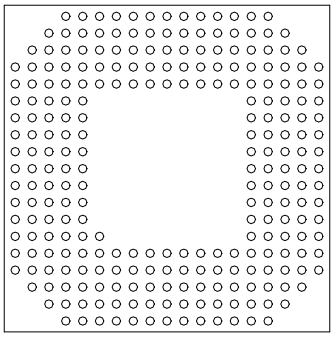


Fig.26

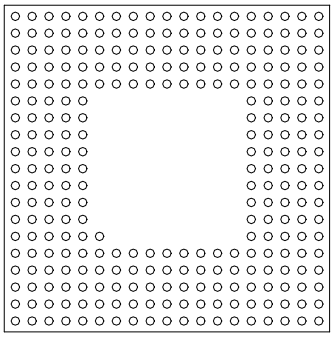


Fig.27

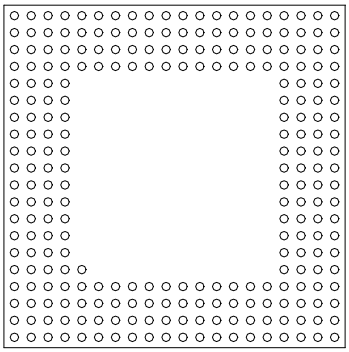


Fig.28

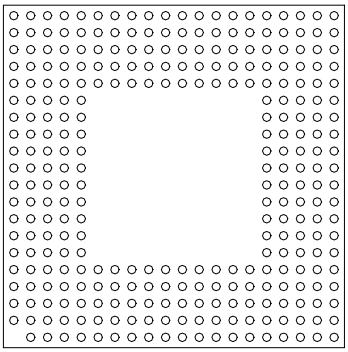


Fig.29

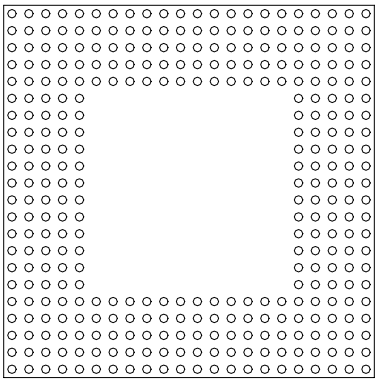


Fig.30

EXPLANATORY NOTES

1. Objective of establishment

This technical report accounts for the industrial standard of Pin Grid Array (hereinafter referred to as PGA) which is applied terminal pitch e = 2.54mm and Shrink pitch Pin Grid Array (hereinafter referred to as SPGA) which is applied 1.27mm. It was established to provide the design guideline of PGA when it is made in to product or when Automatic mounting machinery and associated parts are developed.

2. History of review

The 1980s, Corresponding to the smallness and thinner of the electronic equipment, The development and the production from the pin insertion package (SIP, ZIP, DIP) which makes the through hall of an implementing substrate pierce and insertion to the surface mount package (SOP, QFP) developed. In such, it corresponds to the multifunction of the electronic equipment; the demand to the numerous pin package is increasing rapidly. It answers the demand, at first, PGA appeared that of terminal pitch e = 2.54mm (100mil), and which the pin insertion type to into the printed circuit board through hall. And it is possible to make more numerous pins, SPGA appeared that of terminal pitch e = 1.27mm (50mil), and which the surface mount type of the printed circuit board in the same way Quad Flat I – lead package (QFI). Also, at first, the main constituent of the package body material, which excludes a terminal part, was a ceramic but at present, plastic, too, is adopted like the ceramic. Moreover, in recent years, the ball grid array, which arranges a ball terminal in the pin grid array format instead of the pin terminal, becomes used by the industry. Moreover, enters the latter half of 1990's Pin insertion type SPGA with a more bigger pin diameter (ϕ b_{nom} = 0.30mm), which is produced chiefly by CPU usage of PC in the United States. However, standardization was put off from there was no maker who was producing in Japan. As the PGA relation standard, the following standard exists and results in the present.

(1) EIAJ ED-7408 (General rules for the preparation of outline drawings of integrated circuits, Pin Grid Array Packages)

It was a deliberation in Technical Committee on Semiconductor Package Outlines (currently, Technical Standardization Committee on Semiconductor Device Package) and it was established in October 1988. It provided about PGA in terminal pitch e = 2.54mm (100mil).

(2) EIAJ ED-7408A (General rules for the preparation of outline drawings of integrated circuits, Pin Grid Array Packages)

It began a deliberation from March 1991 in the Ceramic Package Subcommittee (currently, Integrated Circuits Package Subcommittee), which was under Technical Committee on Semiconductor Package Outlines and it was established in February 1994. It was **EIAJ ED-7408** revision versions and the rule of package outline drawing, terminal diameter, and package overhang was revised. Not to be based on general rules for the preparation of outline drawings after doing package outline form investigation (July - December, 1991) for PGA to create individual registration (SC code) data was pointed out and was revised. After that, in 1998, the individual registration data of PGA was proposed from Japan to SC47D/WG1, which takes charge of the standardization of the semiconductor package outline form International Electro technical Commission (hereinafter referred to as IEC), and It plans to establish as **IEC 60191-2/A2** (PIN GRID ARRAY 2.54mm PITCH OUTLINE FAMILY (Intended for inclusion into **IEC 60191-2**), in 2002.

(3) EIAJ EDR-7323 (Design guideline of integrated circuits for Shrink pitch Pin Grid Array)

It began a deliberation from April 1991 in the Ceramic Package Subcommittee (currently, Integrated Circuits Package Subcommittee), which was under Technical Committee on Semiconductor Package Outlines and it was established in May 1999. It provided about SPGA in terminal pitch e = 1.27mm(50mil). The outline drawing investigation (- May, 1993) and the design guide draft of SPGA, and it introduced to JC-11 which takes charge of the standardization of the integrated circuit package outline form which places them in Joint Electron Device Engineering Council (hereinafter referred to as JEDEC), and it exchanged an opinion (1995, the JWG#2 conference). Moreover, to match an international standard, which it is possible to propose in the standardization to IEC, SC47D/WG1. According to the IEC format, we placed in the design guide as the classification.

(4) EIAJ EDR-7323A (Design guideline of integrated circuits for Shrink pitch Pin Grid Array))

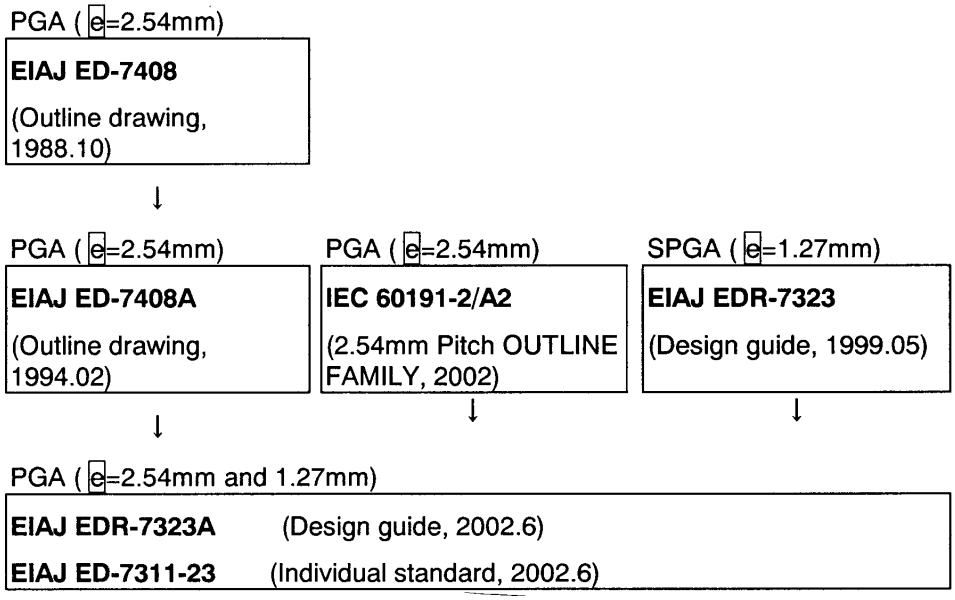
It began a deliberation from October 2001 in the Integrated Circuits Package Subcommittee, which was under Technical Committee on Semiconductor Package Outlines and it was established in June 2002. It is the revision version to have integrated two standards of PGA (**EIAJ ED-7408A**) and SPGA (**EIAJ EDR-7323**) into. In case of revision, the reference in the result which investigated the individual registration data of PGA, SPGA (October, 2001 - March, 2002), **IEC 60191-2/A2**, and It investigates line-up of PGA, SPGA to be supplying a semiconductor manufacturer with in the production from the material manufacturer. Also, according to IEC global drawing format (Revision of **IEC 60191-6** Global drawing format, establishment schedule in 2002 (hereinafter referred to as IEC global drawing format)), it adopted a datum from this technical report.

(5) EIAJ ED-7311-23 (Standard of integrated circuits package (PGA))

It began a deliberation from October 2001 in the Integrated Circuits Package Subcommittee, which was under Technical Committee on Semiconductor Package Outlines and it was established in June 2002. To match an international standard, which it is possible to propose in the standardization to IEC, SC47D/WG1. According to the IEC format, we placed in the individual standard as the classification.

The elapse of the deliberation of PGA relation standard is shown in **explanation table 1** with the flow chart.

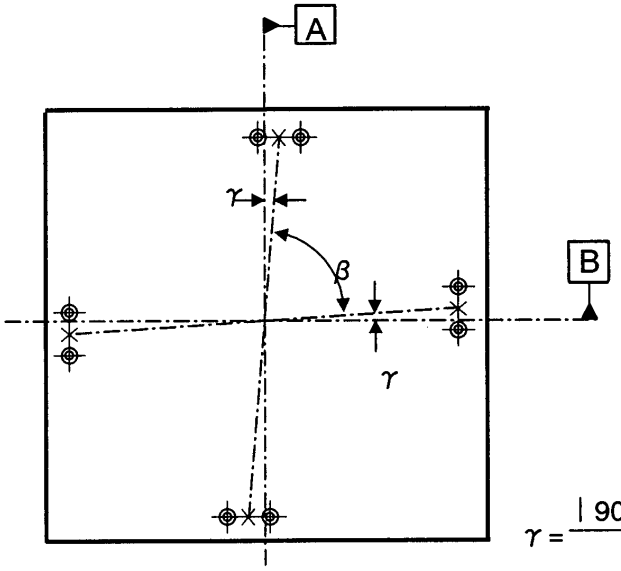
Explanation table 1



3. Basic idea

(1) Datum

This technical report is based on IEC global drawing format and adopts a datum, geometrical tolerance and the point of view. In case of adoption of the datum, it consulted BGA (**EIAJ EDR-7315A**), and the registration package of the PGA in JEDEC standard. At the JEDEC standard, the datum display is end of the package body, which the package outlines figure. However, currently, it maintains that the recognition way of the electronic device of the automatic mounting machinery, based on terminal. By IEC global drawing format, which carried forward establishment newly, it made the datum display of the package outline a package center. In the same way this technical report, with the JEDEC standard, too, being based on the IEC standard and to be adopted is wanted the same point of view and notation. It is shown below about the datum definition. It links respectively the center where each side is opposite and it finds the angle β to accomplish, intersecting. It looks for as it divides difference $|\ 90^\circ - \beta\ |$ between the β and 90° to each side equally axis. It defines the axis as being datum lines A , B.



(2) Dimensions display

As for PGA, the size, which becomes basics on the size decision is inch, because it was based on the JEDEC standard basically. Therefore, it is the soft metric series, which converted an inch to the millimeter. The display dimension in this technical report was based on the ISO standard and made "mm" display. In the way of converting from " inch " to the "mm", it quoted **IEC Publication 191-3** and it made the number of the effective digits 2 digits of the following of the decimal point.

Minimum values (min): The third decimal places to be reckoned as an unit.

Recommended values (nom): The third decimal places to be rounded off.

Maximum values (max): The third decimal places to be omitted.

Furthermore, in specifying each dimensional value, the concept set by the design centers was clearly shown by means of using the designed standard values (recommended nominal value) as guideline for standardization.

(3) The 1 pin display

The example of the concrete way of displaying about the 1 pin display for the automatic mounting machinery to recognize the direction of the package using the terminal, the way of adding one terminal to the corner part with the most internal circumference and the way of removing one terminal of A1 and so on were thought of. However, to prescribe the index display to have standardized on and for it to have been unified didn't result in an arrangement for the following reason. There are the package, which is depopulation terminals in 4 corners already, and the package that the space, which arranges a terminal in the corner part with the most internal circumference, isn't provided for. Also, the point that the user doesn’t unify a request to the 1 pin display, too, is the reason. However, actually, in the form according to this, a 1 pin display is implemented.

(4) Standard package List

To further clarifies the combinations of part dimensions, the combinations of recommended package classifications shall be indicated as shown **table 2 Standard package List** as assistance in the design and development of new package in the future.

4. Background for dimensional provisions

(1) Nominal dimension (M)

It is the notional one which becomes the standard which shows the size of the package outline, it is possible to show quantitatively, Nominal dimension is the number of the matrix (M). It is “M_E“ in number of matrix to the direction of the package width (E). And it is “M_D“ in number of matrix to the direction of the package length (D).

(2) Package width (E)

Package width is calculated in $E = e \times (M_E - 1) + 2Z_E$. But incidentally, $\pm$ 0.51 met about the tolerance as the supplement item in the previous standard. In this technical report, it made plastic PGA, equal to or less than $\pm$ 0.25, ceramic PGA, equal to or less than $\pm$ 0.50.

(3) Package length (D)

Package length is calculated in $D = e \times (M_D - 1) + 2Z_D$. But incidentally, $\pm$ 0.51 met about the tolerance as the supplement item in the previous standard. In this technical report, it made plastic PGA, equal to or less than $\pm$ 0.25, ceramic PGA, equal to or less than $\pm$ 0.50.

(4) Package Seated height (A)

PGA often attaches a heat sink but the height of the heat sink can not be provided because it depends on the consumption electric power of each device. Therefore, this design guide decides not to contain heat sink height in the package seated height (A). In the previous standard, as for the package seated height of PGA and SPGA, only A_{max}=6.10(240mil) was prescribed. Refer to **IEC 60191-2/A2**, in this technical report, it provided with A_{min}=2.45, A_{max}=6.10. Also, it made a recommendation value A_{nom} =4.25.

(5) Standoff height (A_1)

- In the before PGA standard that **EIAJ ED-7408A**, it provided as follows, that the cavity up and the cavity down were separate.
- Cavity up A_{1min}=1.106, A_{1max}=1.524, recommendation value A_{1nom}=1.270
- Cavity down A_{1min}=0.635, A_{1max}=1.524
- In the before SPGA standard that **EIAJ EDR-7323**, Only A_{1min}=0.25 was prescribed.
- Consulting **IEC 60191-2/A2**, it prescribed each of PGA, SPGA as follows. (Unit :mm)

	e	A_{1min}	A_{1nom}	A_{1max}	
PGA	2.54	1.00	1.27	1.52	Cavity up
		0.65	1.27	1.52	Cavity down
SPGA	1.27	0.25	-	-	

PGA that of terminal pitch e = 2.54mm (100mil), and which the pin insertion type to into the printed circuit board through hall. It secures a standoff with the standoff pin which becomes the stopper of the seating plane. SPGA that of terminal pitch e = 1.27mm(50mil), and which the surface mount type of the printed circuit board in the same way Quad Flat I – lead package (QFI). Therefore, it prescribes only a standoff minimum value (A_{1min}).

(6) Package height (A_2)

At the previous standard, Both PGA and SPGA were prescribed with A_{2min}=1.78(70mil), A_{2max}=4.58(180mil). According to **IEC 60191-2/A2**, in this technical report, it provided with A_{2min}=1.78, A_{2max}=4.55. Incidentally, it makes package body height, which contains a package body and a lid.

(7) Terminal pitch (e)

It prescribes 2 kinds, PGA, e =2.54, and SPGA, e =1.27.

(8) Terminal diameter(ϕb, ϕb_1)

ϕb shows the terminal diameter which contains the solder dip, the Au plating size of the terminal pin. ϕb_1 shows the material diameter of the terminal pin. The result of the PGA outline investigation, There were many ones which apply $\phi b = 0.46 \pm 0.10$(mm) and the terminal diameter resulted in missing from ϕb_{min}= 0.406(16mil). However, it implemented ability investigation just now, ϕb_{min}= ϕ0.406(ϕ16mil) was confirmed and it was provided that it was possible fill. And it made a recommendation value ϕb_{nom} =0.457(18mil). It was prescribed that in case of Au plating ϕb_{max} =0.508(20mil), and in case of solder dip ϕb_{max} =0.635(25mil). In **IEC 60191-2/A2**, it is prescribed with ϕb_{min} =0.40, ϕb_{max} =0.60. However, in this technical report, it prescribed with ϕb_{min} =0.40, ϕb_{nom} =(0.46), ϕb_{nom} =0.51(Au plating), 0.64(solder dip). Especially, the opinion that it isn't possible to guarantee at ϕb_{max} =0.60(solder dip), then it prescribed with ϕb_{max} =0.64(solder dip), a solder dip street 0.64, so far and it is the same. SPGA prescribed ϕb_{min} =0.15, ϕb_{nom} =(0.20), ϕb_{max} =0.25 which is the same as the past. From also this technical report, it learned and it added the material diameter ϕb_1 of the terminal pin to the other JEITA standard, and JEDEC standard. PGA prescribed ϕb_{1nom} =0.46, SPGA prescribed ϕb_{1nom} =0.20.

e	ϕb_{min}	ϕb_{nom}	ϕb_{max}	
2.54	0.40	(0.46)	0.64	Solder dip
	0.40	(0.46)	0.51	Au plating
1.27	0.15	(0.20)	0.25	

(9) Metal zed pad diameter (ϕR)

In the before PGA standard that **EIAJ ED-7408A**, it provided, dividing into the ceramic and plastic. Ceramic type prescribed ϕR_{max}=2.032(80mil), ϕR_{min}=1.524(60mil), plastic type prescribed ϕR_{max} =2.032(80mil) and there was not a rule with minimum metal zed pad diameter. Then, it made each recommendation value ϕR_{nom}=1.778(80mil).In the before SPGA standard that **EIAJ EDR-7323**, only ϕR_{max} =0.97 was prescribed. Adjust to the present production SPGA, at this technical report prescribed R_{max}=1.05 (SPGA). PGA and SPGA are not in the rule that ϕR_{min}. Also, it calculates a minimum distance among neighbor metal zed pad diameter in "e - ϕR_{max}".

(10) Positional tolerance of terminal center (x)

In case of e =2.54, x=0.25 (e / 10), and in case of e =1.27, x=0.19.

(11) Terminal co planarity (y)

SPGA that of terminal pitch e = 1.27(50mil), and which the surface mount type. Therefore, terminal co planarity (y) made important and becoming y=0.10. The other hand, PGA that of terminal pitch e = 2.54 (100mil), it is not in the rule, because pin insertion type.

(12) Parallelism of package top surface (y_1)

In case of PGA and SPGA, it often loads a radiation fin into the package top surface, parallelism of package top surface (y_1) was admitted to be necessary and it was deliberated. It confirmed to the PGA manufacturer maker, when the package material was a ceramic, the shrinkage of the ceramic occurred in the process of the manufacture and in the precision of the package curve and so on, there was an opinion to be necessary in containing y_{1max}=0.30. It prescribed y_{1max}=0.35 which is the same rule of BGA (**EIAJ EDR-7315A**).

(13) Number of existing terminals (n)

PGA number of the maximum terminals is $n_{max} = M_E \times M_D$. The number of the maximum terminals is the latently existing number of the terminals. Therefore, as for the fact, the terminal often comes off partially. Then the maximum terminals don't often agree with the actual number of the terminals. When described according to **EIAJ ED-7303B** [Name and Code for Integrated Circuits Package], The pin display which is in the deficit becomes as it is (example 64/100), however in case of PGA, it writes at the number of existing terminals(n). It calculates the allowable number of missing terminals $n_1=(M_E - 2) \times (M_D - 2)$.

(14) Center terminal position in package width(length) direction(S_E , S_D)

Likewise BGA (**EIAJ EDR-7315A**), It prescribes the position of the terminal which is arranged in the nearest position to the datum line of the package center A , B. When the number of matrix (M) is an odd number, $S_E = S_D = 0$, when even number, $S_E = S_D = e/2$.

(15) Package overhang (Z_E , Z_D)

In the before PGA standard that **EIAJ ED-7408A**, at first, it considered easiness in implementing and it was Z_{max} = 2.286(90mil). Also, Z_{min} considered position tolerance with metal zed pad diameter(ϕ R) and pad size and it made Z_{min} =1.016(40mil). However as a result of the outline figure investigation, this standard much didn't agree. For example, it is in case of Z_{nom} =1.270 or 2.032, when the size tolerance with package width (length) thinks that it does $\pm$ 1 %, in case of above E(D)=25.40, it comes off the rule. When the material of the package is a ceramic, it is difficult to do size tolerance within $\pm$ 1 %. As a result, it prescribed Z_{max} =2.540(100mil), Z_{min} =0.762(30mil) and it made a recommendation value Z_{nom} =1.270(50mil), 2.032(80mil). SPGA made the recommendation value Z_{nom} =0.635(40mil) and 1.270(50mil), which are the same as the past. It made a package over hang symbol Z_E and Z_D, which to the direction of the package width (E) and length (D), respectively. Z_E and Z_D are calculated by the following formula. Z_E = (E - (M_E -1) x e)/2, Z_D = (D - (M_D -1) x e)/2

(16) Terminal length (L)

In the before PGA standard that **EIAJ ED-7408A**, it was prescribed in L_{min}=2.540 (L_{nom}=3.302, L_{max}=5.080). In the before SPGA standard that **EIAJ EDR-7323**, it was prescribed in L_{min}=1.40 (L_{nom}=2.00, L_{max}=3.10). In reference of the JEDEC standard **MO-145A** and adjust to the present production SPGA, at this technical report prescribed L_{min}=1.20 (L_{nom}=2.00, L_{max}=2.30). Moreover, as the recommendation value, it added L_{max}=3.90 in case of e =2.54 like SIP, ZIP, DIP.

5. The reference standard

(1) IEC standard

Revision of IEC 60191-6 Global drawing format (establishment schedule in 2002)

IEC 60191-2/A2 (PIN GRID ARRAY 2.54mm PITCH OUTLINE FAMILY (Intended forinclusion into **IEC 60191-2**), establishment schedule in 2002)

(2) JEDEC standard

MS-017B (PGA, cavity down, e=2.54mm, establishment in June, 1993)

MO-066C (PGA, e=2.54mm, establishment in April, 1994)

MO-145A (SPGA, e=1.27mm, establishment in June, 1993)

MO-128C (IPGA, Staggered, e=2.54mm, establishment in January, 1997)

(3) JEITA standard

EIAJ ED-7303B (Name and Code for Integrated Circuits Package), establishment schedule in 2002.

EIAJ EDR-7315A (Design guideline of integrated circuits for Ball Grid Array(BGA)), establishment in November, 1998.

6. COMMITTEE MEMBERS

The IC Package Sub-committee of the Technical Standardization Committee on Semiconductor Device Package has mainly deliberated this standard.

The sub-committee members are shown below.

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