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Technical Report of Japan Electronics and Information Technology Industries Association

EIAJ EDR-7324A

Design guideline of integrated circuits for Plastic Quad Flat Non-leaded package (P-QFN)

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Prepared by

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Technical Report of Japan Electronics and Information Technology Industries Association

Design guideline of integrated circuits for Plastic Quad Flat Non-leaded package (P-QFN)

1. Scope of Application

This standard regulated outline drawings and dimensions of Plastic Quad Flat Non-Leaded Package (herein after referred to as P-QFN), especially plastic package, classified primary as form A and secondary as "terminal-N" under the **EIAJ ED-7300** (Recommended practice on standard for the preparation of outline drawings of semiconductor packages).

Note: This technical report is corresponds **EIAJ ED-7311-22** (Standard of integrated circuits package P-QFN). The other relation standards are shown below.

EIAJ EDR-7318A (Design guideline of integrated circuits for Plastic Small Outline Non-Leaded Package), established in November 1998, revised in April 2002.

EIAJ ED-7311-13A (Standard of integrated circuits package P-SON), established in January 1999, revised in June 2002.

2. Terminology

The definition of the terms used in this technical report complies with the **EIAJ ED-7300**. As for the new term, it is due to the definition in this technical report.

3. History

Recently, electronic appliances become smaller, conventional leaded type packages such as SOP and QFP become unsuitable, and demand for non-leaded type packages makes suppliers develop and commercialize such type of packages. This technical report is in intended to standardize the outer dimensions or "terminal-N" packages and ensure compatibility between products. For the integration of definitions about dimensions or packages, which have leads on both sides and around four sides, the packages were overviewed when the design guideline was made. **EIAJ EDR-7318** (Design guideline of integrated circuits for P-VSON) was established in December, 1998, which have leads on both sides, and **EIAJ EDR-7324** (Design guideline of integrated circuits for P-VQFN) was established in May 1999, which have leads around four sides.

EIAJ EDR-7318 and EIAJ EDR-7324 are considered a comment in every country in case of IEC standardization with a standard revision needed in spreading a variation rapidly by the development trend of each company, and added Seated height newly. Also, it considered an outline drawing by the saw cut which is a consistence with MO-229(Thermal Heat-sink V/WDFPN) and MO-220(Thermal Heat-sink V/WQFN) of JEDEC standard and a technology development trend in recent years, too, And it was created in the addition. As for both standards, it begins a deliberation from September 2001, EIAJ EDR-7318A and EIAJ EDR-7324A are established in April 2002.

This technical report shows the standard design values on the concept of the design centers as far as possible for standardization.

4. Definition of P- QFN

It is classified into N terminals of second category having the form of A. It's leads are flat and positioned at the bottom around four sides or the package to make it possible to mount on the printed circuit board (Metal exposing area is not defined in this report).

5. Numbering of Pins

In conformity with the definition of **EIAJ ED-7300**.

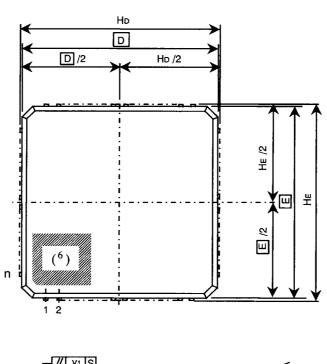
6. Nominal Dimensions

The package body size (package length: D, package width: E) is regarded as Nominal dimensions.

7. REFERENCE CHARACTERS AND DRAWING

7.1 Outline Drawing

Figure 1 (L₁=0.10)



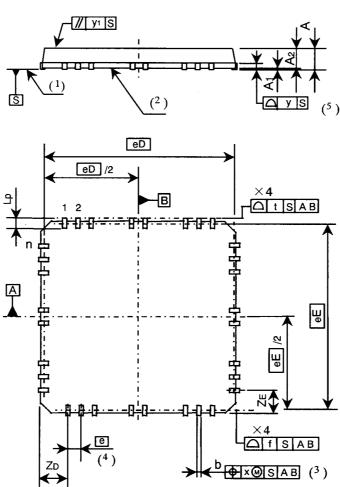
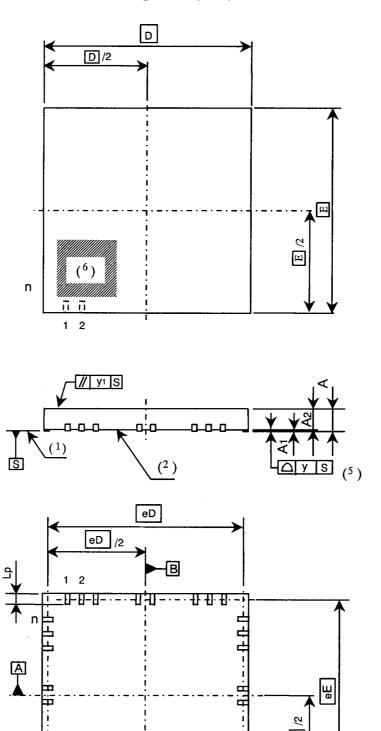


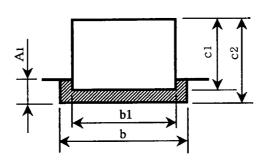
Figure 2 (L₁=0)



е

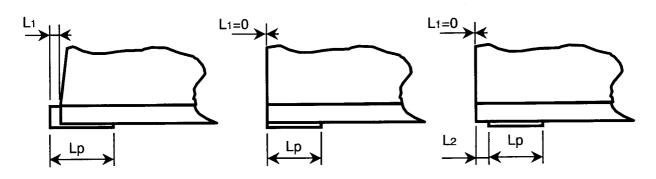
×4 ① f S A B

Figure 3



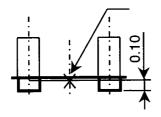
Terminal cross section (7)

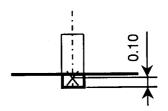
(1) Definition of the datum A_1



Terminal to be soldered

Center between lead centers.





- (a) For even number of leads on a package side (b) For odd number of leads on a package side
 - (3) The detailed figure (datum target)

Notes: (1) The mounting surface, with which a package is in contact.

- (2) The base surface, which is in parallel with the mounting surface and links the lowest point, except the stand off.
- (3) The maximum material requirements apply to the positional tolerance of the terminals. (For the maximum material requirements, refer to ISO 2692/JIS B 0023.)
- (4) Specifies the true geometric position of the terminal axis.
- (5) Specifies the vertical shift of the flat part of each terminal form the mounting surface.
- (6) Shows the allowable position of the Index mark area, which is based on the IEC standard and basically 1/16 with package body size, however in case of small package body size, it is less than 1/4 with package body size, It must be included in the shaded area entirely.
- (7) The dimensions of the terminal section apply to the terminal region ranges of 0.10mm and 0.25mm from the end of a terminal.

8. Outer Dimension

Table 1 below shows the standard dimensions. Combinations of the standard dimensions shown below allow a number of package variations. If a package is newly designed, their dimensions shall be selected in the Table or Standard Package Dimension List in the **Appendix 9**.

GROUP 1

Table 1

	5 (
Description	Reference	Standards	Recommended	Remarks
	symbol			
Nominal	ExD	package length (D) x package width(E)		
dimensions		is regarded as Nominal dimensions.	-	
Package	E	<u> </u>	(1) An integer value	(1) Line-up is
_		2.00 6.00 10.00	is recommended E	
width		2.50 6.50 11.00		made every
		3.00 7.00 12.00	x D.	0.50mm step
		3.50 7.50 13.00	(2) It recommends	for 2.00 -
		4.00 8.00 14.00	to be $E = D$.	10.00mm,
		4.50 8.50 15.00	(3) See 9. Standard	and 1.00mm
		5.00 9.00 16.00	package list.	step for 10.00
		5.50 9.50 17.00 - 18.00		- 20.00 mm.
		19.00		(2) Exclude
		20.00		resin burr.
Package	D			
length		2.00 6.00 10.00		
iongan		2.50 6.50 11.00		
		3.00 7.00 12.00		
		3.50 7.50 13.00		
		4.00 8.00 14.00		
		4.50 8.50 15.00		
		5.00 9.00 16.00 5.50 9.50 17.00		
		18.00		
		19.00		
		20.00		
 .		(1) = 1		
Tolerance	f	(1) Tolerance of package lateral profile shall		Exclude resin
of package		be specified in the outline drawing.		burr.
lateral		f SAB		
profile.		IJAB		
			-	
		(2) Reference symbol " f " shall be replaced		
		as below.		
		f = 0.20		

Table 1 (continued)

Description	Reference symbol	Standards	Recommended	Remarks
Seated height	А	Cord A min A max T >1.00 ≤1.20 V >0.80 ≤1.00 W >0.65 ≤0.80 U >0.50 ≤0.65 X ≤0.50	-	Include package warp age
Stand-off height	A ₁	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-	
Package height	A ₂	$A_2 = A - A_1$	-	
Terminal width	b b ₁	(1) b shows the terminal width with plating. e bmin bnom bmax 1.00 0.37 - 0.47 0.80 0.28 - 0.42 0.65 0.23 - 0.38 0.50 0.17 - 0.30 0.40 0.13 - 0.23 e b₁min b₁nom b₁max 1.00 0.37 0.40 0.43 0.80 0.28 0.35 0.38 0.65 0.23 0.30 0.33 0.50 0.17 0.20 0.23 0.40 0.13 0.16 0.19	Color Colo	(1) Terminal width follows IEC standard (60191-6-1). However, as for P-SON, terminal width was fixed based on the mounting reliability evaluation. (See EIAJ EDR-7318 A) (2) b, b ₁ apply to the ranges of 0.10 - 0.25 from the tip of a terminal. (3) Solder plating, the standard thickness of solder layer shall be [0.010+0.010 /-0.005]. As palladium plating, it is very thin, so terminal width and thickness is bnom=b ₁ nom.

Table 1 (continued)

Description	Reference symbol	Standards	Recommended	Remarks
Terminal pitch	e	e	-	
Tolerance of terminal center position	X	(1) Tolerance of terminal center position shall be specified in the outline drawing. X M S A B (2) Reference symbol " X " shall be replaced as below. X = 0.05	-	(1) The value is derived from the manufacturing ability of the suppliers.(2) The concept of the maximum material requirements shall be applied.
Co planarity	у	(1) Co planarity shall be specified in the outline drawing.	-	The value is derived from the manufacturing ability of the suppliers.
Parallelism of Package top surface	У1	(1) Parallelism of Package top surface shall be specified in the outline drawing. (2) Reference symbol " y ₁ " shall be replaced as below. y ₁ = 0.20	-	The value is derived from the manufacturing ability of the suppliers.

Table 1 (continued)

			1	Unit: mm
Description	Reference symbol	Standards	Recommended	Remarks
Positional tolerance of terminal tips	t	(1) Positional tolerance of terminal tips shall be specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing. The specified in the outline drawing.	-	
Length of soldered part	Lp	Lpnom shall be selected from 2 options (0.55,0.30) shown below. Lp nom	-	(1) Lpnom = 0.30 is specified for equal or less than ExD = 8.00x8.00mm.
Number of terminal position	n	See 9. Standard Package List.	(1) An integer value is recommended E x D. (2) It recommends to be $\boxed{\mathbb{E}} = \boxed{\mathbb{D}}$.	

GROUP 2

Table 1 (continued)

Unit: mm Reference Description Recommended Remarks Standards symbol In case of $L_1 = 0$, Overall H_{E} $H_E = E + 2L_1$ $H_E = E$ width In case of $L_1 = 0$, Overall H_D $H_D = D + 2L_1$ $H_D = \overline{D}$ length $Z_{E} = (E - (nE - 1)x e) / 2$ Exclude Package Z_{E} resin over hang burr. nE: The number of terminals along a widthwise side of a package. $Z_D = (E - (nD - 1)x e) / 2$ Z_{D} nD: The number of terminals along a lengthwise side of a package **Terminal** eЕ $\overline{eE} = \overline{E} - Lp - 2L_2$ inline interval еD $\overline{\text{eD}} = \overline{\text{D}} - \text{Lp} - 2\text{L}_2$ $L_1 min$ L_1 nom L₁max **Terminal** The L_1 value is 0.00 0.10 salient derived from the L₁max=0.20 length manufacturing ability of the То the suppliers. L_2 terminal $L_2 min$ L₂nom L_2 max from the 0.00 0.15 edge of the package

Table 1 (continued)

Description	Reference symbol	Standards	Recommended	Remarks
Terminal layout		Odd number of terminals for each package side. Even number of terminals for each package side.	-	(1) Odd number of terminals for each package side, package center coincides with the terminal center. (2) Even number of terminals for each package side, the terminal center is shifted by elepackage center.
Terminal thickness	C ₁		c₁nom 0.25 0.20 0.15 0.125 0.10	(1) c ₁ , c ₂ apply to the ranges of 0.10 - 0.25 from the tip of a terminal. (2) Solder plating, the standard thickness of solder layer shall be c ₁ +0.04/-0.00 (3) As palladium plating, it is very thin, so terminal width and thickness is c ₁ nom=c ₂ nom

9. Standard package List

To further clarify the combinations of part dimensions, the combinations of recommended package classifications shall be indicated as shown below as assistance in the design and development of new package in the future.

Table 2 Standard package List

Unit:mm(pin numbers in the table indicate)

	Lp nom									
			0.55					0.30		
ExD	1.00	0.80	0.65	0.50	0.40	1.00	0.80	0.65	0.50	0.40
2.00×2.00	-	(4)	8	12	12	(4)	8	8	12	12
2.50×2.50										
3.00×3.00	(4)	8	8	12	12	8	8	12	16	16
3.50×3.50										
4.00×4.00	8	12	12	20	24	12	12	16	24	24
4.50×4.50										
5.00×5.00	12	16	20	28	32	16	20	24	32	32
5.50×5.50										
6.00×6.00	16	20	28	36	44	20	24	28	40	44
6.50×6.50										
7.00×7.00	20	28	32	44	52	24	28	36	48	52
7.50×7.50										
8.00×8.00	24	32	40	52	64	28	32	40	56	64
8.50×8.50										
9.00×9.00	32	40	48	64	80					
9.50×9.50										
10.00×10.00	32	40	52	68	84					
11.00×11.00										
12.00×12.00	40	52	68	84	104					
13.00×13.00										
14.00×14.00	48	60	76	100	124					
15.00×15.00										
16.00×16.00	56	72	88	116	144					
17.00×17.00										
18.00×18.00	64	80	100	132	164					
19.00×19.00										
20.00×20.00	72	92	112	148	184					

- (1) An integer value is recommended ExD.
- (2) It recommends to be $\boxed{E} = \boxed{D}$.
- (3) See EIAJ ED-7311-22, about rectanguier type package which 3.00x4.00, 4.00x5.00, 5.00x6.00.

10 Standard Registration

When you need to register a new outline specification on the standard, complete the appendix format 5 in Technical Standardization Committee on Semiconductor Device Package steering rule, in compliance with the Standardization Rule. In order to make a package dimension table, which come under Item 2, Appendix format 5, fill the dimensions marked with (ν) in the following Table. Incidentally, it supposes that it enters package code form type according to **EIAJ ED-7303A** (Name and Code for Integrated Circuits Package).

Table 3

Table 3					
Serial I	Number				
External Type		P-OQFNO	00-0000×000	0-0.00	
	rence nbol	min	nom	max	
	E		V		
	D		V		
	A ₂	V	レ	V	
	f			V	
	Α			V	
	A ₁	V			
Group1	b	V		V	
Gro	b ₁	V	V	レ	
	e		レ(*)		
	Lp	V	レ	V	
	Х			V	
	у			V	
	t			V	
	n		レ		
	HD		レ		
	HE		レ		
	ZD		レ		
Group2	ZE		レ		
Gro	L ₁		レ		
	L ₂		レ		
	C ₁	V		V	
	C ₂	V		L	

^{*:} Means true geometrical position

EXPLANATORY NOTES

1. Objective of Establishment

This technical report accounts for the industrial standard of Plastic Quad Flat Non-Leaded Package (herein after referred to as P-QFN). It was established to provide the design guideline of P-QFN when it is made in to product or when Automatic mounting machinery and associated parts are developed.

2. Background

As systems get smaller, many companies started to develop non-leaded package that does not have protruding leads as SOP and QFP have by arranging leads at the bottom of the package. Non-leaded package needed to have an industrial standard as SOP or QFP. So, Technical Standardization Committee on Semiconductor Device Package organized a project of standardization or non-lead Package in November 1997 and standardization of P-VSON and P-VQFN went on till March 1998. Referring to the existing design guide of SOP and QFP for basic parts, standardization went on to Make tolerance or dimensions of P-VSON and P-VQFN are identical as possible even for the unique Part of non-lead package. EIAJ EDR-7318 (Design guideline of integrated circuits for P-VSON) was published in December, 1998 and EIAJ EDR-7324 (Design guideline of integrated circuits for P-VQFN) was published in April 1999. Referring to the existing design guide of SOP and QFP for basic parts, standardization went on to make tolerance or dimensions of P-VSON and P-VQFN are identical as possible even for the unique Part of non-lead package.

EIAJ EDR-7318 and EIAJ EDR-7324 are considered a comment in every country in case of IEC standardization with a standard revision needed in spreading a variation rapidly by the development trend of each company, and added Seated height newly. Also, it considered an outline drawing by the saw cut which is a consistence with MO-229 (Thermal Heat-sink V/WDFPN) and MO-220 (Thermal Heat-sink V/WQFN) of JEDEC standard and a technology development trend in recent years, too, And it was created in the addition. As for both standards, it begins a deliberation from September 2001, EIAJ EDR-7318A and EIAJ EDR-7324A are established in April 2002

Datum set up method, definition of tolerance of dimension, etc. are in conformity with EIAJ ED-7300.

3. Key points

(1) Nominal dimension (ExD)

Old **EIAJ EDR-7324** was defined only square body size, Line-up was made every 1.00mm step for ExD=3.00x3.00 - 8.00x8.00 mm according to the CSP concept, and every 2.00 mm step for larger dimensions according the QFP definitions.

This technical report EIAJ EDR-7324A is changed that Line-up is made every 0.50mm step for

E x D=2.00x2.00 - 10.00x10.00mm, and every 1.00mm step for E x D=10.00x10.00 - 20.00x20.00mm, however Line-up of E x D=2.00x2.00 - 10.00x10.00 mm is recommendation value an integer value especially. it consider **EIAJ EDR-7318A** (design guideline of P-SON) and corresponded a comment in every country in case of IEC standardization. Also, rectanguler package are registered in **EIAJ ED-7311-22**. (E x D = 3.00x4.00, 4.00x5.00, 5.00x6.00)

(2) Seated height (A)

Old **EIAJ EDR-7324** taking advantage of the characteristics of Non-leaded packages, it is defined to have 1.00mm maximum. This technical report **EIAJ EDR-7324A** is added Amax=1.20, 1.00, 0.80, 0.65, 0.50mm (code:T, V, W, U, X) which considered of IEC standard.

(3) Standoff height (A₁)

To indicate that the leads are not completely buried in the package, it is defined to be A_1 min=0.00mm. To indicate that the lead is not remarkably protruded from the resin body, it is defined to be A_1 max=0.05mm.

(4) Terminal width (b, b₁)

Tolerance is set to be an uniform value regardless of terminal pitch.

(5) Thickness of terminal (c_1, c_2)

Thickness is set to be an uniform value regardless of terminal pitch. As the part of a lead that is to be mounted is buried under resin, terminal thickness is defined as c_2 equals to "thickness of bare lead frame (c_1) +thickness of bottom plating". It is difficult to measure by non-destructive method so that dimensions of material are shown in Group2.

(6) Terminal pitch (e)

It is defined to have five hard metric dimensions, 1.00mm, 0.80mm, 0.65mm, 0.50mm, 0.40mm.

(7) Terminal interval pitch (eD, eE)

To become the reference of the design pattern of the terminal of print circuit board, it is rule in the terminal interval pitch (\boxed{eD} , \boxed{eE}) which $\boxed{eD} = \boxed{D} - Lpnom - 2L_2$, $\boxed{eE} = \boxed{E} - Lpnom - 2L_2$.

(8) Positional tolerance of terminal center (x)

Owing to the fact that it is non-leaded package, it is defined to have integrated tolerance value regardless of pitch.

(9) Terminal co planarity (y)

Owing to the fact that it is non-leaded package, it is defined to have integrated co planarity value regardless of pitch.

(10) Number of terminal (n)

It is defined to be 2 kinds of Length of the soldered part (Lpnom=0.55, 0.30), and it defined the maximum number of the terminals which the package body can be stored with. In case of Lpnom=0.30mm, It is applied E \times D = 8.00 \times 8.00mm or less. Because it is different that the desired mounting strength between package and print circuit board which depends on the package size.

(11) Length of the soldered part (Lp)

As mounting strength for package is different between package dimensions, it is defined to have 2 Lpnom length (Lp=0.55, 0.30) options. Lpnom=0.60, 0.25mm in old **EIAJ EDR-7324** (Design guideline of integrated circuits for P-VQFN)is changed to Lpnom=0.55,0.30mm in **EIAJ EDR-7324A** (Design guideline of integrated circuits for P-QFN). Restriction of number of pins, which can be, stored in package and it adjustment with the JEDEC standard MO-220 (Thermal Heat-sink V/WQFN) was considered.

(12) Terminal salient length (L₁)

 L_1 is defined to be protruding length of the terminal from the package body. L_1 min=0.00mm in addition to L_1 nom=0.10mm is newly added which adjustment with the JEDEC standard MO-220 (Thermal Heat-sink V/WQFN) were considered. And Recommended value L_1 max=0.20 is added.

(13) To the terminal from the edge of the package (L₂)

In case of the saw cut method, the terminal drags from the end of the package and sometimes designs, too. L_2 is defined to be length to the terminal which was dragged from the end of the package and L_2 min = 0.00mm, L_2 max = 0.15mm which adjustment with the JEDEC standard MO-220 (Thermal Heat-sink V/WQFN) were considered.

(14) Overall width (H_E), Overall Length(H_D)

Overall width and overall Length indicate means true geometrical position ($\overline{H_E}$, $\overline{H_D}$) in old **EIAJ EDR-7324. EIAJ EDR-7324A** not indicate means true geometrical position (H_E , H_D) it added $H_E = \overline{E}$, $H_D = \overline{D}$, In case of terminal length $L_1 = 0.00$ mm and it moved in Group2.

(15) Pattern of terminal areas

At old **EIAJ EDR-7324**, pattern of terminal areas can exist was shown Figure as reference for the foot print design. However, this technical report is deleted because complex of Length of protrusion of terminal (L_1) and to the terminal from the edge of the package (L_2) .

4. COMMITTEE MEMBERS

The IC Package Sub-committee of the Technical Standardization Committee on Semiconductor Device

Packages has mainly deliberated this standard.

The sub-committee members are shown below.

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