

Technical Report of Japan Electronics and Information Technology Industries Association

EIAJ EDR-7329

Design guideline of integrated circuits for Plastic Interstital Land Grid Array package (P-ILGA)

Established in March, 2002

Prepared by

Technical Standardization Committee on Semiconductor Device Package

Published by

Japan Electronics and Information Technology Industries Association

11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan Printed in Japan

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Design guideline of Integrated circuit for Plastic Interstitial Land Grid Array package (P-ILGA)

1. Scope of Application

This technical report regulated outline drawings and dimensions of Plastic Interstitial Land Grid Array (herein after referred to as P-ILGA), especially plastic package, classified primary as form D and secondary as "terminal-N" under the **EIAJ ED-7300** (Recommended practice on standard for the preparation of outline drawings of semiconductor packages).

Note: This technical report is created and corresponds to **EIAJ ED-7311-18** [Standard of integrated package (P-ILGA)] established in March, 2002.

2. Terminology

The definition of the terms used in this technical report complies with the EIAJ ED-7300.

3. History

Recently, electronic appliances become smaller, conventional leaded type packages such as SOP and QFP become unsuitable, and demand for no-lead type packages makes suppliers develop and commercialize such type of packages. This design guideline is in intended to standardize the outer dimensions or "terminal-N" packages and ensure compatibility between products. For the integration of definitions about dimensions or packages, which have leads on both sides and around four sides, the packages were overviewed when the design guideline was made. **EIAJ EDR-7318** [Design guideline of integrated circuits for Plastic Very Small Outline Non-Leaded Package(P-VSON)] was established in December, 1998, which have leads on both sides, and **EIAJ EDR-7324** [Design guideline of integrated circuits for Plastic Very thin Quad Flat Non-leaded package(P-VQFN)] was established in April, 1999, which have leads around four sides.

This technical report places witch the derivation package of **P-QFN**. And this package has terminals, which newly, zigzag (staggered) terminal type witch P-ILGA. It began a discussion from March, 2001, and establishment schedule in January, 2002. This standard shows the standard design values on the concept of the design centers as far as possible for standardization.

4. Definition of P-ILGA

It is classified into N terminals of second category having the form of D. It's leads are flat and positioned at the bottom around four sides or the package to make it possible to mount on the printed circuit board (Metal exposing area is not defined in this report). Incidentally, "I" is the initial of Interstitial, Interstitial terminal of the package means a package except the terminal which stood in line in series.

5. Numbering of Pins

In conformity with the definition of EIAJ ED-7300.

6. Nominal Dimensions

The package body size (package length: D, package width: E) is regarded as Nominal dimensions.

7. REFERENCE CHARACTERS AND DRAWING

7.1 Outline Drawing

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Figure 1 (L<sub>1</sub>=0.10)
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Figure 2 (L₁=0)







Terminal section (⁷) Definition of the datum A₁





Terminal to be soldered

Terminal to be soldered



(a) For even number of leads on a package side.





The detailed figure(datum target)

Notes:

- (¹) The mounting surface, with which a package is in contact.
- (²) The base surface, which is in parallel with the mounting surface and links the lowest point, except the stand-off.
- (³) The maximum mounting conditions apply to the positional tolerance of the terminals. (Refer to ISO 2692/JIS B 0023.)
- (⁴) Specifies the true geometric position of the terminal axis.
- (⁵) Specifies the vertical shift of the flat part of each terminal form the mounting surface.
- (⁶) Shows the allowable position of the Index mark area, which is based on the IEC standard, basically 1/16 with package body size, however in case of small bodysize, it is less than 1/4 with package bodysize, it must be included in the shaded area entirely.
- (⁷) The dimensions of the terminal section apply to the terminal region ranges of 0.10mm and 0.25mm from the end of a terminal.

8. Outer Dimension

Table 1 below shows the standard dimensions. Combinations of the standard dimensions shown below allow a number of package variations. If a package is newly designed, their dimensions shall be selected in the Table or Standard Package Dimension List in the Appendix.

8.1 GROUP 1

Table 1

Unit: mm Reference Recomm Description Standards Remarks symbol -ended Nominal ExD dimensions 3 x 3 Line-up is made every I mm step 4 x 4 5 x 5 for 3-8mm, 6 x 6 and 2 mm step for 8-20 mm. 7 x 7 8 x 8 10 x 10 12 x 12 14 x 14 16 x 16 18 x 18 20 x 20 Package Each dimension is identical with the nominal Exclude resin Е width dimensions. burr. Package D length Tolerance (1) The tolerance of terminal center shall be specified in the outline drawing. or package lateral profile. S AΒ f f (2) Reference symbol shall be replaced as below. f 0.20 Include package max Warp age Т 1.20 А V 1.00 Sealed А height W 0.80 U 0.65 Х 0.50

Table1 (continued)

Unit: mm

Description	Reference symbol	Standards				Recomm -ended	Remarks
Stand-off Height	A ₁	A1	min 0	nom 0.02	max 0.05	-	
Package height	A ₂		$A_2 = A - A_1$				Exclude package warp age
Terminal width	b	e	bmin	bnom	bmax		The thickness of a terminal plating is
		1.00	0.17		0.27		to be min 0,
		0.80	0.17		0.27		max 0.04.
		0.65	0.13		0.23		
		0.50	0.13		0.23		
		0.40	0.13		0.23		
Terminal width	b ₁	e	b1min	b1nom	b1max		Tolerance is set to be an uniform
		1.00	0.17	0.20	0.23		value.
		0.80	0.17	0.20	0.23	-	
		0.65	0.13	0.16	0.19		
		0.50	0.13	0.16	0.19		
		0.40	0.13	0.16	0.19		
Terminal pitch	e	1.00 0.80 0.65 0.50 0.40					<u>e/2</u> = 0.5xe
	e/2	0.50 0.40 0.325 0.25 0.20					
Terminal interval pitch	<u>e</u> 1	e 1.00 0.80 0.65	e1 0.87 0.69 0.56	e ₁] = (√3	/ 2) x [e]	_	
		0.50 0.40	0.50 0.40	e ₁] = [e]			

Table1 (continued)

				Unit: mm
Description	Reference symbol	Standards	Recomm -ended	Remarks
Tolerance of terminal center position	x	 (1) The tolerance of the terminal center shall be specified in the outline drawing. 	_	
		1.00 0.80 0.65 0.50 0.40		
Coplanarity	У	 (1) The co planarity shall be specified in the outline drawing. y S (2) The symbol y shall be replaced with any of the values shown below. e y 1.00 0.80 0.65 0.05 0.50 0.40 	_	
Prallelism of package top surface	У1	 (1) The prallelism of package top surface shall be specified in the outline drawing. y₁ S (2) The symbol y₁ shall be replaced with any of the values shown below. y₁ = 0.20 	_	
Positional tolerance of terminal tips	t	 (1) The tolerance of the terminal tips shall be specified in the outline drawing. t S A B (2) The character t shall be replaced with any of the values shown below. t = 0.20 	_	

Table1 (continued)

Unit: mm

Description	Reference symbol		Standards				Recomm -ended	Remarks
Number of terminal	n	Standard shown b	d number o elow.		For each length of soldered part (Lp), maximum			
position		(1) Lpno	m=0.55					available number of
			FxD		е			are specified about
				1.00	0.80	0.65		Lp _{nom} =0.30 and
		-	7 x 7	44	52	60		Lp _{nom} =0.55.
			8 x 8	52	60	76		1.Lpnom=0.55 In case of maximum
			10 x 10	60	76	100		
			12 x 12	76	100	124		available
			14 x 14	92	116	148		terminal position
			16 x 16	108	140	172		each body size, Lp=0.55 is
			18 x 18	124	156	196	_	ExD=7x7-
			20 x 20	140	180	220		20x20mm e=1.00 - 0.65
		(2) Lpno	m=0.30			_		2.Lpnom=0.30 In case of maximum available number of
				е				terminal position
			EXD	0.50	0.40			Lp=0.30 is
		-	3 x 3	28	28	-		ExD=3x3 - 8x8
			4 x 4	44	52			
			5 x 5	60	68			
			6 x 6	76	92			
			7 x 7	92	108			
		.	8 x 8	108	132			

Table1 (continued)

					Unit: mm
Description	Reference symbol		Standards	Recomm- ended	Remarks
Terminal			Terminal layout		
layout		Odd number of terminals for each package side.	The package centercoincides with the terminal center.		
		Even number of terminals for each package side.	The terminal Center is shifted by e /2 from the package center.		
The distance from the package center to the inner terminal center	eD /2 eE /2	eD /2 = (D +2 eE /2 = (E +2	L1) /2 – Lpnom/2 – <u>e</u> 1 _1) /2 – Lpnom/2 – <u>e</u> 1		The numerical value in the table which the distance from the package center to the inner terminal center , and $\boxed{\text{eD}}$ /2 = $\boxed{\text{eE}}$ / 2

Table1 (continued)

						Unit: mm
Description	Reference symbol		Standards	Recomm- ended	Remarks	
Length of soldered part	Lp	Lpnom shall be below.	pnom shall be selected from two options shown below.			1.Lp=0.55 is specified for package body
			Lp			size of E x D
		EXD	1	2		equal or above than 7
		3 x 3				x 7mm.
		4 x 4				
		5 x 5		Lpnom=0.30		2.Lp=0.30 is specified for package body size of E x D equal or less
		6 x 6	6 Lpmin=0.15			
		7 x 7				
		8 x 8				
		10 x 10	nnom			
		12 x 12	=0.55			
		14 x 14	_pmax=0.75			
		16 x 16	_pmm=0.35			
		18 x 18				
		20 x 20				
Terminal length	L ₁	min 0	n nom max 0.10		_	L ₁ is stored in Group 2.

8.2 Group2

Unit: mm Recomm Reference Description Standards Remarks symbol -ended $L_1=0$ $H_E = E$ Overall $H_E = E + 2L_1$ H_{E} width L₁=0 $H_D = D$ Overall $H_D = D + 2L_1$ H_{D} Length Package Exclude resin $Z_{D} = (D - (nD - 1) x e) / 2$ over hang burr. ZD nD : The number of terminals along a Lengthwise side of a package. $Z_{E} = ([E] - (nE - 1)x[e])/2$ Z_E nE : The number of terminals along a widthwise side of a package Derived from Terminal C_1 the lead frame thickness thickness range е c₁ min $c_1 nom$ c1 max that has 1.00 nominal 0.09 0.21 thickness of 0.80 0.09 0.21 0.10-0.20, it's 0.65 0.09 0.21 tolerance defined to be 0.50 0.09 0.21 0.09-0.21. 0.40 0.09 0.21 The thickness **C**₂ of a terminal plating is е $c_2 \min$ c₂ nom $c_2 max$ uniformly defined to be 1.00 0.09 0.25 $\min 0$, 0.80 0.09 0.25 max 0.04. 0.25 0.65 0.09 0.50 0.09 0.25 0.25 0.40 0.09

Table 1 (continued)

9. Standard package List

To further clarify the combinations of part dimensions, the combinations of recommended package Classifications shall be indicated as shown below as assistance in the design and development of new Package in the future.

										Unit: mm
		Terminal Pitch e								
ExD		1.00		0.80		0.65		0.50	0.40	
3 x 3		-		_		_	28	- 0.30	28	- 0.30
4 x 4		-	_				44	- 0.30	52	- 0.30
5 x 5		-		_		-		- 0.30	68	- 0.30
6 x 6		-		_		-	76	- 0.30	92	- 0.30
7 x 7	44	- 0.55	52	- 0.55	60	- 0.55	92	- 0.30	108	- 0.30
8 x 8	52	- 0.55	60	- 0.55	76	- 0.55	108	- 0.30	132	- 0.30
10 x 10	60	- 0.55	76	- 0.55	100	- 0.55		-		-
12 x 12	76	- 0.55	100	- 0.55	124	- 0.55		-		-
14 x 14	92	- 0.55	116	- 0.55	148	- 0.55		-		-
16 x 16	108	- 0.55	140	- 0.55	172	- 0.55		-		-
18 x 18	124	- 0.55	156	- 0.55	196	- 0.55		_		-
20 x 20	140	- 0.55	180	- 0.55	220	- 0.55		_		_

Note The numbers in the table indicate

(terminal number (n)) – (length of soldered part (Lp))

10. Standard Registration

When you need to register a new outline specification on the standard, complete the appendix format 5 in Technical Standardization Committee on Semiconductor Device Package steering rule, in compliance with the Standardization Rule.

In order to make a package dimension table, which come under Item 2, Appendix format, fill the dimensions marked with (🗸) in the following **Table 3**.

It supposes that it enters Extenal Type according to EIAJ ED-7303A (Name and Code for Integrated Package).

Serial	Number			
Exter	nal Type	P-ILGA XX	$X - XX.XX \times X$	X.XX – X.XX
Referen	ce Symbol	min	nom	max
	D		V	
	E		v	
	A ₂	✓	v	v
	f			v
	A			v
	A ₁	v		
	b	~		v
	b ₁	v	1	1
up 1	е		√ (*)	
Gro	e/2		v	
	e ₁		v	
	eD		_	
	еE		v	
	Lp	v	v	v
	x			1
	у			v
	t			v
	n		v	
	H₀		v	
	H _E			
Group 2	L ₁		v	
	ZD	~		v
	Z _E	1		V
	C ₁	v		v
	Ca	v		V

Table 3

EXPLANATORY NOTES

1. Objective of Establishment

This technical report accounts for the industrial standard of Plastic Interstitial Land Grid Array (herein after referred to as P-ILGA). It was established to provide the design guideline of P- ILGA when it is made in to product or when Automatic mounting machinery and associated parts are developed.

2. Background

As systems get smaller, many companies started to develop non-leaded package that does not have protruding leads as SOP and QFP have by arranging leads at the bottom of the package. Non-leaded package needed to have an industrial standard as SOP or QFP. So, Technical Standardization Committee on Semiconductor Device Package organized a project of standardization or non lead Package in November 1997 and standardization of P-VSON and P-VQFN went on till March 1998. Referring to the existing design guide of SOP and QFP for basic parts, standardization went on to Make tolerance or dimensions of P-VSON and P-VQFN are identical as possible even for the unique Part of no lead package. **EIAJ EDR-7318** [Design guideline of integrated circuits for Plastic Very Small Outline Non-Leaded Package(P-VSON)]was published in December, 1998 and **EIAJ EDR-7324**[Design guideline of integrated circuits for Plastic Very thin Quad Flat Non-leaded package(P-VQFN)]was published in April,1999. Referring to the existing design guide of SOP and QFP for basic parts, standardization went on to make tolerance or dimensions of P-VSON and P-VQFN are identical as possible even for basic parts, standardization for Plastic Very thin Quad Flat Non-leaded package(P-VQFN)]was published in April,1999. Referring to the existing design guide of SOP and QFP for basic parts, standardization went on to make tolerance or dimensions of P-VSON and P-VQFN are identical as possible even for the unique Part of non lead package.

Datum set up method, definition of tolerance of dimension, etc. are in conformity with EIAJ ED-7300.

This technical report places with the derivation package of P-QFN. And this package has terminals, which newly, zigzag (staggered) terminal type witch P-ILGA. It was proposed in September 2000, it began a discussion in working group of IC Plastic Package Sub-Committee, witch lower part of Semiconductor Package Standardization Committee. It was started from January 2001. And established in March 2002. This package naming, seated height and new reference symbol were discussed and then defined in Sub-Committee of general rule of semiconductor package. It was considered of during the IEC standardization progress which seated height, **EIAJ EDR-7318**, **EIAJ EDR-7324**. And it also considered of JEDEC standard **MO-220** (Thermal Heat sink V/WQFN), **MO-208** (Double row QFN).

3. Key points

- (1) Package name This package naming was defined which P-ILGA (Plastic Interstitial Land Grid Array Package), and it was discussed and then defined in Sub-Committee of general rule of semiconductor package. Incidentally, there is a case of the change in tentative name in the future.
- (2) Nominal dimension (ExD) Only square body size is defined for P-VQFN, Line-up is made every 1.00mm step for 3X3 8X8 mm according to the CSP concept, and every 2.00 mm step for larger

dimensions according the QFP definitions.

- (3) Seated height (A) EIAJ EDR-7324 taking advantage of the characteristics of Non-leaded packages, it is defined to have 1.00mm maximum. This technical report is added Amax = 1.20, 1.00, 0.80, 0.65, 0.50mm (code:T, V, W, U, X) which considered of IEC standard.
- (4) Stand-off height (A₁) To indicate that the leads are not completely buried in the package, it is defined to be 0.0 minimum. To indicate that the sides m² the lead is not remarkably protruded from the resin body, it is defined to be 0.05 mm maximum
- (5) Terminal width (b,b₁) Tolerance is set to be an uniform value regardless of terminal pitch.
- (6) Thickness of terminal (c_1,c_2) Thickness is set to be an uniform value regardless of terminal pitch. As the part of a lead that is to be mounted is buried under resin, terminal thickness is defined as c_2 equals to "thickness of bare lead frame (c_1) +thickness of bottom plating ".

It is difficult to measure by non-destructive method so that dimensions of material is shown in Group2.

- (7) Terminal pitch (e) It is defined to have five hard metric dimensions, 1.00mm, 0.80mm, 0.65mm, 0.50mm, 0.40mm.
- (8) Terminal interval pitch(e_1) The position relation between the most peripheral terminal and the 2nd line of terminals is always an equilateral triangle, the straight line distance, in case ofm $e_1=1.00\sim0.65$ mm, $e_1=(\sqrt{3}/2)xe$. And in case of $e_2=0.50\sim0.40$ mm, $e_1=e$, because to avoid approaching by the most peripheral terminal and the 2nd line of terminals.

In the working group discussed about three rows of, four rows stagger arrangements, too. However, The one of each company, There is not a production and development schedule about equal to or more than three rows package. The standardization got to let, this time.

- (9) Positional tolerance of terminal center (x) Owing to the fact that it is non-leaded package, it is defined to have integrated tolerance value regardless of pitch.
- (10) Terminal co planarity (y) Owing to the fact that it is non-1eaded package, it is defined to have integrated co planarity value regardless of pitch.
- (11) Number of terminal (n) It is defined to be a maximum number defined from terminal length(L). In case of Lp = 0.55, it was E x D =6 x 6mm or less body size did not standardize. Because it was noting the number of pins merit that about P-ILGA compared with P-VQFN. In case of Lp = 0.30, it standardize only by e = 0.50 0.40mm, it dose not standardize in e = 1.00 0.65mm for similar reasons.
- (12) Length of the soldered part (Lp) As desired mounting strength for package is different between package dimensions, it is defined to have two (Lpnom = 0.55, 0.30) Lp length options.

Lpnom = 0.60 in P-VQFN is changed to Lpnom = 0.55 in P-ILGA and, Lpnom = 0.25 in P-VQFN is changed to Lpnom = 0.30 in P-ILGA. Restriction of number of pins which can be stored in package and it adjustment with the JEDEC standard were considered.

(13) Length of the protrusion of terminal (L₁) L₁ is defined to be protruding length of the terminal from the package body.

 L_1 min = 0 in addition to L_1 nom = 0.10 is newly added which adjustment with the JEDEC standard were considered.

- (14) Overall width (H_E), Overall Length(H_D) It added H_E = \vec{E} , H_D = \vec{D} , In case of terminal length L₁=0, and it moved to group 2 (reference value).
- (15) The distance from the package center to the inner terminal center (eD /2, eE /2) It defined the distance from the package center to the inner terminal center(eD /2, eE /2). Because the design pattern of the print circuit board to make it be possible to compatibility, if length of the soldered part (Lp) changes.

(16) Prallelism of package top surfacecenter (y₁)

It added prallelism of package top surface (y1) from this technical report.

4. Members of discussion

Project Group and IC Package Sub-Committee of Semiconductor Package Standardization Committee have discussed this technical report. The members are as shown below.

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