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EIAJ EDR-7602

Design guideline of tray for integrated circuits

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Design guideline of tray for integrated circuits

1. Scope

This technical report specifies the shapes and dimensions of trays used in shipment and production of integrated circuits (hereafter denoted as trays).

2. Definition of Terms

Definition of main terms used in this report shall conform to **EIAJ ED-7300** [Recommended Practice on Standard for Preparation of Outline Drawing of Semiconductor Packages] and EIAJ other terms, not covered by these standards, shall be as defined in this report.

3. Packages Concerned

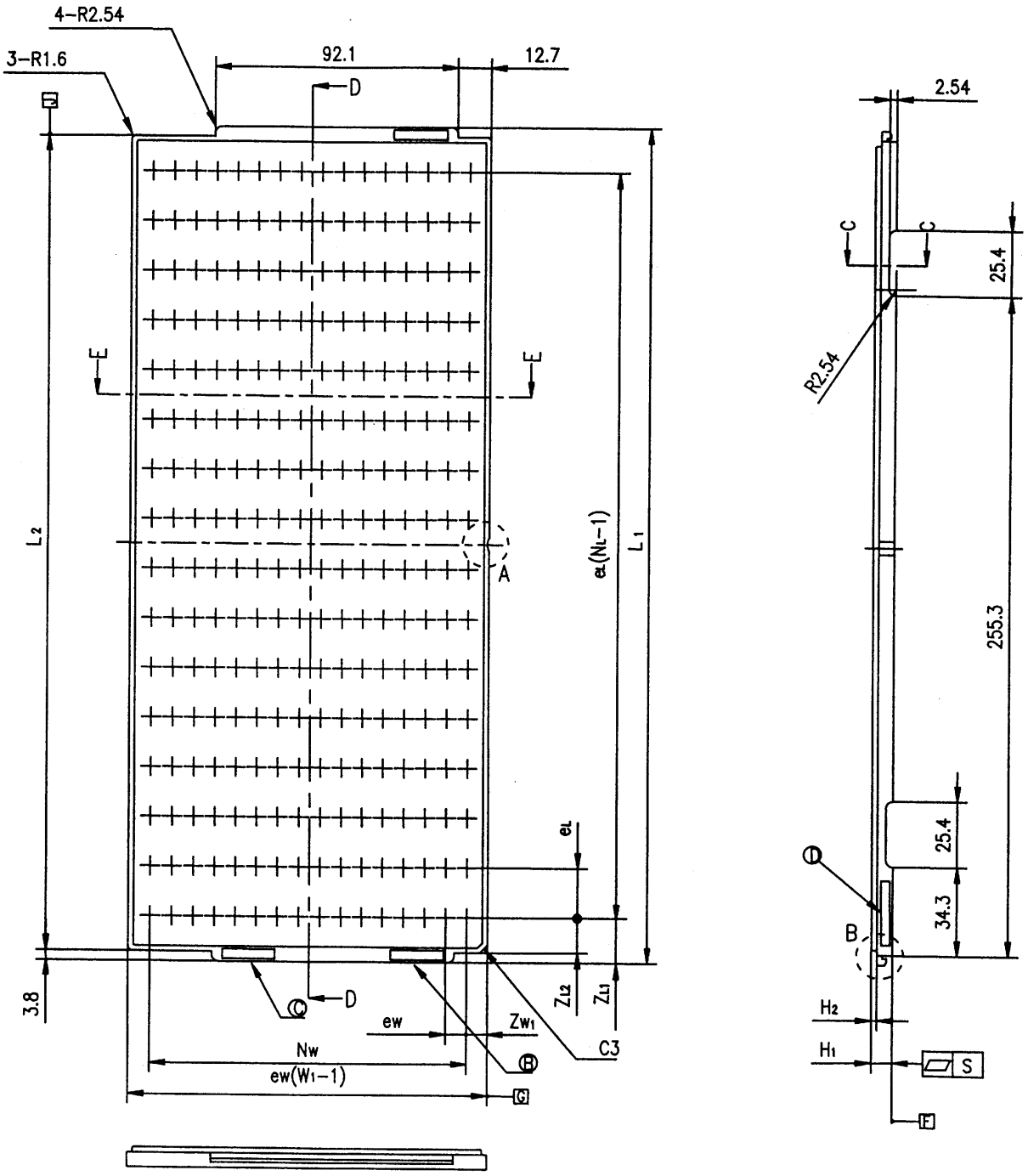
This technical report shall apply to QFP, TSOP, SOP, PGA and BGA packages. Tray size shall be referred to by the outside dimensions (reference Symbol: E x D) of the package.

4. Reference Symbols and Drawings

4.1 Outline drawing

Trays shall be outlined as drawn in **Figure 1.**

Figure 1 Outline drawing



4.2 Sectional detail drawing

Sectional areas of a tray shall be as drawn in detail in **Figures 2** through **6**.

Figure 2 A (Enlarged)

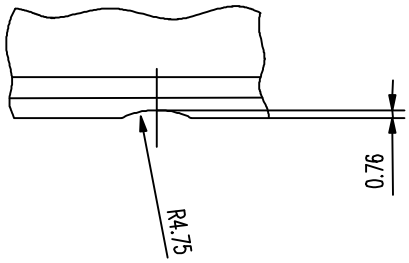


Figure 3 B (Enlarged)

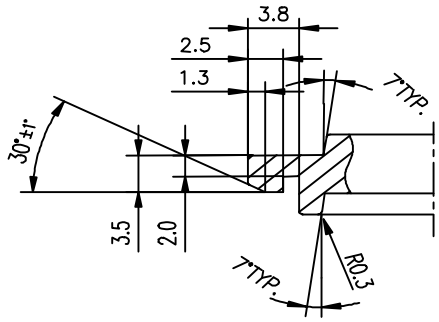


Figure 4 C-C (Enlarged)

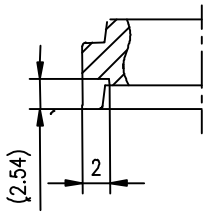


Figure 5 D-D (Enlarged)

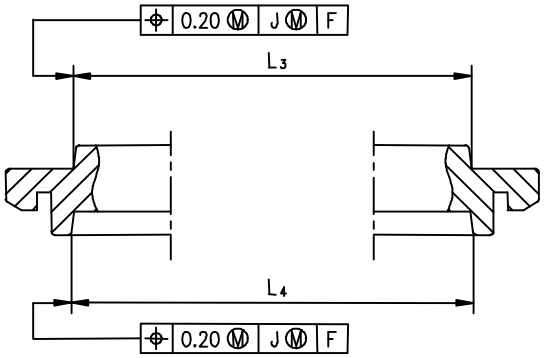
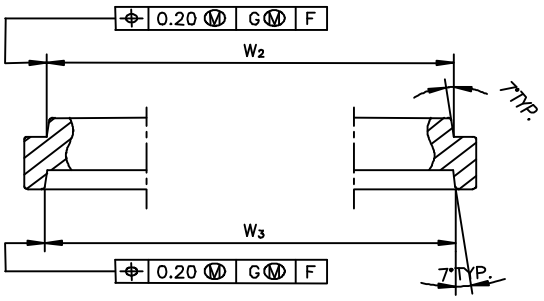


Figure 6 E-E (Enlarged)



4.3 Outside dimensions

Outside dimensions of a tray shall be determined as in **Table 1.**

Table 1 Outside dimensions

Unit: mm

Title	Reference Symbol	Standard	Remarks
Nominal size	E x D	Based on nominal size of package carried in tray	
Width of tray	W_1	(1) Nominal W_{1nom}=135.9 (2) Tolerance $W_1=W_{1nom}\pm0.25$	
Length of tray (including end tabs)	L_1	(1) Nominal L_{1nom}=322.6 (2) Tolerance $L_1=L_{1nom}\pm0.25$	
Length of tray (excluding end tabs)	L_2	(1) Nominal L_{2nom}=315.0 (2) Tolerance $L_2=L_{2nom}\pm0.25$	
Thickness of tray	H_1	(1) Nominal (a) Low profile type: H_{1mon}=7.62 (b) High profile type : H_{1mon}=12.19 (2) Tolerance $H_1=H_{1nom}\pm0.13$	
Width of tray stack convex area	W_2	(1) Nominal W_{2nom}=132.08 (2) Tolerance $W_2=W_{2nom}$	
Length of tray stack convex area	L_3	(1) Nominal L_{3nom}=311.15 (2) Tolerance $L_3=L_{3nom}$	
Tray stack margin in width direction	W_3-W_2	Tolerance W_3-W_2 = 0.13~0.89	Recommended W_3 value: W_{3nom}=132.59
Tray stack margin in length direction	L_4-L_3	Tolerance L_4-L_3=0.13~0.89	Recommended L_4 value: L_{4nom}=311.66
Tray stack height	H_2	(1) Nominal (a) Low profile type: H_{2nom}=1.27 (b) High profile type: H_{2nom}=2.03 (2) Tolerance $H_2=H_{2nom}\pm0.13$	

4.4 Pocket count/location and filler pocket location in width direction

Pocket count, end pocket location, pocket pitch and filler pocket location in the width direction of the tray, referred to by their corresponding reference Symbols in **Table 1**, shall be as specified in **Table 2**.

Table 2 Pocket count/location and filler pocket location in width direction

Pocket count	Location of end pocket (mm)	Pocket pitch (mm)	Filler pocket location	
N_W	Z_{W1}	e_W	Both ends	Center
2	35.10	65.70	1,2	1 or 2
3	24.15	43.80	2	2
4	18.75	32.80	2,3	2 or 3
5	15.35	26.30	3	2,3,4
6	13.20	21.90	3,4	3,4
7	11.70	18.75	4	3,4,5
8	10.55	16.40	4,5	4,5
9	9.55	14.60	5	4,5,6
10	9.00	13.10	5,6	4,5,6,7
11	8.20	11.95	6	5,6,7
12	8.00	10.90	6,7	5,6,7,8
13	7.35	10.10	7	6,7,8
14	7.50	9.30	7,8	6,7,8,9
15	6.70	8.75	8	6,7,8,9,10
16	6.45	8.20	8,9	7,8,9,10
17	6.35	7.70	9	7,8,9,10,11
18	5.90	7.30	9,10	8,9,10,11
19	5.85	6.90	10	8,9,10,11,12
20	6.20	6.50	10,11	8,9,10,11,12,13

4.5 Pocket count/location and filler pocket location in length direction

Pocket count, end pocket location, pocket pitch and filler pocket location in the length direction of the tray, referred to by their corresponding reference Symbols in **Table 1**, shall be as specified in **Table 3.**

Table 3 Pocket count/location and filler pocket location in length direction

Pocket count	Location of end pocket (mm)	Pocket pitch (mm)	Filler pocket location	
N_L	Z_{L2}	e_L	Both ends	Center
4	41.10	77.60	1,4	2 or 3
5	33.30	62.10	2,4	3
6	28.25	51.70	2,5	3 or 4
7	24.45	44.35	2,6	4
8	21.70	38.80	2,7	4 or 5
9	19.50	34.50	2,8	5
10	18.00	31.00	2,9	5 or 6
11	16.50	28.20	2,10	6
12	15.60	25.80	2,11	6 or 7
13	14.40	23.85	2,12	6,7,8
14	13.85	22.10	2,13	7,8
15	12.60	20.70	2,14	7,8,9
16	12.00	19.40	2,15	8,9
17	11.50	18.25	2,16	8,9,10
18	11.30	17.20	2,17	9,10
19	10.80	16.30	2,18	9,10,11
20	10.25	15.50	2,19	10,11
21	10.00	14.75	2,20	10,11,12
22	9.45	14.10	2,21	11,12
23	9.00	13.50	2,22	11,12,13
24	9.15	12.90	2,23	11,12,13,14
25	8.70	12.40	2,24	12,13,14
26	8.75	11.90	2,25	12,13,14,15
27	8.00	11.50	2,26	13,14,15
28	9.00	11.00	2,27	13,14,15,16
29	7.70	10.70	2,28	14,15,16
30	8.15	10.30	2,29	14,15,16,17
31	7.50	10.00	2,30	15,16,17
32	7.15	9.70	2,31	15,16,17,18
33	7.10	9.40	2,32	15,16,17,18,19
34	7.35	9.10	2,33	16,17,18,19
35	7.05	8.85	2,34	16,17,18,19,20

4.6 Calculations of pocket count/location

With the highest priority given to the number of packages accommodated, values shown in **Tables 2** and **3** are basically calculated according to the following formulas.

(1) D_W=E nom+W

(2) D_L=D nom+W

(3) N_W= (135.9-6.4)/D_W (Integer: decimals omitted)

(4) N_L= (315.0-6.4)/D_L (Integer: decimals omitted)

(5) Z_{W1}= [135.9-e_W (N_W-1)]/2

(6) e_W= [(135.9-6.4)-W(N_W-1)]/N_W+W

(7) Z_{L2}= [315.0-e_L(N_L-1)]/2

(8) e_L= [(315.0-6.4)-W(N_L-1)]/N_L+W

(9) Z_{L1}=Z_{L2}+3.8

Notes

1. Emax and Dmax are the nominal package dimensions determined by the EIAJ.

2. W is the minimum pocket-to-pocket pitch: 2.0 mm.

3. 3.2 mm wide peripheral area of the tray is excluded from the pocket area.

4. N_W and N_L are the numbers of pockets along the shorter and longer sides respectively. Therefore, the total number of pockets is N_W x N_L.

Explanation

1. Purpose

The purpose of this design guideline is to standardize the shapes and dimensions of trays used in shipment and production of encapsulated integrated circuits.

2. Background

Standardization of tray designs was proposed and selected as part of its activity plan at the 11th meeting of the sub-committee on the packing of semiconductor devices in March, 1997. Developed through discussion and consideration by the sub-committee, this design guideline was approved and established by the Technical Standardization Committee on Semiconductor Device Package. If new trays appear or questions occur in the future, it shall be supplemented or corrected as necessary.

3. Issues Settled by Discussion

This design guideline was prepared in consultation with EIA/JEDEC NO. 95-1 SEC 10. In order to prevent FBGA packages from jumping out from the tray, however, it was necessary to modify the A2 and W values specified in the guideline. Accordingly, the sub-committee proposed an individual EIAJ standard for FBGA trays (JC-11.5-08-178 FBGA Matrix Tray Design for Shipping and Handling) to the EIA/JEDEC, but this proposal was rejected by a vote of 7 to 7 with 8 abstentions at the JC-11.5 meeting held in October, 1998. After then, the EIA/JEDEC proposed a design guideline for FBGA packages of up to 1.2 mm in thickness. Discussion by the EIAJ revealed the following two facts.

(1) 2.5 mm was proposed as the W dimension as compared with the 3.5 mm proposed by the EIAJ.

(2) Package thickness must be considered up to 1.7 mm.

Accordingly, the sub-committee made a questionnaire survey on its member companies. The majority replied “W=2.5 mm is no problem” and “FBGA packages of 1.2 to 1.7 mm in thickness are popular”. Accordingly, at the EIA/EIAJ JWG#2-12 Fukuoka meeting in June, 1999, it was proposed to let the design guideline cover packages of up to 1.7 mm in thickness. As the result of discussion, it was decided to prepare a new design guideline (Low Stacking Profile Tray for BGA Packages) separately from this design guideline.

This design guideline drafted so far will be effective as an individual guideline.

Allowable warp and tolerance shall be specified in the respective individual standards.

4. Location of Filler Pockets for Vacuum Chuck

The filler pockets for vacuum chuck shall be formed as follows:

(1) One at the center of the tray and one on each end, as located in **Tables 2** and **3**.

(2) The center filler pocket shall be 32 x 32 mm at least.

5. Recommended device mount direction

(1) The longer sides of each package shall be in parallel with the longer sides of the tray.

(2) Pin 1 of each package shall face a chamfered corner of the tray or the central semicircle on a side of the tray.

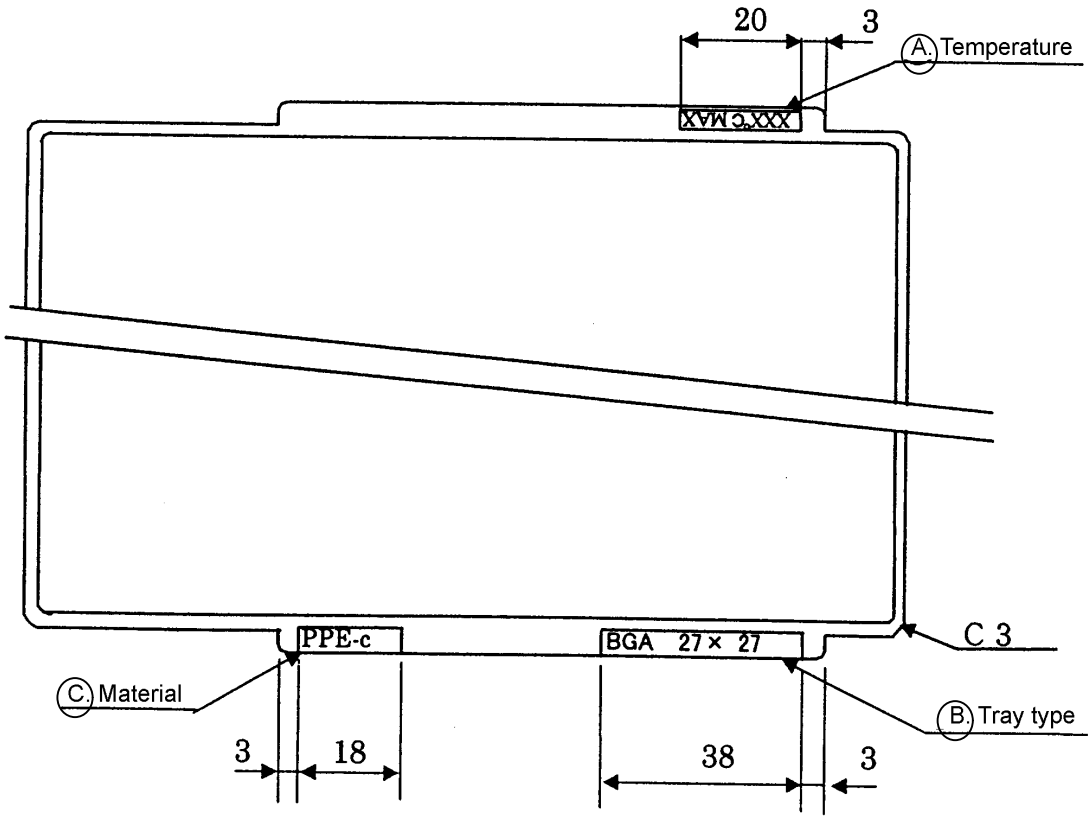
6. Warp

In this design guideline, the maximum allowable amount of warp shall be defined for the peripheral warp of the tray from the viewpoint of stability on a flat base. S_{MAX}=0.8 mm specified by the JEDEC shall be employed as recommended.

7. Marking

Temperature rating, tray type (package size) and material of the tray shall be indicated at Ⓐ, Ⓑ and Ⓒ respectively. It shall also be allowed to indicate the tray type (package size) at Ⓓ (see **Figure 1**)in addition B. Explanation **Figure 1** shows an example.

Explanation Figure 1　Marking



8. Deliberation committee

This standard was deliberated mainly by the subcommittee on Packing for Semiconductor Device in the Standardization Technical Committee on Semiconductor Device Package.

The committee members are shown below.

<Technical Standardization Committee on Semiconductor Device Package>

Chairman　Ichiro Anjoh　Hitachi, Ltd..

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Vice Chief	Masaaki Mukai	NEC Corp.
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	Tsunemori Yamaguchi	Rohm Inc.

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Member	Hirohide Takahashi	Oki Electric Industry Co.,Ltd.
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