

Technical Report of Japan Electronics and Information Technology Industries Association

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Making guideline of packing for lead-free semiconductor device

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Marking guideline of packing for lead-free semiconductor device

1. Scope of application

In regard to the shipping and packing materials for semiconductor products, this technical report specify a unified marking method to facilitate the discrimination of lead-free semiconductor products.

2. Definitions of terms

The definitions of major terms used in this technical report conform to the **EIAJ ED-7303**, and **JIS Z 0108** and new terms shall be defined herein.

(1) Semiconductor products

In this technical report, the term "semiconductor products" means integrated circuits, and passive parts (such as resistors and capacitors), connection parts (such as converters, cartridges) and elements constituting these parts are not included within the category of this term.

(2) Lead-free

In this technical report, the term "lead-free" means 0.1% by mass and less, which has been adopted by the World Lead-Free Soldering Roadmap Framework of 2002 by JEITA.

(3) Packaging materials

In this technical report, the term "packing materials" means packing materials for shipping of semiconductor products and the term includes dampproof packaging bags, inner boxes, outer boxes and reels.

3. Marking method

3.1 Marking symbol

A standard marking symbol is shown in Table 1.

Table 1 standard marking item			
Marking symbol	Details of marking		
Pb-Free T.	Product that does not contain any lead in the plate and electrodes of a terminal to be		
	attached to the substrate of a semiconductor product		
	Pb stands for lead and T. is an abbreviation of the term "Terminal".		

3.2 Size of marking characters

Marking characters shall be sufficiently large to be legible.

3.3 Typeface of marking characters

For a standard marking, the marking symbol shown in **Table 1** shall be used and its typeface may be determined arbitrarily.

3.4 Marking method and marking examples

Markings shall be provided on labels and if a marking is added to a shipping label, it shall appear only on the upper right hand corner of the shipping label as shown in **Figure 1**. If there is no marking space on the upper right hand corner, marking may appear in any blank space. Markings may arbitrarily be performed by inscription or printing, as long as they are not easily erased.

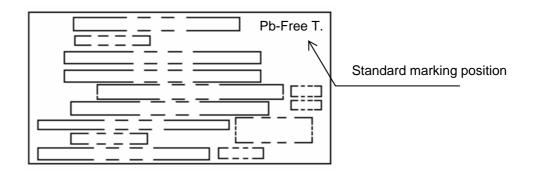
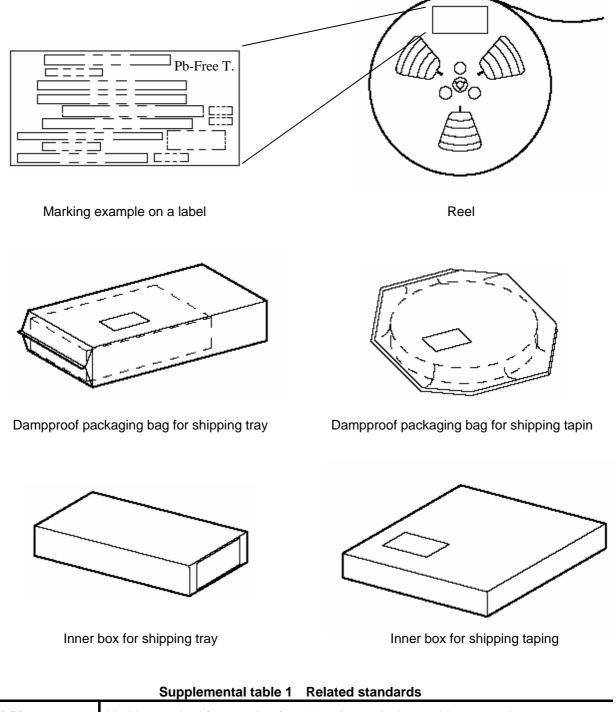


Figure 1 Marking example on a shipping label

4. Applicable objects for marking

This technical report shall apply to packing materials for shipping, on which markings may be provided in conformity with the provisions of **3.1**, **3.2**, **3.3** and **3.4** above, in principle.

5. Marking examples on packing materials for shipping



EIAJ ED-7631	Marking method for recycle of semiconductor device packing magazines		
EIAJ EDR-4701B	Handling guidance for semiconductor devices		
JIS Z 0108	Glossary of terms for packaging		

Explanation

1. Purpose of establishment of standards

In regard to the packing materials used for semiconductor products, this technical report specify a unified marking method to facilitate the discrimination of lead-free semiconductor products.

On November 1, 2000, the Electronic Industries Association of Japan (EIAJ) and the Japan Electronic Industries Development Association (JEIDA) merged to form the Japan Electronics and Information Technology Industries Association (JEITA).

2. Background for standards establishment

In 2002, the Subcommittee on Packing for Semiconductor Device made a proposal for marking rules and determined to deliberate on the proposal as a business plan. The subcommittee made a series of deliberations and examinations to pursue standardization and in December, 2003, this technical report were approved and established through document deliberation by members of the Technical Standardization Committee on Semiconductor Device Packages.

If any question arises in the future, deliberation/examination shall be made appropriately to revise as required.

3. Matters particularly discussed in deliberations

For this technical report, a questionnaire was made in connection with the marking of lead-free packing used by semiconductor manufacturers and deliberations were carried out. Although unified view was not reached, necessity for prompt standardization to handle environment problems was pointed out. Therefore, the Subcommittee on Packing for Semiconductor Device made a series of deliberations regarding this. In the beginning, some members insisted that this standardization should apply to all electronic parts, however, since a number of semiconductor manufacturers had already started lead-free marking on packing materials and without prompt standardization, it was evident that confusion would be inevitable. Accordingly, standardization was limited to semiconductors and the Subcommittee on Packing for Semiconductor Device was established.

One of the most essential items in preparing these guidelines was a marking symbol. As to the marking symbol for lead, two suggestions, that is, lead and Pb (chemical symbol for lead), were made. Therefore, a questionnaire to semiconductor manufacturers was carried out. In consideration of the performance record of semiconductor manufacturers that have already started to use Pb-Free T. and the number of characters that can be marked in the blank space of a label, the symbol, Pb, which has fewer characters, was adopted.

According to JEITA's World Lead-Free Soldering Roadmap Framework of 2002, as for the definition of "lead-free" classification carried out based on lead-free phases, some members insisted that markings on packing materials should conform to each phase, however, since it is difficult to use different labels based on phases, it was determined that the indication of Pb-free T. will uniformly be provided for any products that contain no lead for plating or electrodes of a terminal to be attached to a substrate (lead can be contained in components and materials of parts).

4. Committee members

This technical report was chiefly deliberated by the Sub-committee on Packing for Semiconductor Device under the Technical Standardization Committee on Semiconductor Device Packages. Members of the committee are noted below.

< Technical Standardization Committee on Semiconductor Device Package >

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