Technical Report of Japan Electronics and Information Technology Industries Association

EIAJ EDR-7712

Design guideline of open-top type socket for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (FBGA/FLGA)

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JEITA EDR-7712

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Design guideline of open-top type socket for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array (FBGA/FLGA)

1. Scope of Application

This technical report defines the outline drawing and dimensions of the open-top type socket out of the test and burn-in sockets applied to the fine-pitch ball grid array package (“FBGA” hereafter) and fine-pitch land grid array package (“FLGA” hereafter) provided in **EIAJ EDR-7316** [Design guideline of Integrated Circuits for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array] and **EIAJ EDX-7316** [Design guideline of Integrated Circuit for Fine-pitch Ball Grid Array and Fine-pitch Land Grid Array in Rectangular Package outline] .

2. Definition of Technical Terms

The main terms used in this technical report shall conform to those defined in the **EIAJ ED-7300** [Recommended practice on standard for the preparation of outline drawings of semiconductor packages] and **EIAJ ED-7701** [Glossary of socket for BGA, LGA, FBGA and FLGA]. The new terms not included therein shall be defined in the text of this technical report.

3. Background

This technical report aims to standardize the outer dimensions of the sockets for FBGA and FLGA, where more attention is currently paid, to establish their compatibility as the need for the surface mount type rapidly increased due to enhanced functions and performance of electrical devices.

For defining each dimension, the object was to indicate the design standard value that is the concept of the design center as much as possible, aiming to enhance the function as a standardization index.

4. Socket Code

4.1 Construction of Socket Code

Socket Code is constructed as follows:

Symbol of Socket **4.2 (1)**	-	Symbol of Socket type **4.2(2)**	-	Symbol of nominal dimension **4.2(3)**	-	SocketNumber of terminal arrays **4.2(4)**	-	Terminals pitch **4.2(5)**
Example SFB	-	TX	-	2120AB	-	1616	-	080

4.2 Symbols

(1) Semiconductor sockets symbol

The symbol for socket shall be expressed in 3 letters. The first letter, “S” refers to socket and the rest to the package code. FBGA shall be expressed as “FB”, FLGA shall be expressed as “FL”.

(2) Socket Type Symbol

The symbol for Socket Type shall be expressed in 2 letters. The first letter “T” refers to open top type and the rest remains option. Clamshell type socket is referred to as “C”.

(3) Socket nominal dimension symbol

The symbol of socket type shall be expressed in 6 letters, which are 4 numeric letters and 2 alphabetical letters. First 4 numeric letters comply with nominal dimension E x D which refers to applicable maximum width and length of FBGA/FLGA package.

The last 2 alphabetical letters refers to socket base terminal row number either an even or an odd.

It refers to an odd contact row by “A” and an even contact row by “B” in order socket width direction and next socket length direction.

Namely, it refers to “AA” in case row number is an odd at both for width and length direction, “BB” in case row number is an even at both for width and length direction, “AB” in case row number is an odd at width direction and an even at length direction and “BA” in case row number is an even at width direction and an odd at length direction.

(4) Number of terminal arrays

The symbol for number of terminal arrays shall be expressed by 4 numeric letter applying applicable package terminal row number expressed in ME x MD

(5) Terminal pitch

The symbol for terminal pitch of applicable package shall be expressed in 3 numeric letters.

A decimal [.] is omitted.

5. Terminal Number

Terminal number is provided with following manner when socket is viewed with angle from topside. The horizontal row nearest to the index corner when the index is placed on the left –topside is referred to A. As the row moves down, the number changes in order of B, C, ……. AA, AB.

1 is defined for the vertical row nearest to the index corner. As the row moves rightward, the number is increases 2, 3, …… Terminal number is combined with these alphabets and numbers and expressed as A1 or B1. I, O, Q, S, X and Z are not used as symbol for horizontal row.

6. Nominal Dimensions

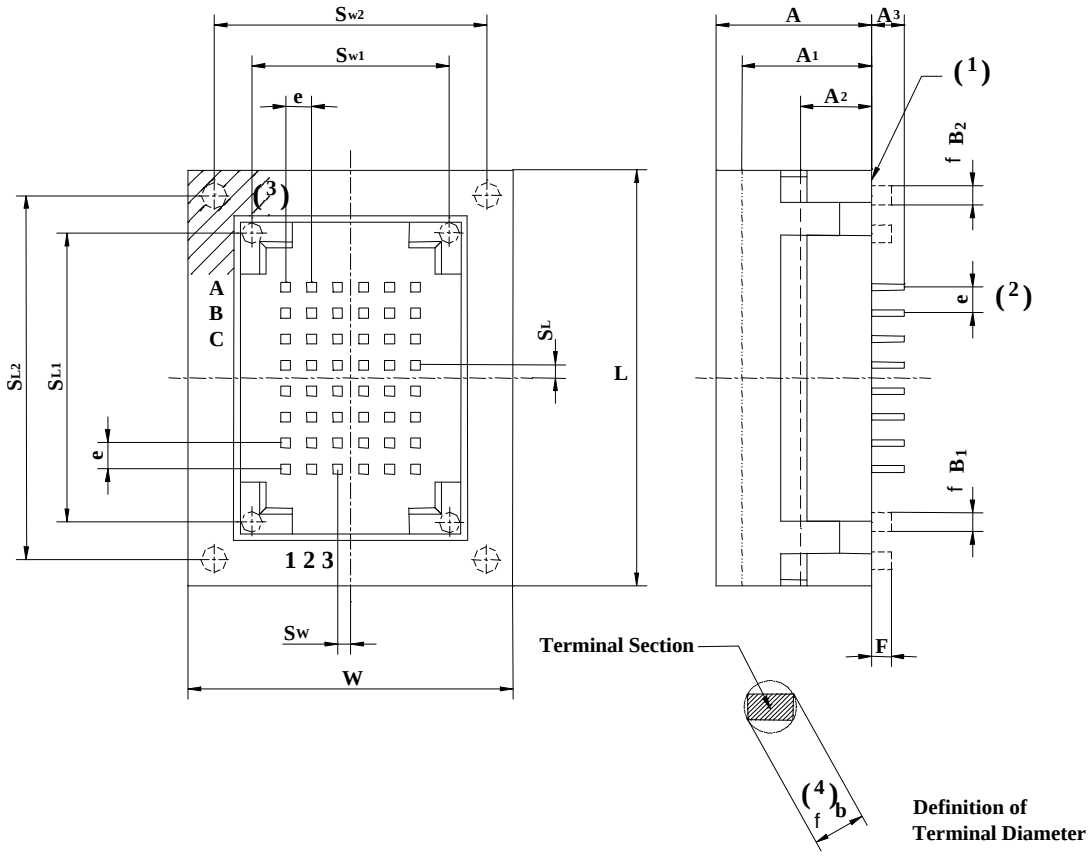
In this technical report, maximum nominal dimension of the package (E x D) applicable with a socket is used as the nominal dimension of the socket.

7. Reference Symbols and Schematics

7.1 Outline Drawings

Outline drawings of the socket are shown in **Figure 1** and that for applicable package is in **Figure 2**.

Figure 1



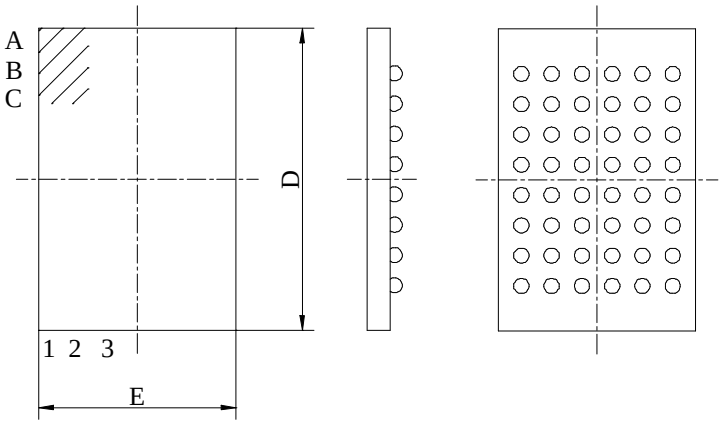
Notes:(1) Indicates mounting plane. Mounting plane is defined by the plane where the socket contacts its mounting surface.

(2) Stipulates true geometric position of the terminals.

(3) Indicates positional tolerance of the index mark. Index mark should be completely within the shaded area.

(4) Terminal diameter is defined as the maximum diameter of a circle circumscribed about a vertical projection of the terminal from the mounting plane.

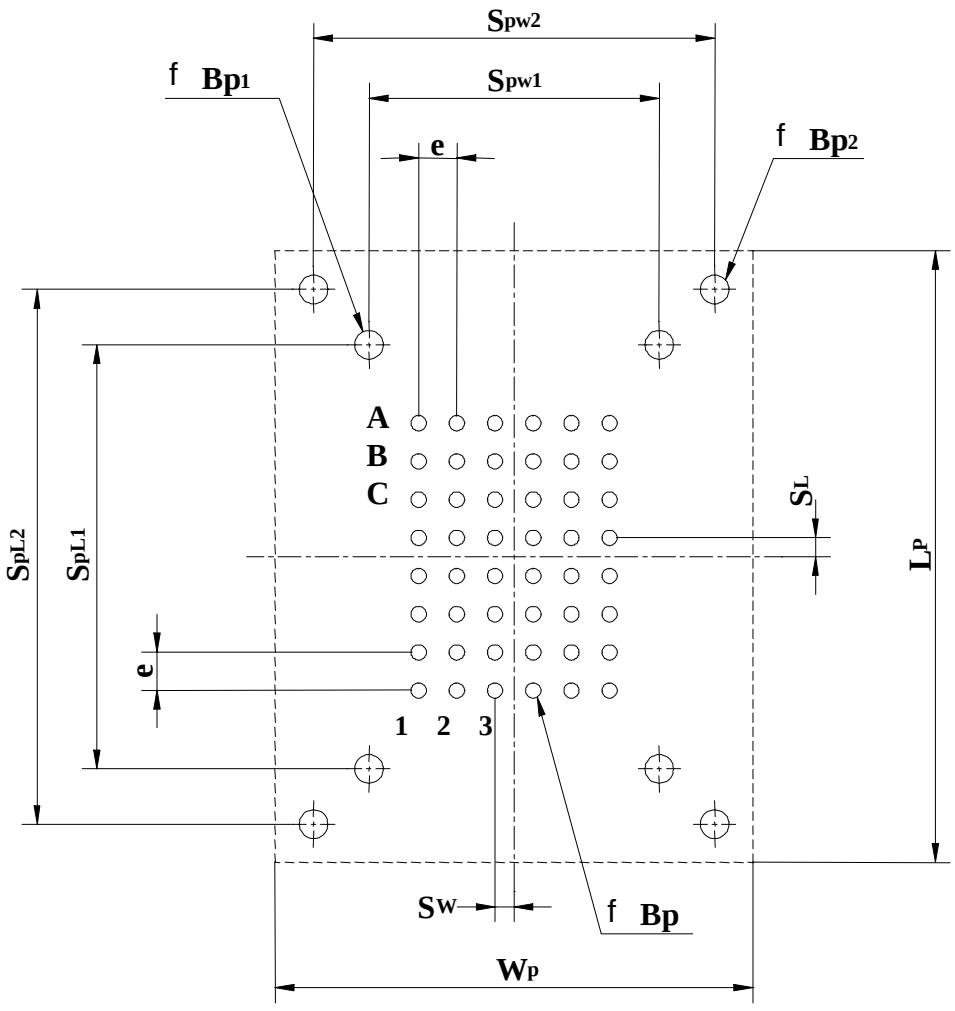
Figure 2



7.2 Reference Symbols and Schematics of Recommended Socket Mounting Pattern on Printed Circuit Board

The drawing of the recommended socket mounting pattern on printed circuit board is shown in **Figure 3** for reference in printed circuit board designing.

Figure 3



7.3 Overall Dimensions

Table 1

Unit: mm

Name	Reference symbol	Stipulations	Recommended value	Supplement
Socket Nominal dimension	E x D	This value is based on the nominal dimensions of conformable FBGA and FLGA to the socket	-	**Table 2**
Socket length	L	Socket length: L nominal defined. L=W (group 4 is exception.)	-	**Table 2**
Socket width	W	Socket width: W nominal defined W=L (group 4 is exception.)	-	**Table 2**
Socket height	A	A max = 22.0	-	
End stroke height	A_1	A_1 max = 16.0	14.0 13.5	
Seating plane Height	A_2	A_2 max = 14.0	9.7 8.2	
Terminal distance	e	e = 0.80 e = 0.65 e = 0.50 e = 0.40	-	
Terminal length	A_3	A_3 = 0.7 to 6.3	-	
Terminal diameter	Øb	Maximum distance of the terminal cross section E | Øb max 0.80 | 0.28 0.65 | 0.21 0.50 | 0.20 0.40 | 0.19	-	
Number of Alignment pin (inside)	n_1	n_1= 0, 2, 3, 4 (either one to be selected)	-	
Number of Alignment pin (outside)	n_2	n_2= 0, 2, 3, 4 (either one to be selected)	-	
Alignment pin Length	F	Fmin=1.0	-	
Distance between Alignment pin in L dimension (inside)	S_{L1}	Group 1, 2, 3 = Socket nominal dimension plus 5.0 Group 4 = No pin exist	-	**Table 2**
Distance between Alignment pin in W dimension (inside)	S_{W1}	Group 1, 2, 3 = Socket nominal dimension plus 5.0 Group 4 = No pin exist	-	**Table 2**

Table 1 (continued)

Unit: mm

Name	Reference symbol	Stipulations	Recommended value	Supple-ment
Distance between Alignment pin in L dimension (outside)	S_{L2}	Group 1 = Socket nominal dimension plus 30.0 Group 2 = Socket nominal dimension plus 18.0 Group 3 = Socket nominal dimension plus 9.0 Group 4 = Socket nominal dimension plus 5.0	-	**Table 2**
Distance between Alignment pin in W dimension (outside)	S_{W2}	Group 1 = Socket nominal dimension plus 30.0 Group 2 = Socket nominal dimension plus 18.0 Group 3 = Socket nominal dimension plus 9.0 Group 4 = Socket nominal dimension plus 5.0	-	**Table 2**
Alignment pin diameter (inside)	$ØB_1$	$ØB_1$ max = 1.5	-	
Alignment pin diameter (outside)	$ØB_2$	Group 1 and 2 = $ØB_2$ max = 2.0 Group 3 and 4 = $ØB_2$ max =1.5	-	**Table 2**
Center terminal position in L-direction	S_L	When M_L is an odd number, $S_L = 0$ When M_L is an even number, $S_L = e / 2$	-	
Center terminal position in W-direction	S_W	When M_W is an odd number, $S_W = 0$ When M_W is an even number, $S_W = e / 2$	-	
Number of terminals	n	Maximum terminal number and its matrix number shall be equal to number which are specified in **EIAJ EDR-7316** and **EIAJ EDX-7316**. Matrix ray out with partially depopulated terminal is accepted.	-	
Matrix size in L-direction	M_L			
Matrix size in W-direction	M_W			
Package setting direction		Direction of shifting for Package Insertion. This is to provide the direction of package shifting in order to ensure uniformity when fitting a package to a socket that has a larger terminal matrix than the package, when that package has an odd number of rows less than the socket. The direction of shifting shall be upper left.	-	

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Table 2

Unit: mm

Package outline		Socket nominal dimension plus E x D		Socket length and width							
				Group 1		Group 2		Group 3		Group 4	
D	E	D	E	L	W	L	W	L	W	L	W
1.50	1.50	5	5	45.0	45.0	33.0	33.0	21.0	21.0	13.0	13.0
2.00	2.00										
2.50	2.50										
3.00	3.00										
3.50	3.50										
4.00	4.00										
4.50	4.50										
5.00	5.00										
5.50	5.50	6	6							14.0	14.0
6.00	6.00										
6.50	6.50	7	7							15.0	15.0
7.00	7.00										
7.50	7.50	8	8							16.0	16.0
8.00	8.00										
8.50	8.50	9	9							17.0	17.0
9.00	9.00										
9.50	9.50	10	10	49.0	49.0	37.0	37.0	25.0	25.0	18.0	18.0
10.00	10.00										
10.50	10.50	11	11							19.0	19.0
11.00	11.00										
11.50	11.50	12	12							20.0	20.0
12.00	12.00										
12.50	12.50	13	13							21.0	21.0
13.00	13.00										
13.50	13.50	14	14	53.0	53.0	41.0	41.0	29.0	29.0	22.0	22.0
14.00	14.00										
14.50	14.50	15	15							23.0	23.0
15.00	15.00										
15.50	15.50	16	16							24.0	24.0
16.00	16.00										
16.50	16.50	17	17							25.0	25.0
17.00	17.00										
17.50	17.50	18	18	57.0	57.0	45.0	45.0	33.0	33.0	26.0	26.0
18.00	18.00										
18.50	18.50	19	19							27.0	27.0
19.00	19.00										
19.50	19.50	20	20							28.0	28.0
20.00	20.00										
20.50	20.50	21	21							29.0	29.0
21.00	21.00										

7.4 Recommended Dimensions of Socket Mounting Pattern on Printed Circuit Board

Table 3

Unit: mm

Name	Reference symbol	Stipulations	Recommended value	Supplement
Socket mounting length	L_p	Socket mounting length: L_p max $L_p = L + 0.8$	-	
Socket mounting Width	W_p	Socket mounting width: W_p max $W_p = W + 0.8$	-	
Terminal length	A_3	A_3 = 0.7 to 6.3	-	
Through hole diameter	$Øb_p$	Through hole diameter: $Øb_p$ min E: 0.80 → $Øb_p$ min: 0.30 E: 0.65 → $Øb_p$ min: 0.23 E: 0.50 → $Øb_p$ min: 0.22 E: 0.40 → $Øb_p$ min: 0.20	-	
Distance between holes for alignment pin in L dimension (inside)	S_{PL1}	Group 1, 2, 3: Socket nominal dimension plus 5.0 Group 4: No holes exist	-	**Table 2**
Distance between holes for alignment pin in W dimension (inside)	S_{PW1}	Group 1, 2, 3: Socket nominal dimension plus 5.0 Group 4: No holes exist	-	**Table 2**
Distance between holes for alignment pin in L dimension (outside)	S_{PL2}	Group 1: Socket nominal dimension plus 30.0 Group 2: Socket nominal dimension plus 18.0 Group 3: Socket nominal dimension plus 9.0 Group 4: Socket nominal dimension plus 5.0	-	**Table 2**
Distance between holes for alignment pin in W dimension (outside)	S_{PW2}	Group 1: Socket nominal dimension plus 30.0 Group 2: Socket nominal dimension plus 18.0 Group 3: Socket nominal dimension plus 9.0 Group 4: Socket nominal dimension plus 5.0	-	**Table 2**
Hole diameter of alignment pin (inside)	$ØB_{p1}$	$ØB_{p1min}$= 1.6	-	
Hole diameter of alignment pin (outside)	$ØB_{p2}$	Group 1 and 2 = $ØB_{p2min}$= 2.1 Group 3 and 4 = $ØB_{p2min}$= 1.6	-	

8. Individual Outline Drawing Standard Registration

To propose the registration of an individual standard for a new outline, section marked with (*) table shown below shall be filed with dimensions or letters.

Table 4

Reference Number			
Socket Code	***-**-*****-****-***-**		
Reference Symbol	Minimum	Nominal	Maximum
L		*	
W		*	
A			*
A_1			*
A_2			*
e		*	
A_3	*	*	*
Øb			*
n_1	*		*
n_2	*		*
F	*		
S_{L1}		*	
S_{W1}		*	
S_{L2}		*	
S_{W2}		*	
$ØB_1$			*
$ØB_2$			*
S_L		*	
S_W		*	
N		*	
M_L		*	
M_W		*	

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EXPLANATION

1. Purpose of Establishment

This technical report was established for the purpose to pursue standardization of FBGA/FLGA open top socket and to show design guideline of the socket and its related parts.

Electronic Industries Association of Japan (**EIAJ**) and the Japan Electronic Development Association (**JEIDA**) have marged effective November 1, 2000, the Japan Electronics and Information Technology Industries Association (**JEITA**).

2. Process of Deliberation

Standardization of semiconductor package has been actively executed by JEDEC/JC-11 in U.S.A. and by EIAJ/Technical Standardization Committee on Semiconductor Device Package in Japan. On the other hand, test and burn-in socket, which is indispensable for development of package, has been developed independently by each semiconductor maker and socket maker with their own specifications.

In such situation, necessity of the standardization activity of the socket was raised and then establishment of Semiconductor Socket Project Group (PG) was approved by Technical Standardization Committee on Semiconductor Device Package.

As the standardization activity of this PG, design guide for the Glossary of Semiconductor Socket and BGA Open Top Type Socket were discussed and the result has been published upon approval by the committee. Afterwards, importance of the socket standardization was recognized and this PG reorganized as Semiconductor Socket Sub-committee for further activities since April 26, 2000.

Approximately two year was spent until the Design Guideline was issued because of the difficulty to unify sockets which the makers have completed its development. This design guideline is expected to be functional as a standard for development of new FBGA/FLGA sockets although range of dimension became extensive as the result to include sockets currently available as many as possible.

In regards to description on datum definition which is relating to dimension of distance between alignment pins, alignment pin holes, diameter of alignment pin, alignment pin holes and length and width of socket, it is decided to leave the issue to future examination because of difficulty to define exact dimensions at this stage where tolerant standard is applied.

3. Background of Respective Standard Defined

(1) Scope of application

This design guideline defines open-top type socket applied to Fine-pitch Ball Grid Array (FBGA) and Fine-pitch Land Grid Array (FLGA) which has been defined by **EIAJ EDR-7316** and **EIAJ EDX-7316**, Design Guideline for FBGA/FLGA. Design Guideline for these packages, **EIAJ EDR-7316** and **EIAJ EDX-7316**, are expected to be consolidated within year of 2000 as unified design guideline. After its consolidation, definition of socket in this Design Guideline means semiconductor socket applicable to all packages of FBGA/FLGA standardized by newly consolidated design guideline.

(2) Socket code

As a symbol to designate a socket code, not only the socket nominal dimension but also the number of applicable terminal matrix of FBGA/FLGA was applied. The reason is that the nominal dimension does not always include the length and width of the applicable FBGA/FLGA package. For details, refer to the appendix; “Example of application on FBGA/FLGA package and IC Socket”.

(3) Nominal dimension

Basically largest nominal dimension of the FBGA/FLGA is used as the dimension of the socket which is applicable to the package If the socket length and width are used as the nominal dimension, it is difficult to judge if a given package is able to be accommodated by the selected socket. Variation of the socket nominal dimension will be too extensive in case all dimensions of the package is applied to socket as well since package nominal dimension is defined with the increment of 0.5mm such as 1.5mm~21.0mm. In order to prevent such inconvenience, socket nominal dimension was limited to 4 variations covering all package nominal dimensions. In fact, a socket is used in many cases for several packages replacing a part of socket component. However, nominal dimension with 1.0mm increment is also accepted for the case of specific need for ultimately small socket outline. Package with its nominal dimension less than 5.0mm is assumed to be uncommon case and such packages shall be included in the package of 5.0mm. Dimension less and decimal point shall be round up.

(4) Length and width of socket

Since the socket length and width dimensions vary due to the difference of its terminal count and mechanism, they were categorized into 4 groups which is from group 1 to group 4. Length and width of the socket categorized in group 1, 2, and 3 shall be largest nominal dimension plus 36.0mm, 24.0mm and 12.0mm respectively and that for socket in group 4 shall be 8.0mm. Socket in group 1 is supposed to accommodate high terminal count or FLGA which require complicated structure. Sockets currently available are categorized into group 2 and 3 Socket which is required with its smallest possible outline dimension such as for Memory IC FBGA/FLGA is categorized into group 4. Only square outline is approved in group 1, 2 and 3 but rectangular outline is also accepted in group 4 in order to accommodate the requirement for smallest possible outline. These length and width dimensions are specified with its nominal dimension considering needs of compatibility when the socket is used with IC handler or IC loader/unloader.

The length and width were limited to define with its maximum dimension since those dimensions are required by semiconductor makers for their printed circuit board design.

(5) Socket height, seating plane height and end stroke height

These dimensions were defined based on the sockets currently available.

Seating plane height is defined with two recommended values in order to accommodate different terminal number and various structure of FLGA socket

(6) Terminal length and diameter

Wide range terminal length was specified because the terminals should slightly extrude from the backside of the printed circuit board the thickness of which varies with the number of board layers in order to solder the terminals on printed circuit board securely. The terminal diameter was defined based on the dimensions of the socket currently available.

(7) Alignment pin

It was unable to standardize the alignment pin with the consideration to sockets currently available since the pin have been required for various kinds of purpose such as for alignment of the socket to the printed circuit board and for ease of terminal insertion to the printed circuit board. Therefore, the number of pins was specified with wide range of choice from 0 to 8, and only the minimum length was specified as an inevitable dimension. Position of the pin was determined assuming the internal pin is used to align the terminals to the printed circuit board and the external pin is used to align the socket housing to the printed circuit board. The pin diameter was defined based on the dimensions of the socket currently available. As an option, screw hole for mounting of the socket on printed circuit board may also be accepted instead of alignment pin.

Sockets categorized in group 4 may be with no inside alignment pin because the area for pin fitting is limited due to its small length and width such as nominal dimension plus 8.0mm

(8) Number of terminals and matrix

The number of terminals the socket must comply with that for package specified in **EIAJ EDR-7316** and **EIAJ EDX-7316**. Matrixes with partially depopulated terminals are allowable.

(9) Package setting direction

When an even/uneven socket terminal matrix is not consistent with that of FBGA/FLGA terminal matrix, for example, when number of the socket terminal row is 26 and that for the FBGA/FLGA is 25, the FBGA/FLGA have to be shifted to a side in the socket. This shifting direction is required to be unified in order to assure right connection between the socket and the FBGA/FLGA. For details, refer to the “Examples of application on FBGA/FLGA package and IC Socket” in next page.

(10) Socket mounting length and width

As a reference to design the printed circuit board, the dimension of geographic area need for socket mounting and operation was defined. The socket length and width plus 0.8mm was specified as the mounting length and width considering the socket outline dimensional tolerance, the alignment pin positional tolerance and the printed circuit board dimensional tolerance.

(11) Through hole diameter

Through hole diameter is key dimension to design the circuit pattern of printed circuit boards, then it was specified in accordance with the popular dimension currently applied.

(12) Alignment hole diameter

This diameter was specified for “alignment pin diameter +0.1mm”, considering the tolerances of the socket and the printed circuited board.

4. Examples of Application on FBGA package and IC Socket

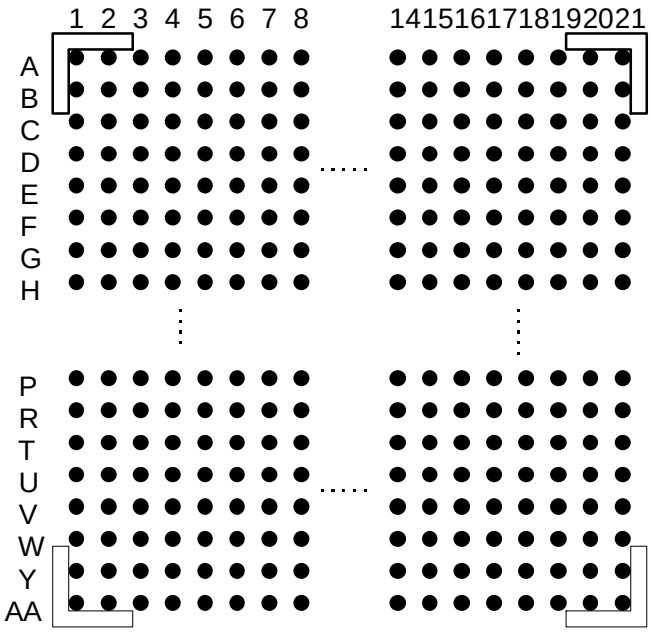
(1) IC Socket: Nominal dimensions 17x17,

Matrix size of W-direction M_W=21, Matrix size of L-direction M_L=21, Terminal pitch e=0.80

(a) In case of FBGA package: Length x Width = 17x17,

Matrix size in E-direction M_E=21, Matrix size in D-direction M_D=21

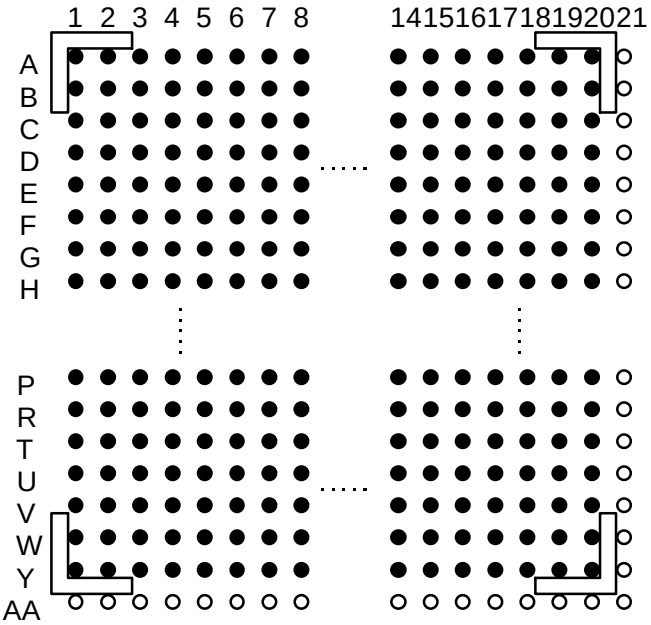
Socket code = **SFB-T-1717AA-2121-080**



(b) In case of FBGA package: Length x Width = 17x17,

Matrix size in E-direction M_E=20, Matrix size in D-direction M_D=20

Socket code = **SFB-T-1717AA-2020-080**

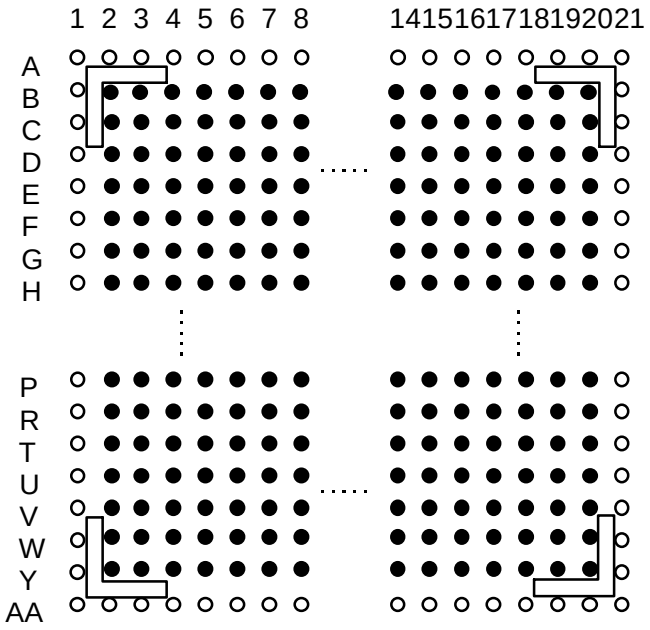


Above drawings are shown from the top side of the Socket (Package mounting surface), and black dots mean the contact area with FBGA terminals, and white dots mean the contact area without FBGA terminals.

(c) In case of FBGA package: Length x Width = 17x17,

Matrix size in E-direction M_E=19, Matrix size in D-direction M_D=19

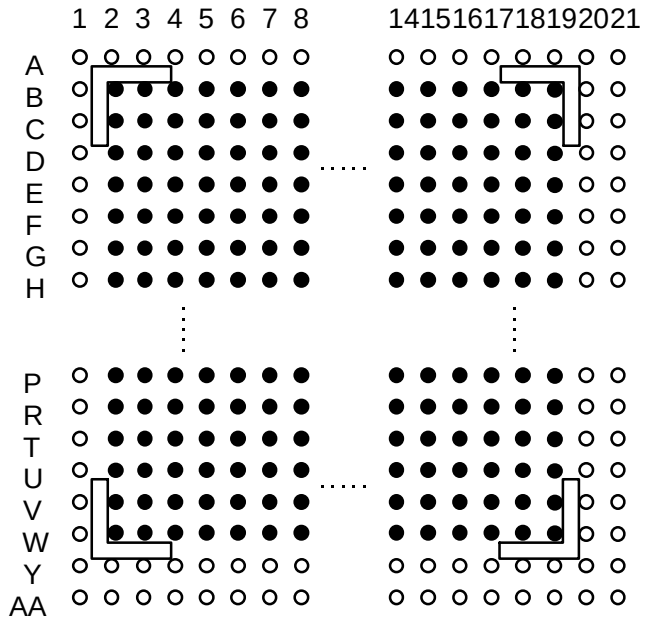
Socket code **= SFB-T-1717AA-1919-080**



(d) In case of FBGA package: Length x Width = 15x15,

Matrix size in E-direction M_E=18, Matrix size in D-direction M_D=18

Socket code = **SFB-T-1717AA-1818-080**



Above drawings are shown from the top side of the Socket (Package mounting surface), and black dots mean the contact area with FBGA terminals, and white dots mean the contact area without FBGA terminals..

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(2) IC Socket: Nominal dimensions 14x17,

Matrix size of W-direction M_W=16, Matrix size of L-direction M_L=21, Terminal pitch e=0.80

(a) In case of FBGA package: Length x Width = 14x17,

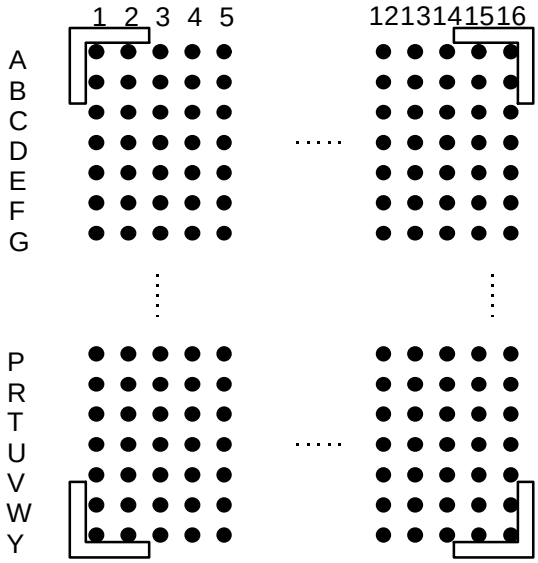
Matrix size in E-direction M_E=17, Matrix size in D-direction M_D=21

Socket code = Impossible

(b) In case of FBGA package: Length x Width = 14x17,

Matrix size in E-direction M_E=16, Matrix size in D-direction M_D=21

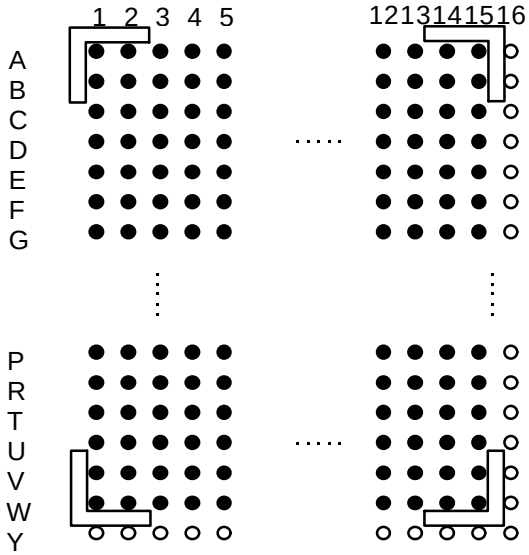
Socket code = **SFB-T-1417BA-1621-080**



(c) In case of FBGA package: Length x Width = 14x17,

Matrix size in E-direction M_E=15, Matrix size in D-direction M_D=20

Socket code **= SFB-T-1417BA-1520-080**

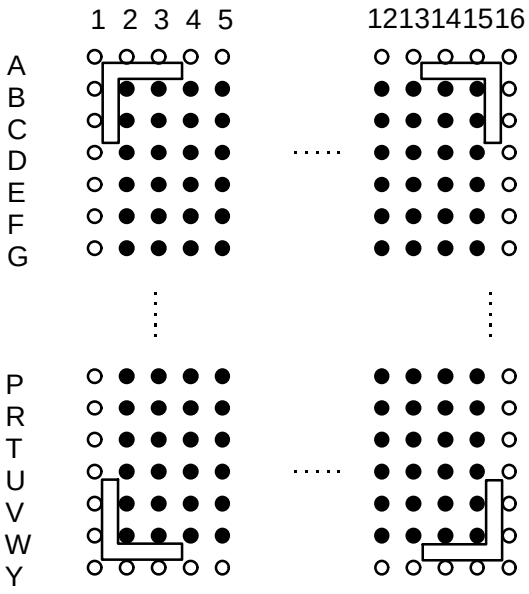


Above drawings are shown from the top side of the Socket (Package mounting surface), and black dots mean the contact area with FBGA terminals, and white dots mean the contact area without FBGA terminals..

(d) In case of FBGA package: Length x Width = 13x16,

Matrix size in E-direction M_E=14, Matrix size in D-direction M_D=19

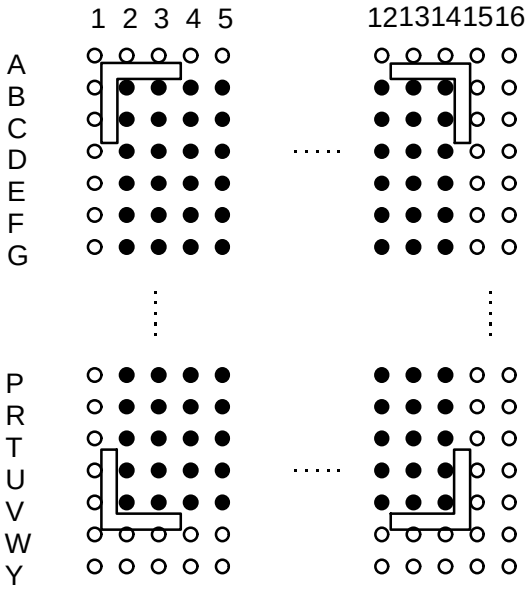
Socket code = **SFB-T-1417BA-1419-080**



(e) In case of FBGA package: Length x Width = 12x16,

Matrix size in E-direction M_E=13, Matrix size in D-direction M_D=18

Socket code = **SFB-T-1417BA-1318-080**



Above drawings are shown from the top side of the Socket (Package mounting surface), and black dots mean the contact area with FBGA terminals, and white dots mean the contact area without FBGA terminals.

5. Members of the Committee

This design guideline was deliberated by Semiconductor Socket Project Group of Technical Standardization Committee on Semiconductor Device Package.

The members are as shown below.

<Technical Standardization Committee on Semiconductor Device Package>

Chairman:	Ichiro Anjoh	Elpida Memory, Inc.

<Semiconductor Socket Project Group>

Chief Examiner:	Kazuhiro Tashiro	Fujitsu Ltd.
Vice-Chief Examiner:	Hidekazu Iwasaki	Mitsubishi Electric Corporation
	Shunji Abe	Yamaichi Electronics Co.,Ltd.
	Shuji Inoue	Intel Corporation
	Kazumasa Sato	Wells-CTI K.K.
	Tsutomu Kashiwagi	Enplas Corporation
	Hiroaki Hirao	Samsung Japan Corporation
	Tohru Hayashi	SANYO Electric Co.,Ltd.
	Syouzou Yokoyama	Shinon Electric Industry Co.,Ltd
	Takayuki Nagumo	Sumitomo 3M Limited
	Kazuo Yazawa	Seiko Epson Corp.
	Teruto Yamauchi	Sony Corporation
	Yoichi Kimura	Toshiba Corporation
	Tsuneo Kobayashi	IBM Japan,Ltd.
	Masao Tohyama	Texas Instruments Japan Ltd.
	Hiroyuki Hosogi	Texas Instruments Japan Ltd.
	Hiroshi Yamanouchi	NEC Corporation
	Akira Kaneshige	Molex Japan Co.,Ltd.
	Yuji Wada	Hitachi,Ltd.
	Shigeru Kuriyama	Matsushita Electronics Corporation
	Shinichi Nakamura	Unitechno Inc.
	Osamu Miyata	Rohm Co.,Ltd.